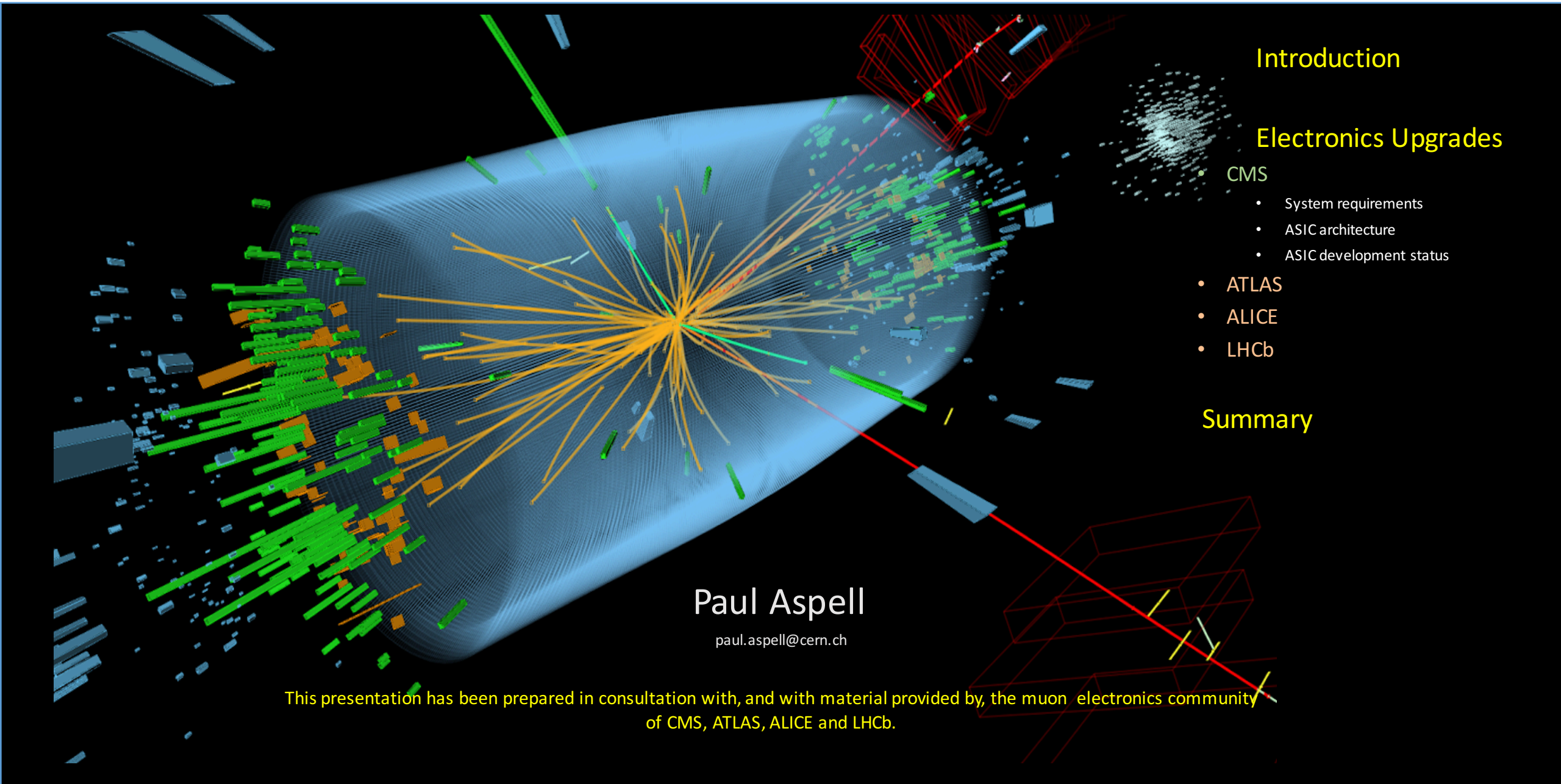
Overview of the ASIC Developments for the Muon Upgrades



Introduction

Electronics Upgrades

- CMS
  - System requirements
  - ASIC architecture
  - ASIC development status
- ATLAS
- ALICE
- LHCb

Summary

Paul Aspell

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This presentation has been prepared in consultation with, and with material provided by, the muon electronics community of CMS, ATLAS, ALICE and LHCb.

General reasons for Muon upgrades

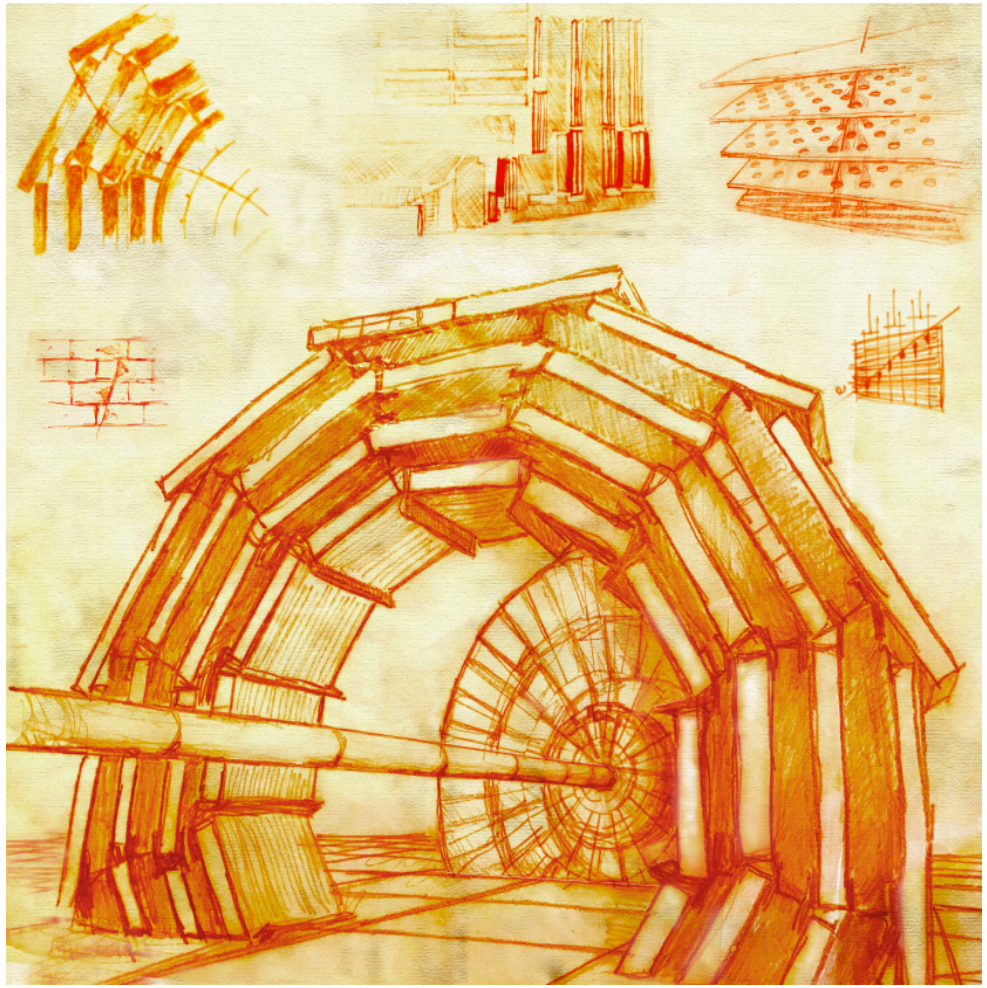
Detectors :
Most Muon systems use a form of gas detector.
Most of these detectors are expected to remain into Phase 2.

Some however need to be replaced, particularly in regions of significantly high rate. In these regions, new detectors with higher rate capabilities and finer granularity are being brought in.

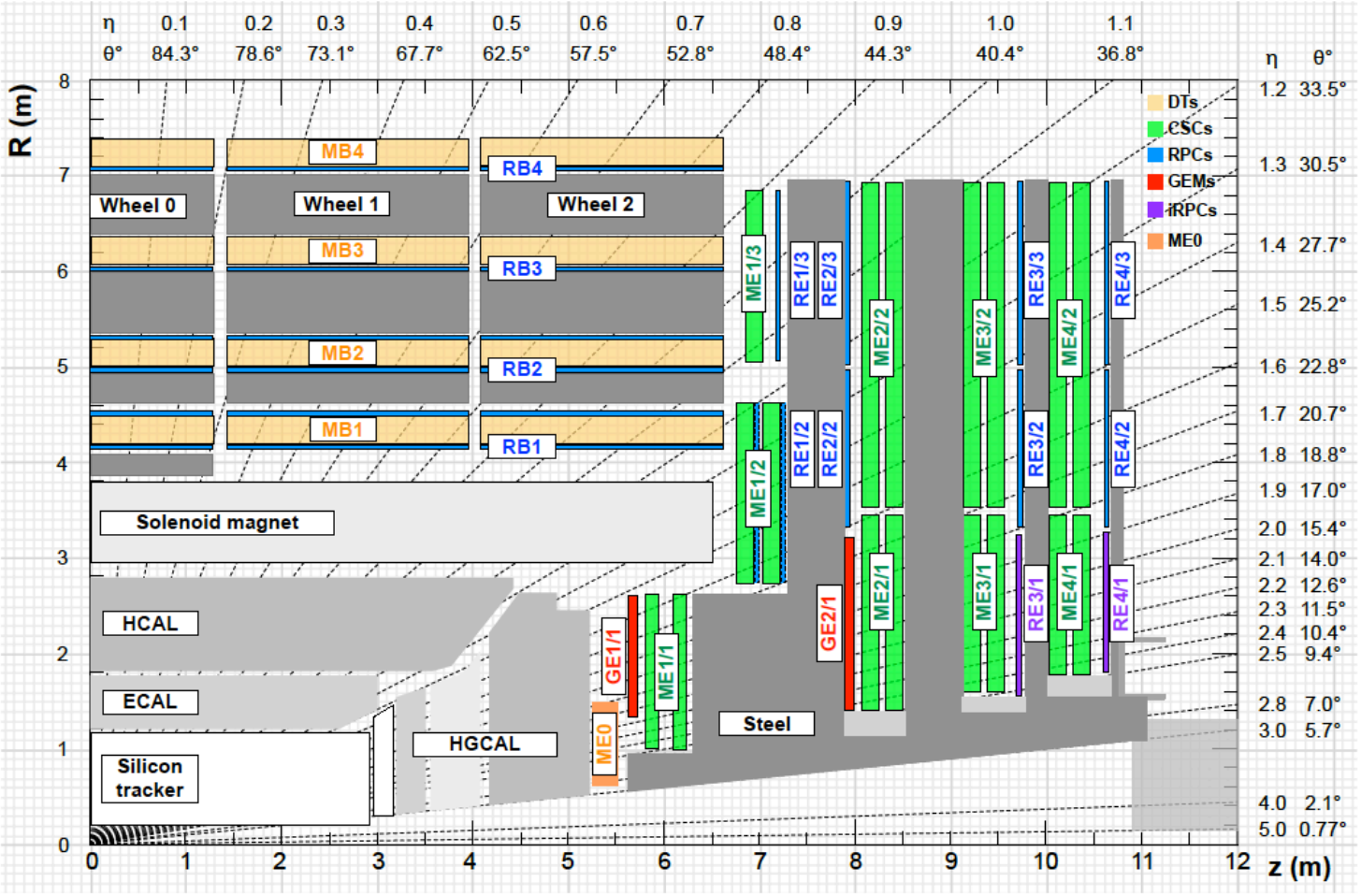
Performance:
Increased particle rates and pile-up require more selective triggering to keep the trigger efficient and the trigger rate within control.
This (in most cases) requires improved tracking for pT selection and fake trigger rejection.

New ASICs and electronics systems are required primarily for :
Higher Data Volumes,
Higher Trigger Rates,
Faster and smarter data processing to reduce/control trigger rate
Longer trigger latencies,

The CMS Muon Upgrade



The CMS Muon Upgrade



Existing Muon System composed of:

Drift Tubes (DTs)

Cathode Strip Chambers (CSCs)

RPCs.

Electronics upgrades in all systems

DT : FPGA based plus GBT(lpGBT)

No dedicated ASIC design

LS2; single sector prototype

LS3 main upgrade

CSC: upgrade for increased rate & LV1A latency.

FPGA based, no dedicated ASIC design. GBTs to be used.

LS2 on chamber electronics

LS3 off chamber electronics

RPCs : Link board replaced, FPGA based

LS3 : Possible R3/1 & R4/1 iRPC for high rate operation, using the Petiroc ASIC + GBTs

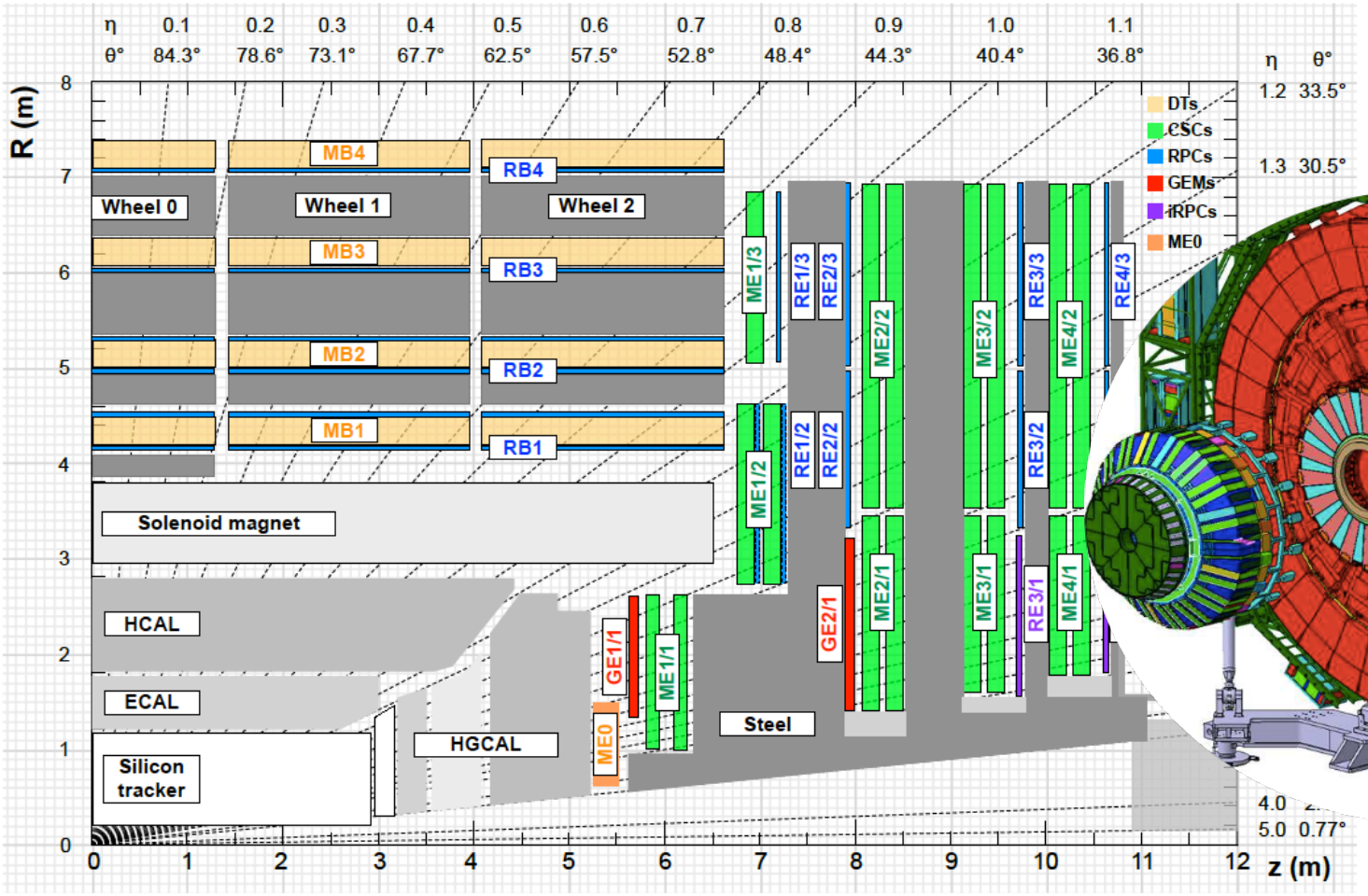
GEMs:

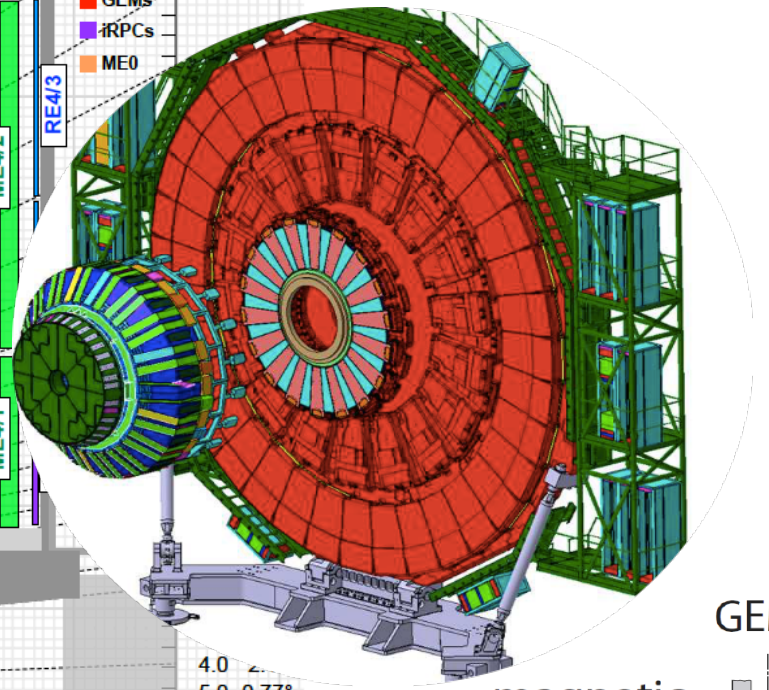
LS2 : GE1/1

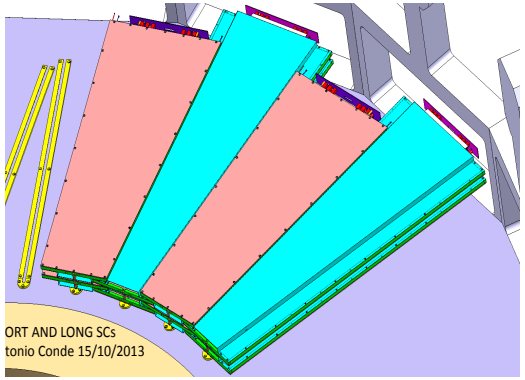
LS3 : GE2/1 & ME0

ASIC development is the VFAT3 chip

CMS GEM Upgrades GE11, GE21 & ME0

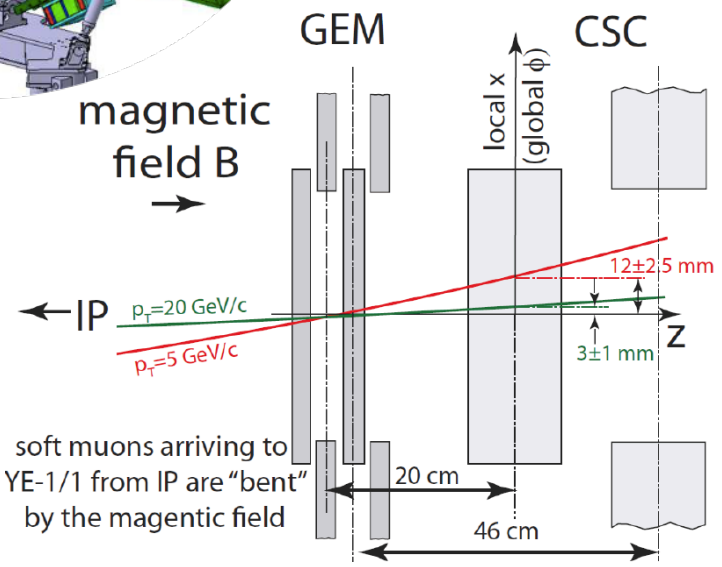




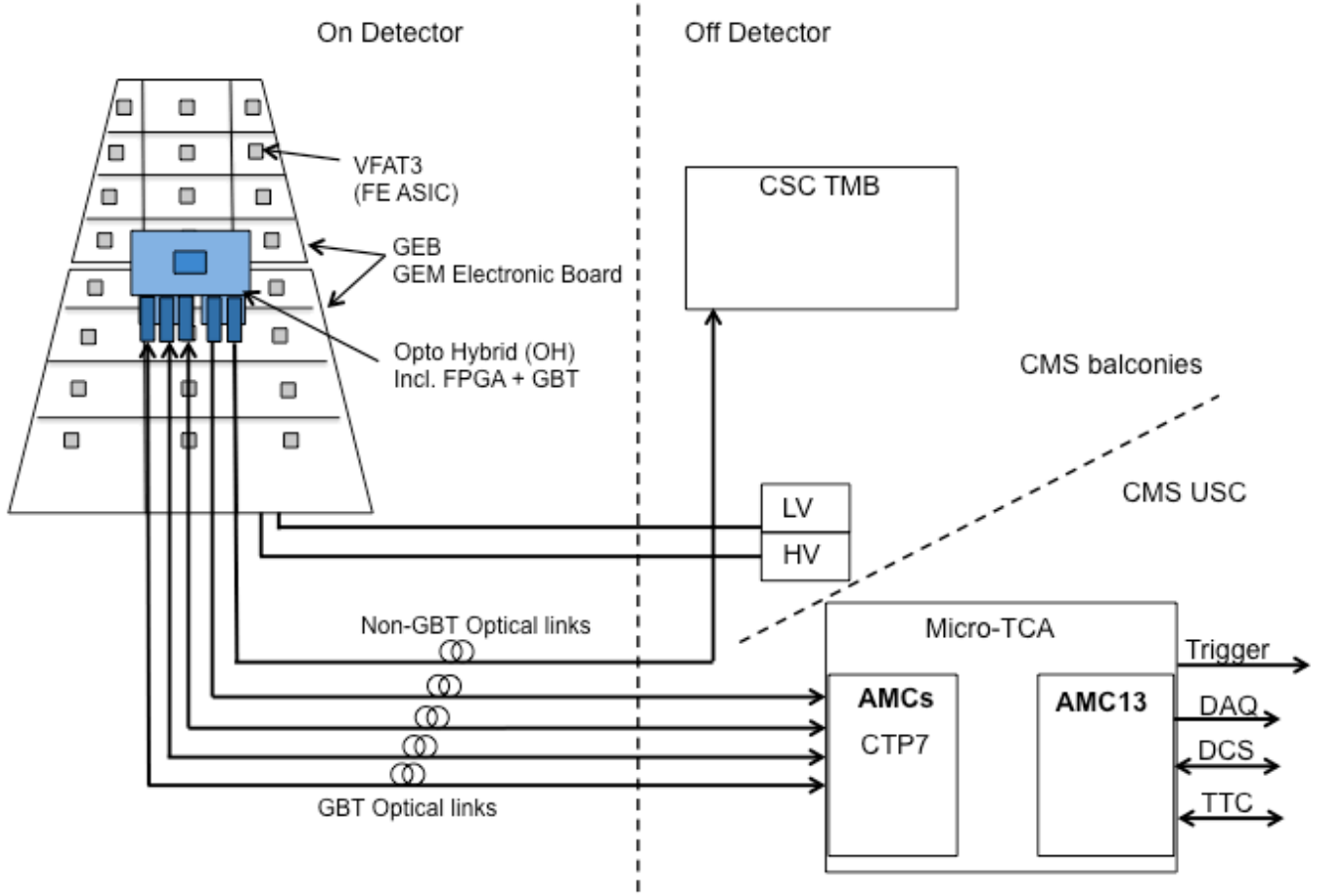


GE1/1 and GE2/1 to add redundancy and provide separation of high and low pT Muons needed for trigger efficiency at high particle rate.

ME0 : Extending eta coverage up to eta=~3 with 6 layers of GEM detectors



GEM Electronics System for GE11

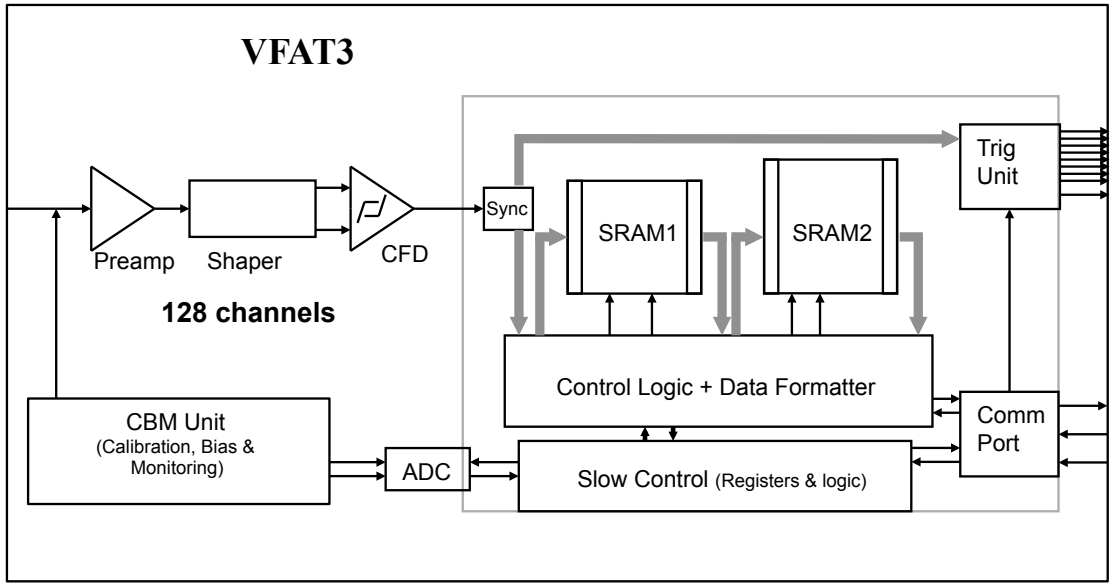


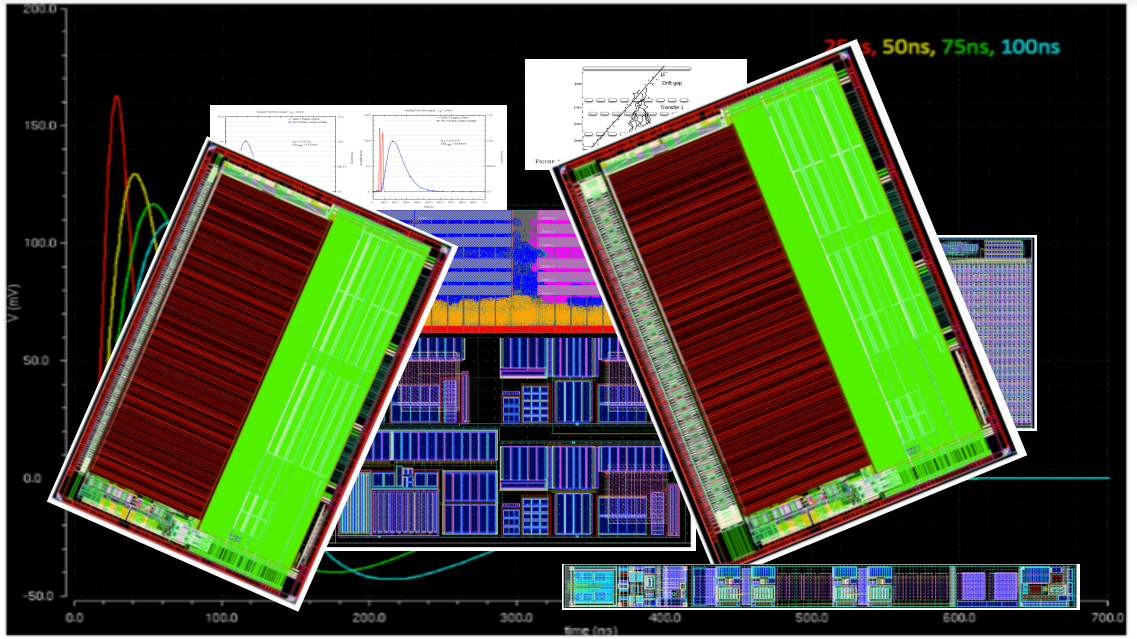
72 super-chambers, 144 chambers
24 VFAT3 / chamber
1 Opto-hybrid v3 / chamber
3GBT, 1 SCA / chamber
3 VTRx, 2 VTTx / chamber

	VFAT3	GBTx	VTRx	VTTx	SCA	CTP7
GE11	3456	432	432	288	144	12
Spares	400	50	50	30	20	1
Test setups	480	60	60	40	20	2
Total	4336	542	542	358	184	15

GE21 and ME0 will be very similar to GE11 in terms of electronics system architecture.

VFAT3





VFAT3a

VFAT3 trigger and tracking binary architecture

Designed specifically for GEM detectors in CMS Phase 2 operating conditions.

VFAT3a fabricated in 130nm CMOS in 2016 – Tested in 2017, satisfying spec.s

Approx. 15 man years of design work

Design Team :

CERN : P.Aspell, M.Dabrowski, INFN Bari: F. Loddo, G. De-Robertis, F. Licciulli, LUT: H.Petrow, AGH: M. Idzik (AGH coordination)

VFAT3b
submission July 2017

Modified design to upgrade SRAMs for radiation SEE

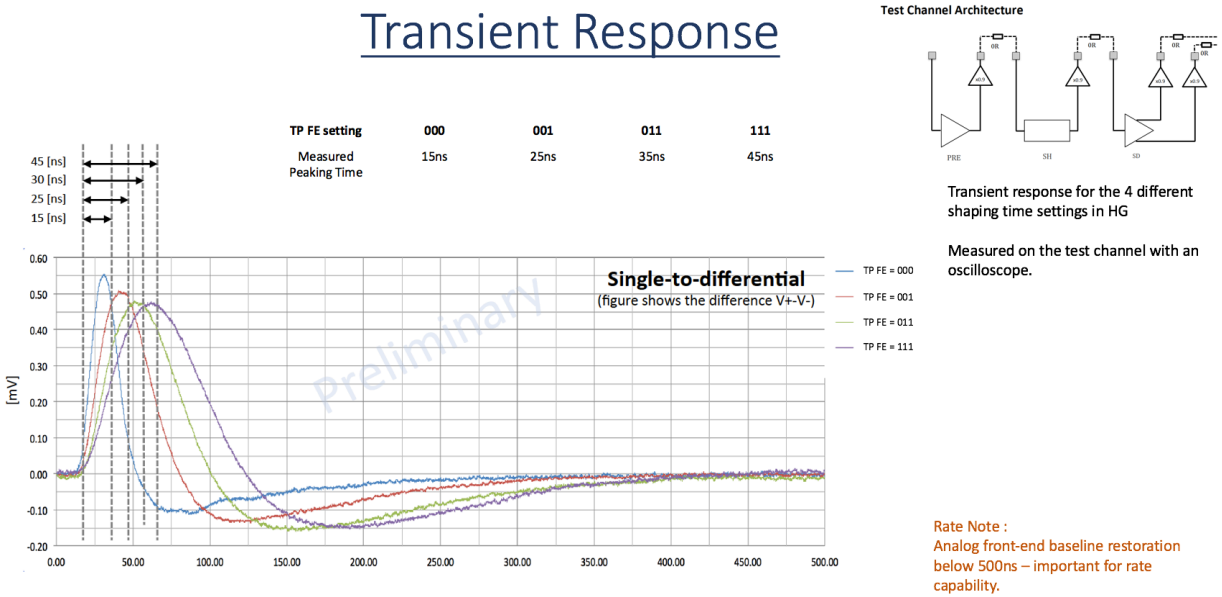
from ARM single port SRAM IP to dual port IP cells
Limit substrate/well contact spacing to 15um

Modification to CFD biasing

Production launched at same time.

VFAT3 measurements

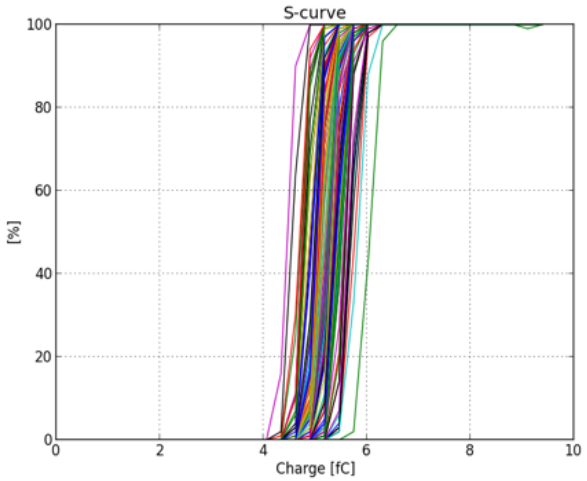
Transient Response

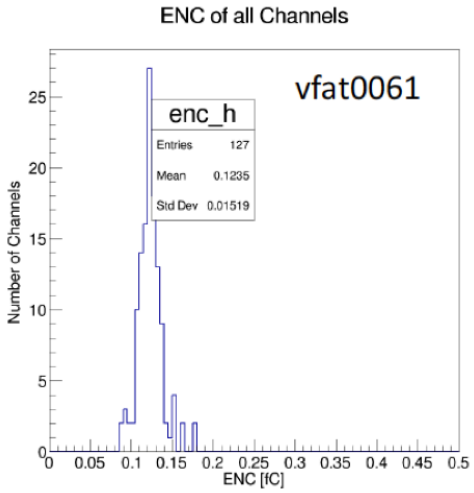


Transient response for the 4 different shaping time settings in HG

Measured on the test channel with an oscilloscope.

Rate Note :
Analog front-end baseline restoration below 500ns – important for rate capability.





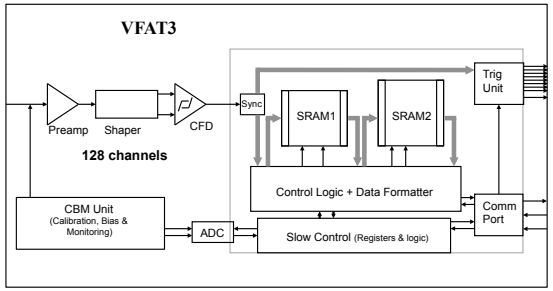
VFAT3a measured in 2017
VFAT3b measured in 2018

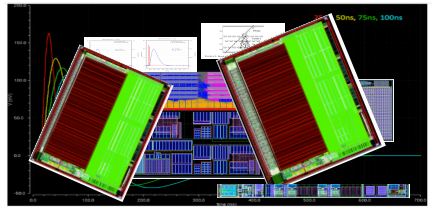
VFAT3b updates for new SRAM blocks and corrected biasing of CFD all working correctly.

Fully operational
Satisfies CMS phase 2 specifications
Suitable for GE1/1

VFAT3 Key Features & Results

Feature	Parameter	*Notes*
No of channels	128	*129 incl. test channel*
Signal charge polarity	+ & -	*Suitable for Silicon and gaseous detectors*
Programmable Gain & Shaping time	yes	*3 modes of gain* *4 modes of shaping time*
Comparator	Arming + CFD	*CFD for reducing time walk*
Rate per channel	Up to 2MHz	
Trigger Path granularity	Fast OR of 2 channels 320Mbps Full granularity, DDR 640Mbps	*8 slvs output* *Trigger-less operation with full granularity readout*
Data Path : LV1A Latency Programmability	25ns to 25.6us	*SRAM1 depth = 1024* *CMS spec.=12.5us*
Consecutive triggers	Yes	*Allows multiple time slot readout per LV1A*
Max LV1A rate	Up to 2MHz	*CMS spec = 0.75MHz*
Zero suppression	Yes	*Many options for ZS in the data packet* *Used to increase trigger rates > 2MHz*
Directly compatible with GBTx and LpGBT	Yes	*Includes HDLC addressing and adapts to slvs CM differences*
Calibration, Bias and monitoring	integrated	*Controlled via Slow Control (SC), internal ADC*
Channel Thresh. Trim	Yes	*Reduces threshold spread*
Temperature measurement	Yes	*Internal & external temperature measurement read through SC*
Radiation tolerance	Ionising SEE	*Up to 10s of Mrads,* *Triplication and SEL tolerance design*



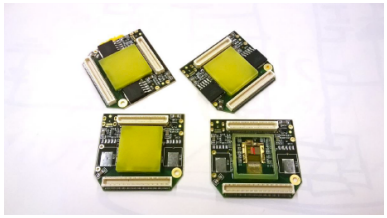


Measured Parameter	Measured Result
Peaking times (programmable)	15ns, 25ns, 36ns, 45ns
Gain/Linear range (programmable) Gain mV/fC & linear range to 10% amplitude reduction in fC	HG 48 mV/fC 9.5 fC MG 16 28 fC LG 8 55 fC
ENC	HG: 620e + 33e/pF MG: 1072e + 30e/pF
Timing walk (CFD)	< 0.4ns (signal range 3fC to 30fC)
Input capacitance range	0– 80pF
Internal temperature measurement	20 to 110 degrees
Power consumption (Vdd = 1.2V)	Sleep Mode : Analog = 74mA, Digital = 50mA Run Mode : Analog = 139mA, Digital = 67mA

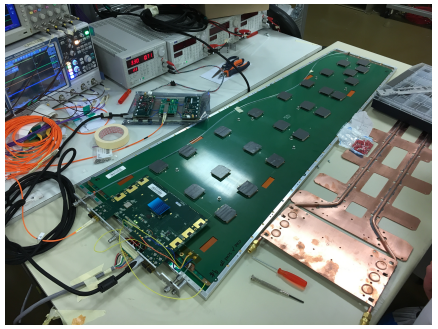
Full results to be shown in June ESE seminar

CMS GEM Electronics - Developing prototype systems

- **System V2**, for prototypes
- V2a System 2015
- V2b System 2016
- VFAT2 , GEBv2 , OHv2

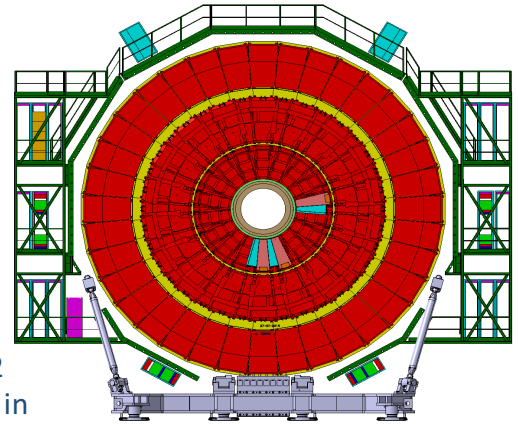


VFAT2 hybrids



V2 System Development
Cosmic stand operation

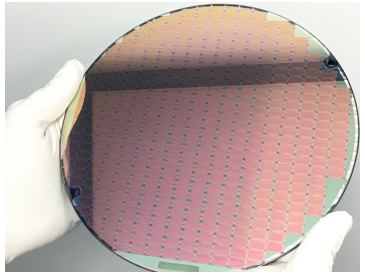
Proved GEM operation and allowed the development of an experiment level DAQ system



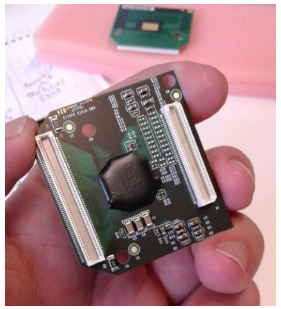
V2b Slice
Insertion of 5 V2 super-chambers in CMS

V3 Slice, V3 super-chamber inserted 1/3/2018

- **System V3**, for GE11
- V3a system 2017
- V3b system 2018
- VFAT3a/b, GEBv3 , OHv3



Wafer Processing



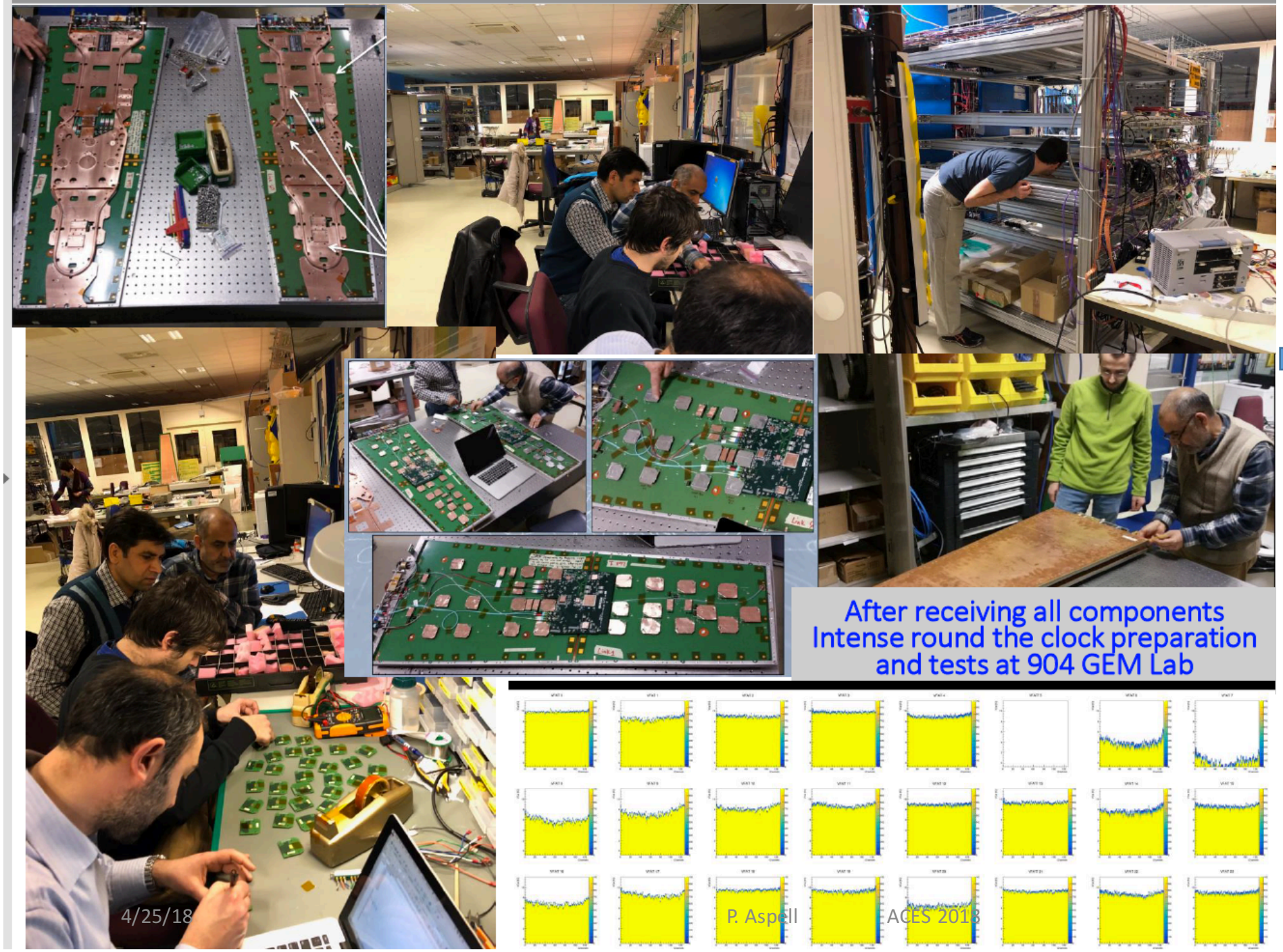
Hybrid design and development
(LUT & NCP)

V3 System Development
Cosmic stand operation

Assembled super-chamber
Ready for V3b slice installation

ESR done Jan 2018

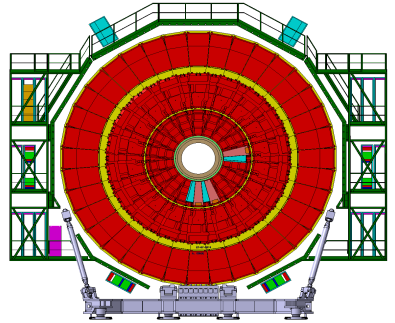
Chamber assembly with VFAT3 HV3b hybrids



After receiving all components
Intense round the clock preparation and tests at 904 GEM Lab

Assembled super-chamber
Ready for V3 slice installation

V3 Slice, V3 super-chamber inserted 1/3/2018



VFAT3 status

LS2:

VFAT3b production for GE11

Engineering run and GE11 production run is complete

Wafer processing (thinning and dicing), currently being done.

VFAT3 Hybrid (HV3b)

Production fabrication currently be done

Hybrid assembly (SMD mounting, chip mounting, bonding, QC)

2 companies chosen with 50 % of the production each

Pilot runs of 70 pieces in each company – currently being done

Full production assembly to follow.

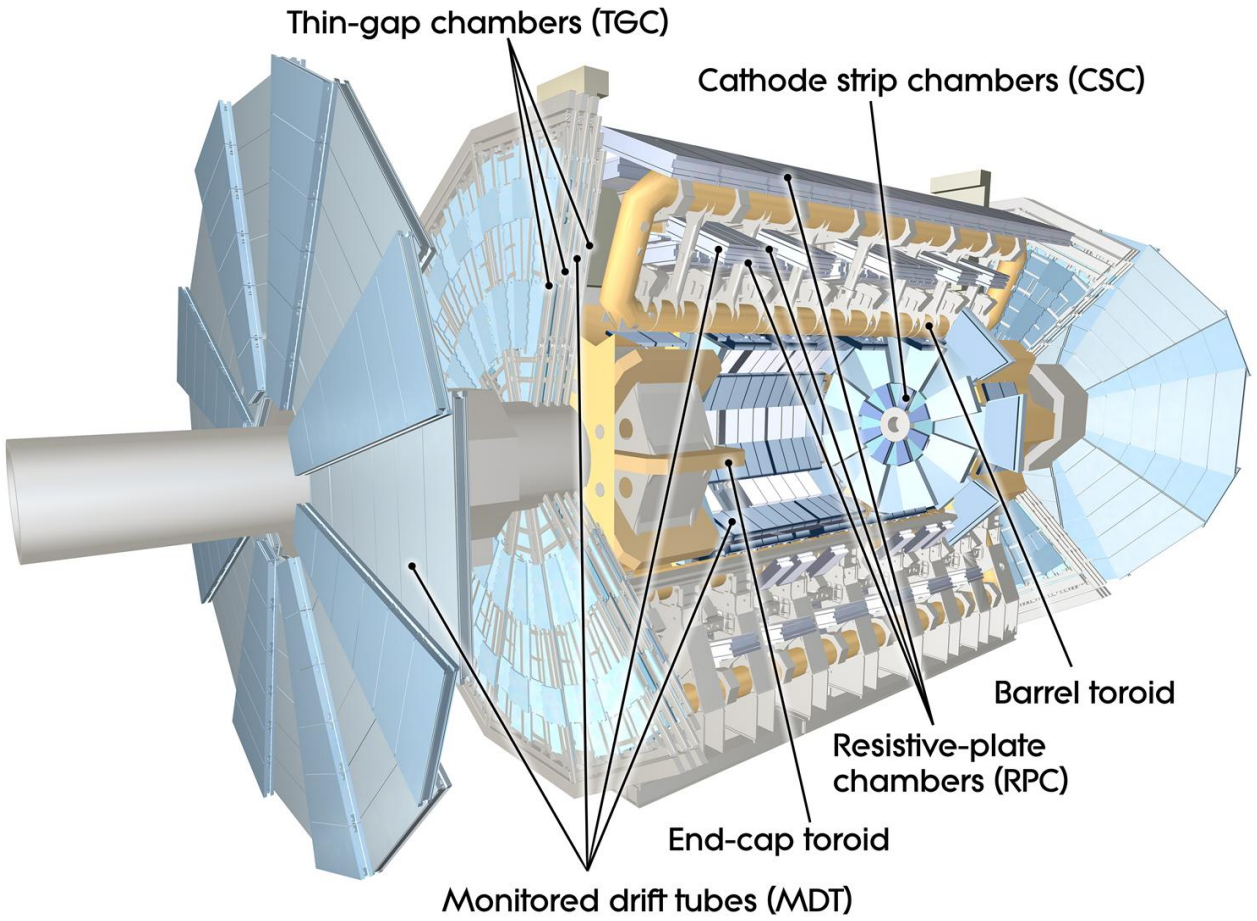
LS3:

GE21 and ME0

VFAT3 will be packaged – tendering currently ongoing

VFAT3c ? – VFAT3b could be used for GE21 and ME0 however a modification to the front-end to optimise for the higher detector capacitance of GE21 is desirable, depends mostly on designer availability.

The Atlas Muon Upgrade



ASIC development in the NSW & MDTs

The new Small Wheel (nSW)

To improve rejection of fake triggers ie rejecting candidates not pointing to the interaction vertex.

MDTs

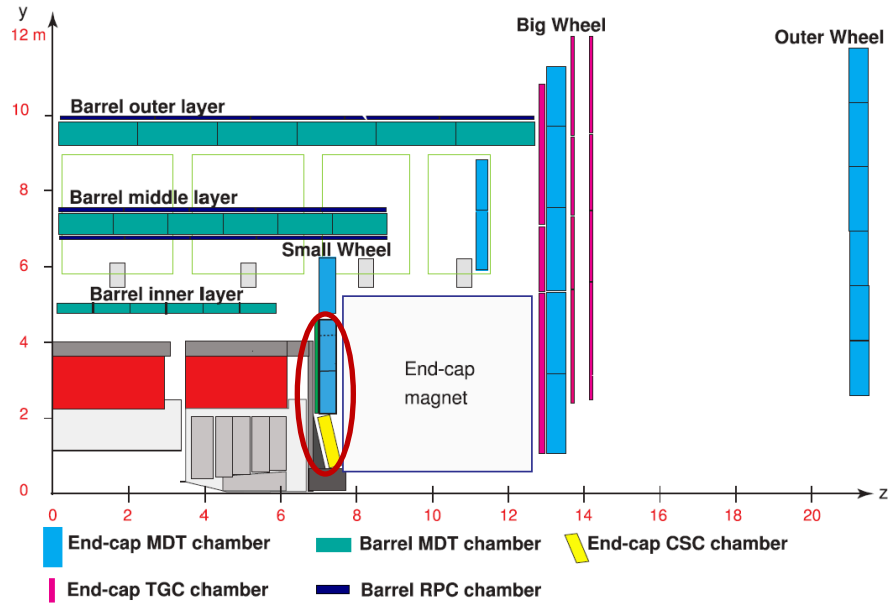
Precision tracking in phase 1.

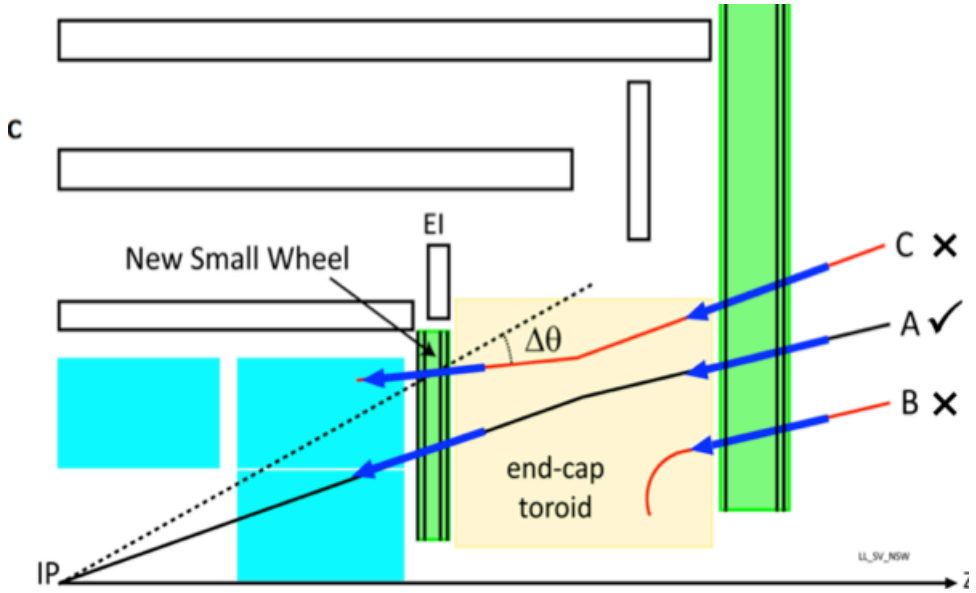
MDTs integrated into the trigger during Phase 2 to help pT selection.

Upgrades required to operate at high rate and with increased trigger latencies.

The New Small Wheel (NSW)

- Precision tracking chambers: MDT for $|\eta|<2.5$, CSC for $2.5<|\eta|<2.7$ in SW
- Trigger chambers: RPC in the barrel, TGC in the endcap



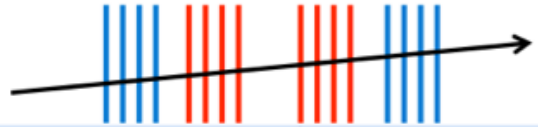


NSW: Rejection of "fake" triggers not pointing to the interaction vertex.

In LS2, the NSW wheel will replace existing small wheel in the endcap Muon system

The NSW will have Micromega and small strip TGC (sTGC) detectors

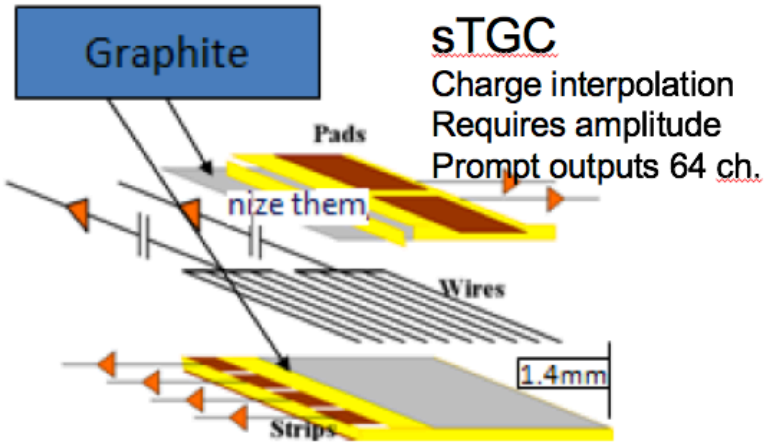
- 2 technologies, **MicroMegas** and **sTGC**

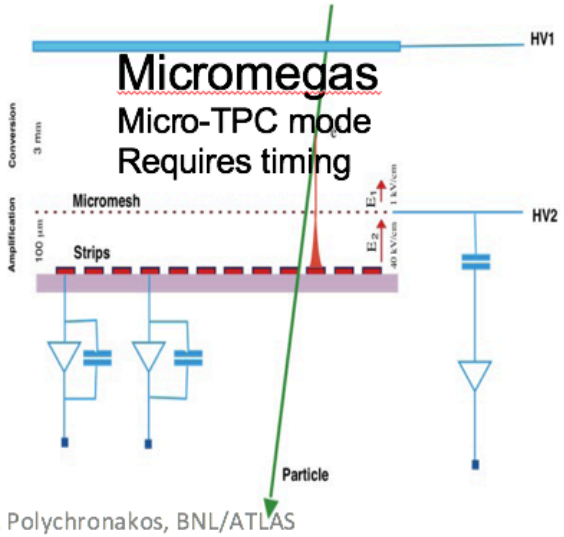


Sources : R.Richter, L.Levinson, J Zhu, S.Zimmermann

Front End for both New Small Wheel Technologies

- Both Detectors participate in the trigger, as well as providing precision measurements following a Level1 trigger
- Imposes severe demands throughout the project and in particular on the Front End
- Provides charge and time measurements as well as Trigger Primitives for both
- This let to the design of a multifunction System on Chip (SOC)
  - Four independent Data Paths
  - 3 ADC/channel, 192 total per chip
  - One of the most complex ASIC designed for an HEP experiment





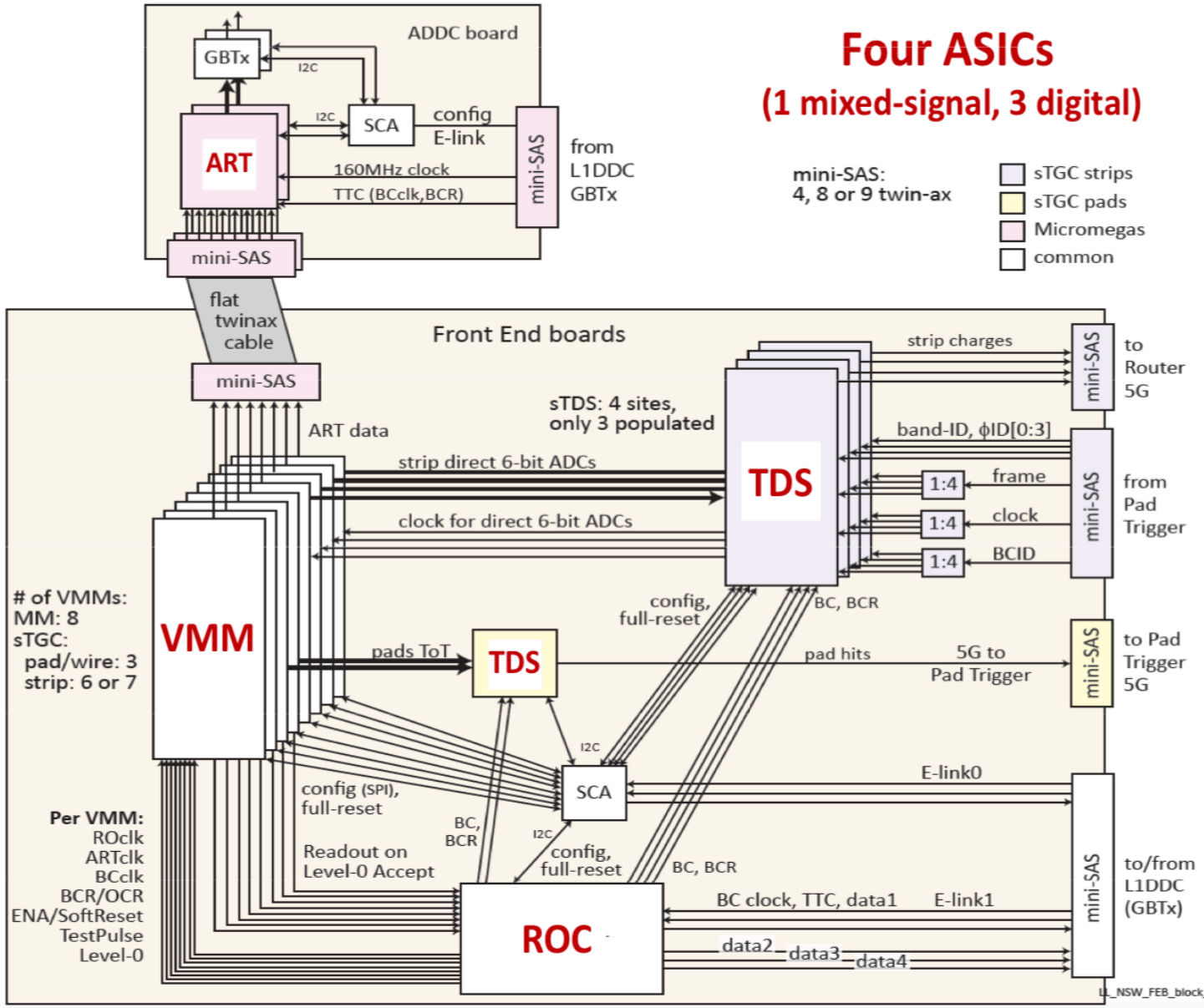
V. Polychronakos, BNL/ATLAS

Very large signal range

MM signal charge = 60-70 fC spread over 4-5 strips

sTGC charge of several pC

NSW Front-End Electronics Architecture



Same front-end chip for MM and sTGC

Custom ASIC Developments :

- **VMM** – 64ch front-end chip for sTGC and MM.

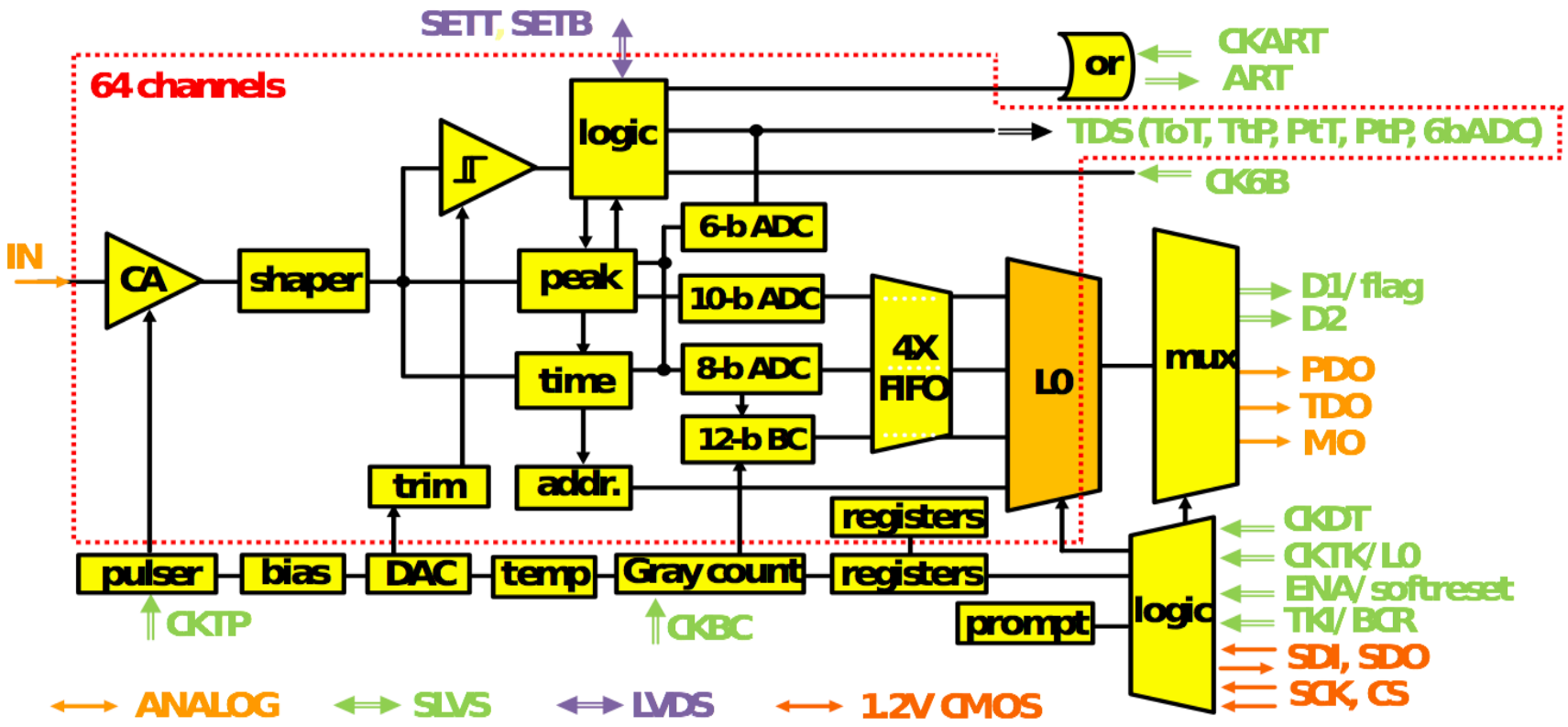
1st channel "hit" /bx, address sent to the **ART (**Address in Real Time).

Amplitude sent to **TDS**

Addr, ampl., and time tag sent to **ROC**

- **ART** – Concentrator of 32 VMM "hit" addresses, forms data packet for GBT.
- **TDS** – Trigger Data Serialiser. Collects pulse height information from VMM.
- **ROC**– L0 readout + e-link interface to GBT.

VMM3 Architecture



Integrates Full ATLAS DAQ/Trigger Functionality

VMM is the common front-end ASIC for both MM and sTGC.

It provides trigger primitives, signal amplitude and time information.

Technology : 130nm GF

64 Channels

- Trigger primitives
- Amplitude peak detector
- Time to Analog converter (TAC)

3 ADCs/channel 6b, 10b & 8b,

3 output modes

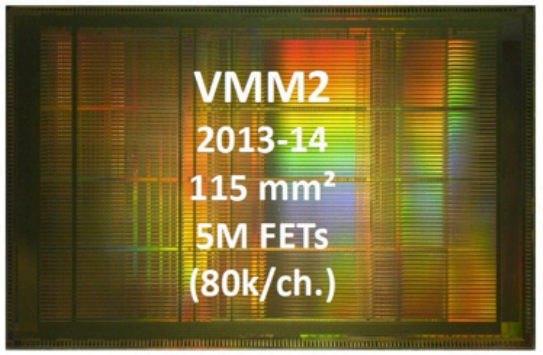
- 2 phase analog (acquisition/readout)
- Continuous mode (@ 1MHz)
- L0 mode

source V.Polychronakos
BNL

The Road to VMM3a
VMM1→VMM2→VMM3

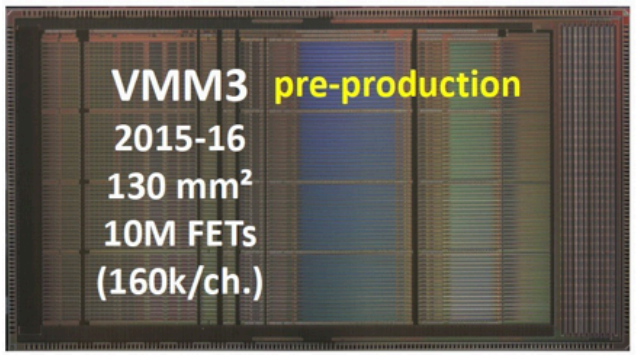
- mixed-signal
- 2-phase readout
- peak and timing
- neighboring
- sub-hysteresis
- few timing outputs

March 2012



- mixed signal
- continuous fully-digital readout
- current-output peak detector
- increased range of gains
- three ADCs per channel
- FIFOs, serialized data with DDR
- serialized ART with DDR
- additional timing modes
- 64 timing outputs
- ITAR
- additional functions and fixes

September2014



- mixed signal + digital
- continuous simultaneous readout
- SEU-tolerant logic
- deeply revised front-end for TGC (2nF, 50pC, fast recovery, ...)
- L0 handling digital core
- SLVS and new config. interface
- new reset control and fast reset
- timing at threshold
- timing ramp optimization
- pulser range extension
- ART synchronization
- 32-channel skip
- additional functions and fixes

July 2016

VMM3a includes ONLY fixes, improvements

VMM3a
Submitted 9/17
Being tested now

source V.Polychronakos

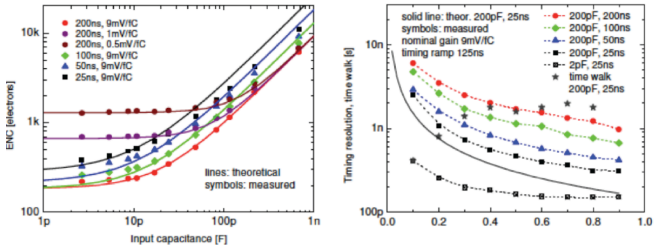
VMM

Design Parameters/Features

- Dual Polarity
- Adjustable Gain (0.5, 1.0, 3.0, 4.5, 6.0, 9.0, 18.0 mV/fC)
- Adjustable peaking Time (25, 50, 100, 200 ns)
- Address in Real Time (Fast OR in effect - Mmegas Trigger)
- Prompt (6-bit) Amplitude of all 64 channels, Time-over-threshold, time-to-peak selection (sTGC Trigger)
- Peak Detector, Time Detector (<1 ns)
- Discriminators with sub-hysteresis
- Neighbor enable logic (channel to channel and across ICs)
- Sparse readout with smart token passing,
- 10-bit DAC global threshold, 5-bit channel trim, built-in calibration pulser, channel mask, analog monitor of selected channel, temp. sensor, Band Gap Reference, LVDS digital IO

Power consumption ~ 1W

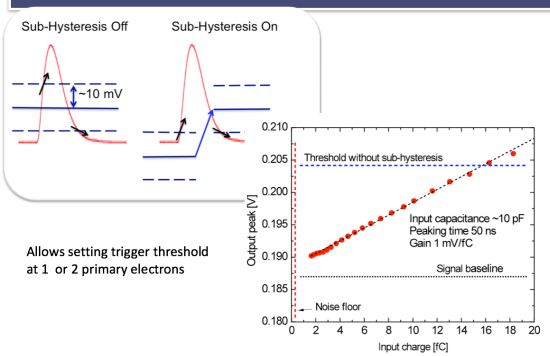
Selected performance plots



ENC as a function of input capacitance <1fC even with fast shaping (25 ns) and large input capacitance (200 pF)
Solid lines calculations, points are measurements

Time resolution as a function of amplitude ~ ns resolution and time walk

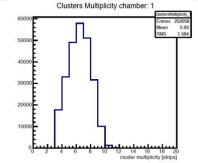
Subhysteresis allows trigger at very low Amplitudes

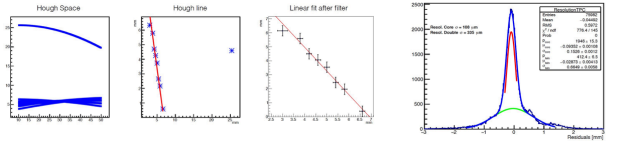


Allows setting trigger threshold at 1 or 2 primary electrons

Test Beam Spatial Resolution, Inclined Tracks

- Much more challenging
- Cluster multiplicity much higher
- Cluster can have holes due to ionization fluctuations
- Use Hough transform filter to remove hits not belonging to track (invented in 1962 by Paul Hough at Brookhaven)
- Perform linear fit including y errors (timing resolution)
- More work needed, room for improvement (e.g. timing off of threshold instead of peak, etc
- Close to NSW requirements (100 μm)





source V.Polychronakos

VMM

Status, Plans, Schedule

- GF 8RF 130 nm CMOS, 15x8.4 mm^2 die
- Packaged in 400 ball (1 mm spacing) BGA
- Received and evaluating samples of the Engineering run a month ago (4^{th} iteration)
  - Issue with 10-bit ADC differential non-linearity, effective resolution 7-8 bits adequate for both Detectors
  - No show stoppers
- 175 more wafers to be received mid-May
- Expect to issue order for the final production (350 wafers) shortly after we finish testing

40 000 chips required (mostly for micromegas, 2 million channels)

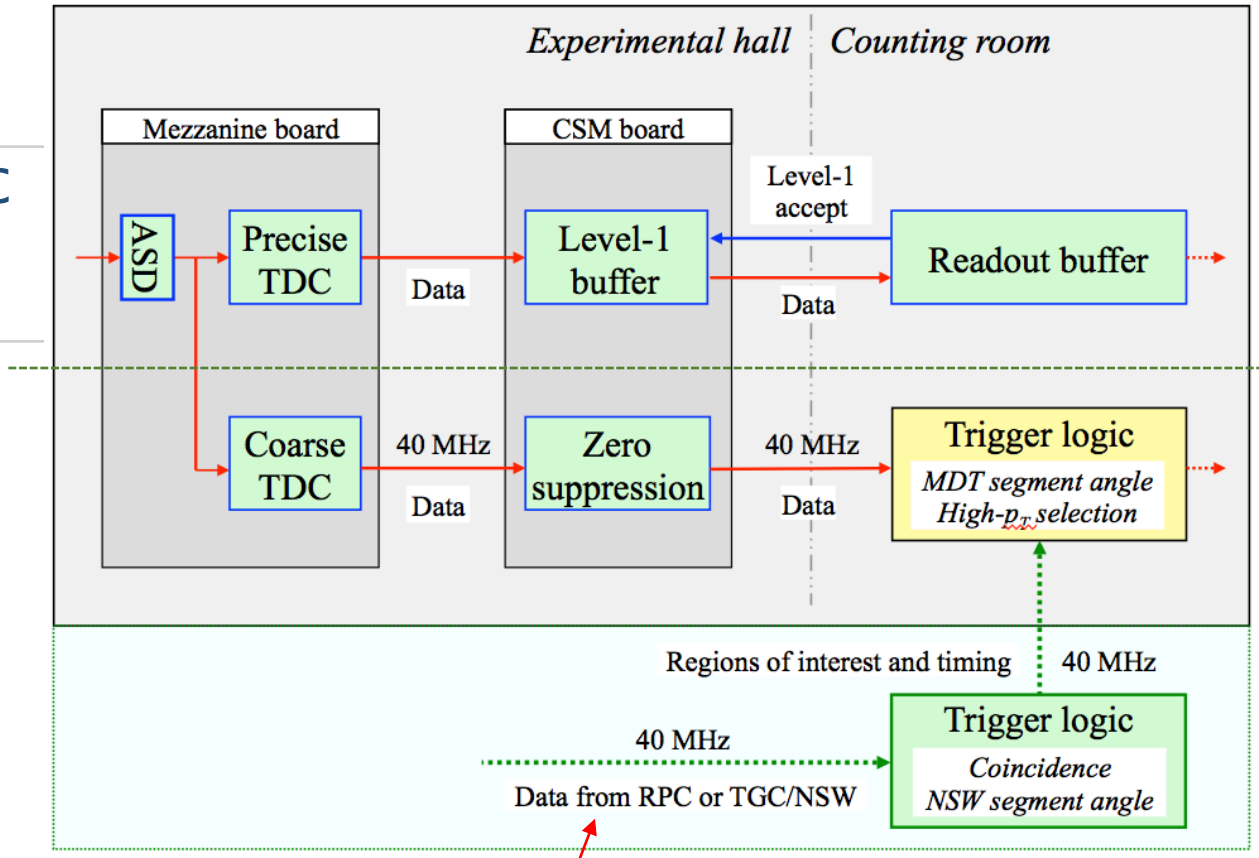
source V.Polychronakos

The ATLAS MDT Upgrade

CSM concentrator on chamber

GBT used in the tracking and control path

ASD Font end ASIC & TDC ASIC



Control & Tracking (post LV1) path

Trigger path

Region of interest from RPC/TGC trigger / bx

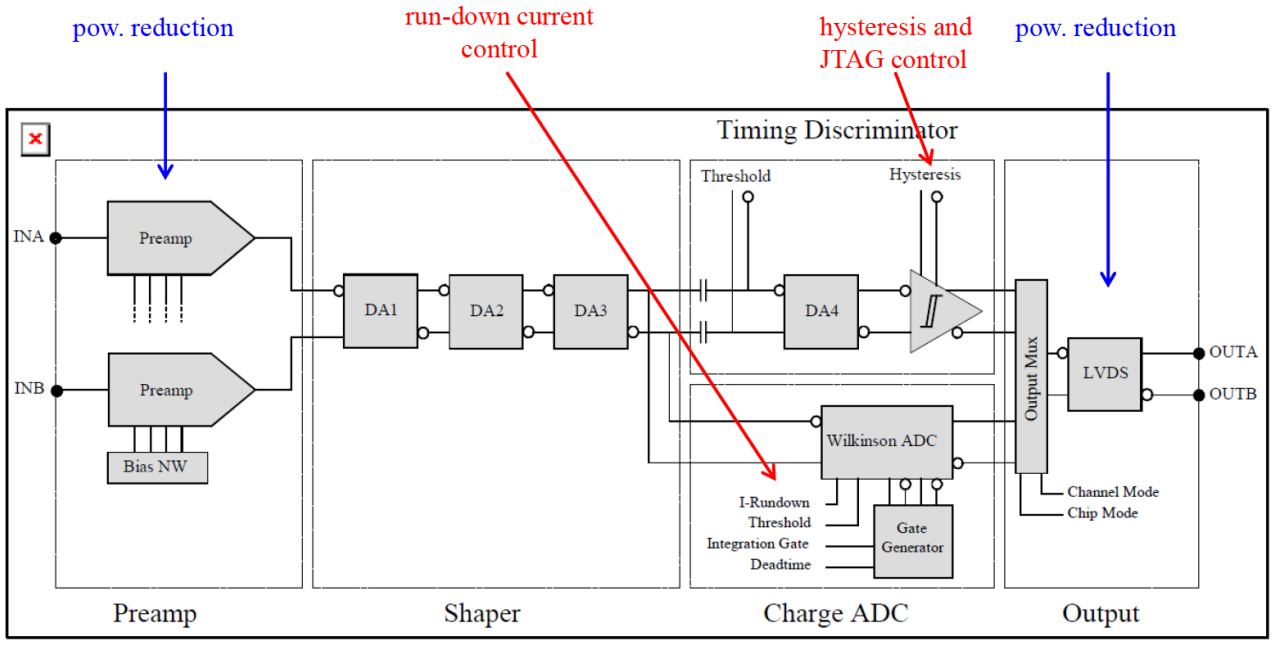
GBT not used in the triggering path due to GBT latency.

LS3

ASD ASIC

(Amplifier Shaper Discriminator)

Regions of design modifications for ASDv6



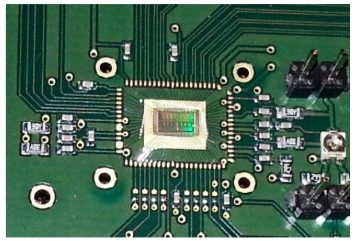
8 channel chip

Peaking time = 12ns

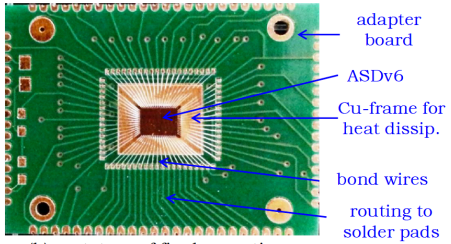
Multiplexed digital LVDS output

ADC is measuring time information

ASDv6: testing bare and packaged chips



(a)



(b) prototype of final mounting

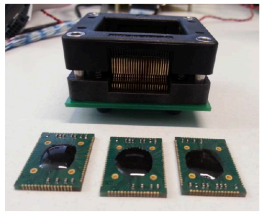
Tests in the Lab:

(a) chip directly bonded on an experimental test board

(b) chip bonded on an adapter board to be mounted on a mezzanine

(c) easy series testing w. socket, chip covered w. protective resin

All PCB layouts by Varuzhan Danielyan, MPI



(c) socket for fast testing

ASDv6_a and ASDv6_b

submitted	aug	2017
subm. alternative design:		
	nov	*2017*
received	dec	2017
first tests	jan	2018
fully analysed	april	2018
FDR	may	2018
engineering run	nov	2018
PRR	june	2019
full production	aug	2019

The ALICE Muon System

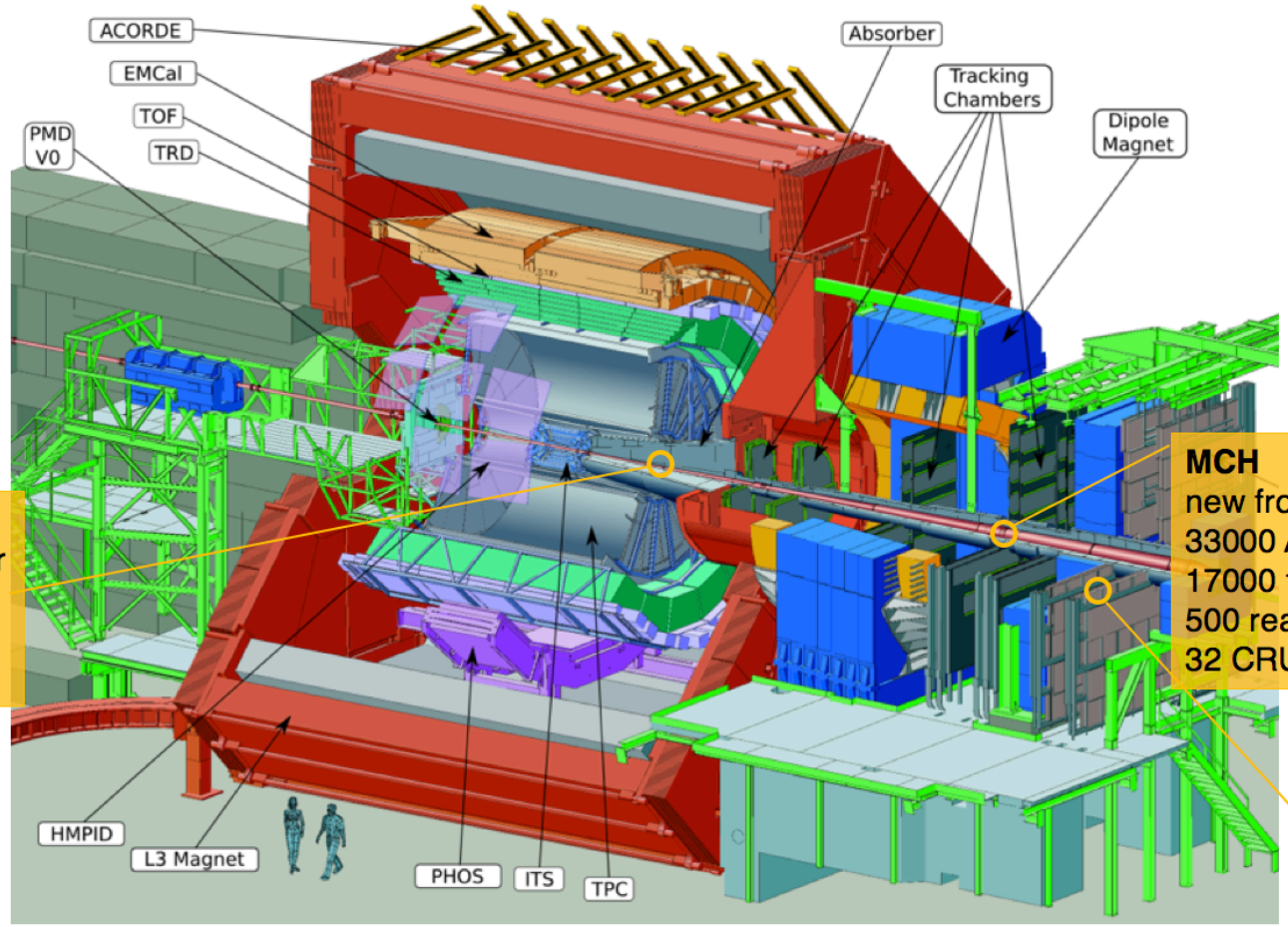
The ALICE Muon System:

Composed of 3 sub-systems :

The Muon Forward Tracker (MFT)
The Muon Chambers (MCH)
The Muon Identifier (MID)

All have ASICs

All target LS2



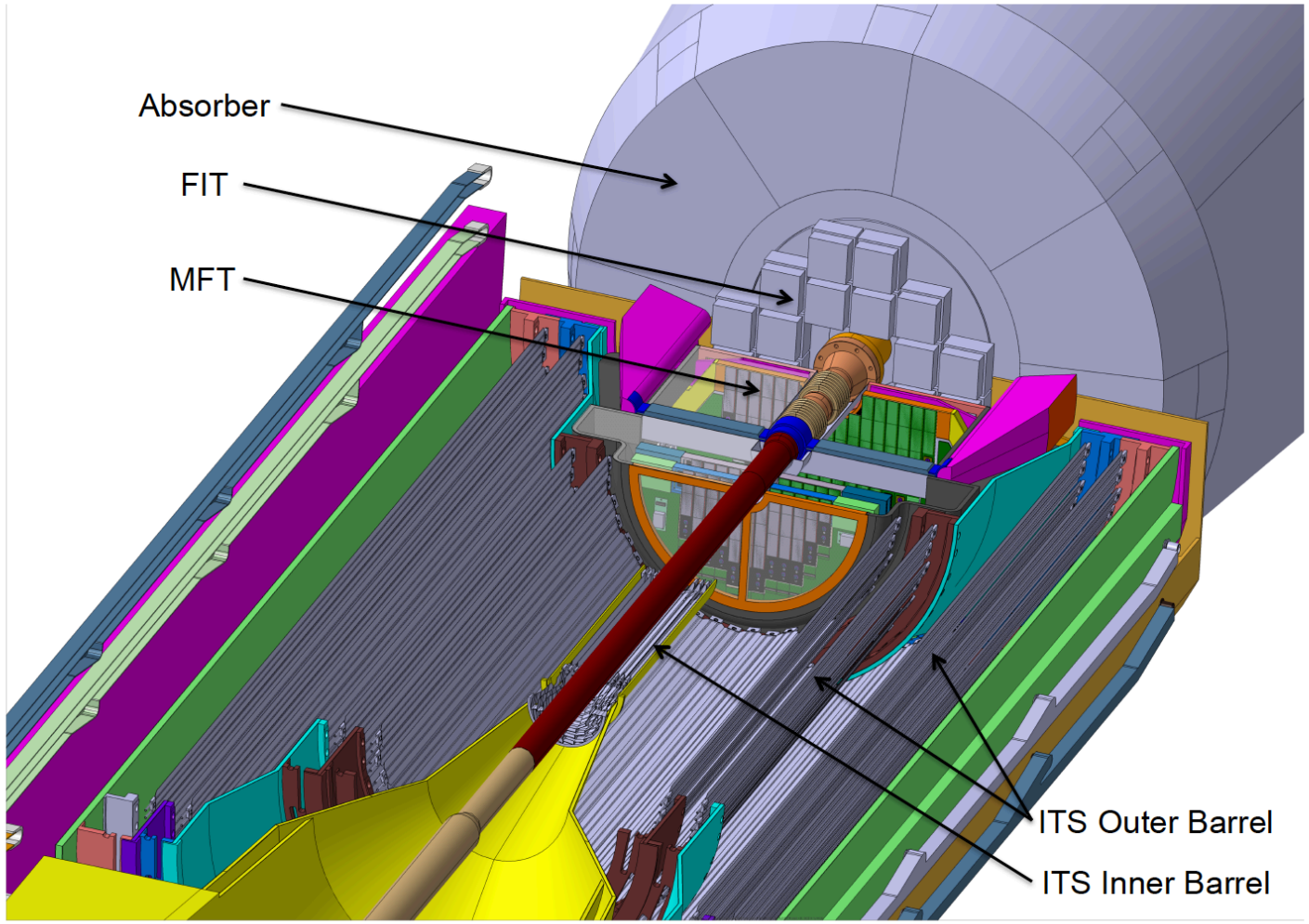
MFT
complete new detector
896 ASICs,
80 read-out cards
10 CRUs

MCH
new front-end and read-out,
33000 ASICs
17000 front-end cards,
500 read-out cards
32 CRUs

MID
new front-end,
new read-out
4000 ASICs,
234 read-out cards
2 CRUs

Ref: ESE seminar 10/4/18 - Alex Kluge

ALICE Muon Forward Tracker



MFT:

Adds vertexing capabilities.
Extends precision measurement of QGP properties to the forward region.

Several discs of monolithic silicon pixel sensors

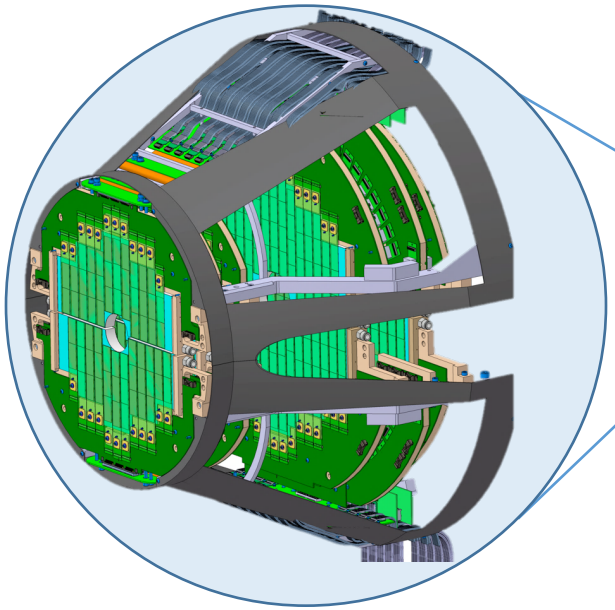
Uses the same sensor and pixel technology as the ITS.

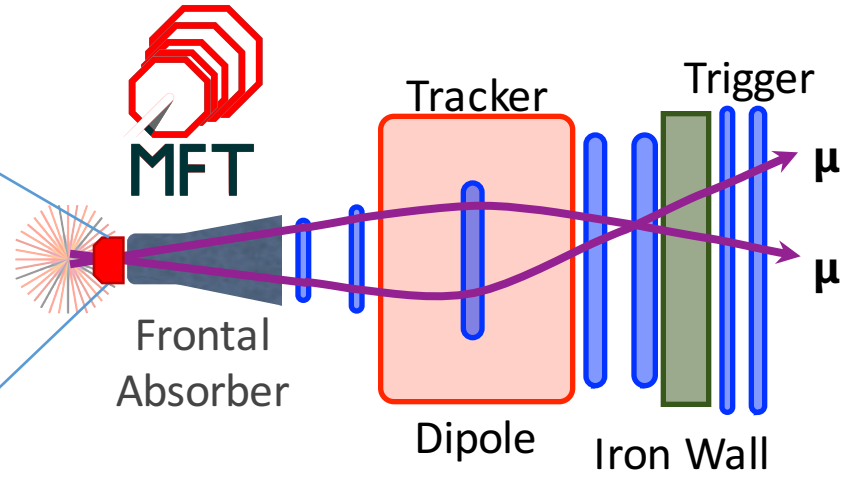
Alpide techinical detail in the ACES 2018 talk : Monolithic Pixel Developments (Thanushan Kugathasan)

ALPIDE : Monolithic Active Pixel Sensor for ALICE trackers

The Muon Forward Tracker in a nutshell

- WHAT : **Vertexing** for the Muon Spectrometer ($-3.6 < \eta < -2.45$).
- HOW : 5 lightweight disks ($0.7\%\ X_0$), 2 detection planes per disk.
- WHEN : LHC upgrade phase 1.
- CHALLENGE : 920 **silicon pixel sensors** ($0.4\ m^2$) assembled and wire-bonded on 280 aluminum flexible printed circuits (FPC).

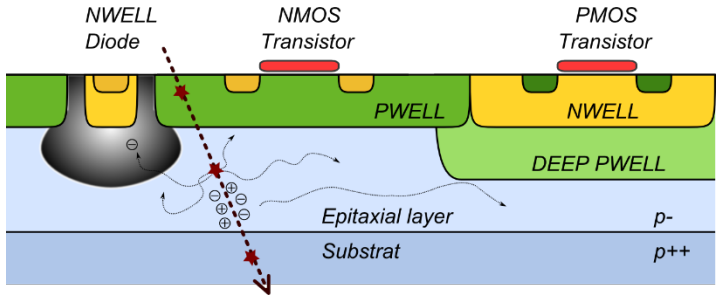




Status : 1200 wafers produced
(option up to 1400 wafers)

TowerJazz CMOS 180nm technology

- Deep P-well ➔ **Full CMOS within the pixel.**
- Thick (18µm - 30µm), high resistivity epitaxial layer (>1kΩ·cm)
- 50 µm sensor ➔ **Low material budget.**

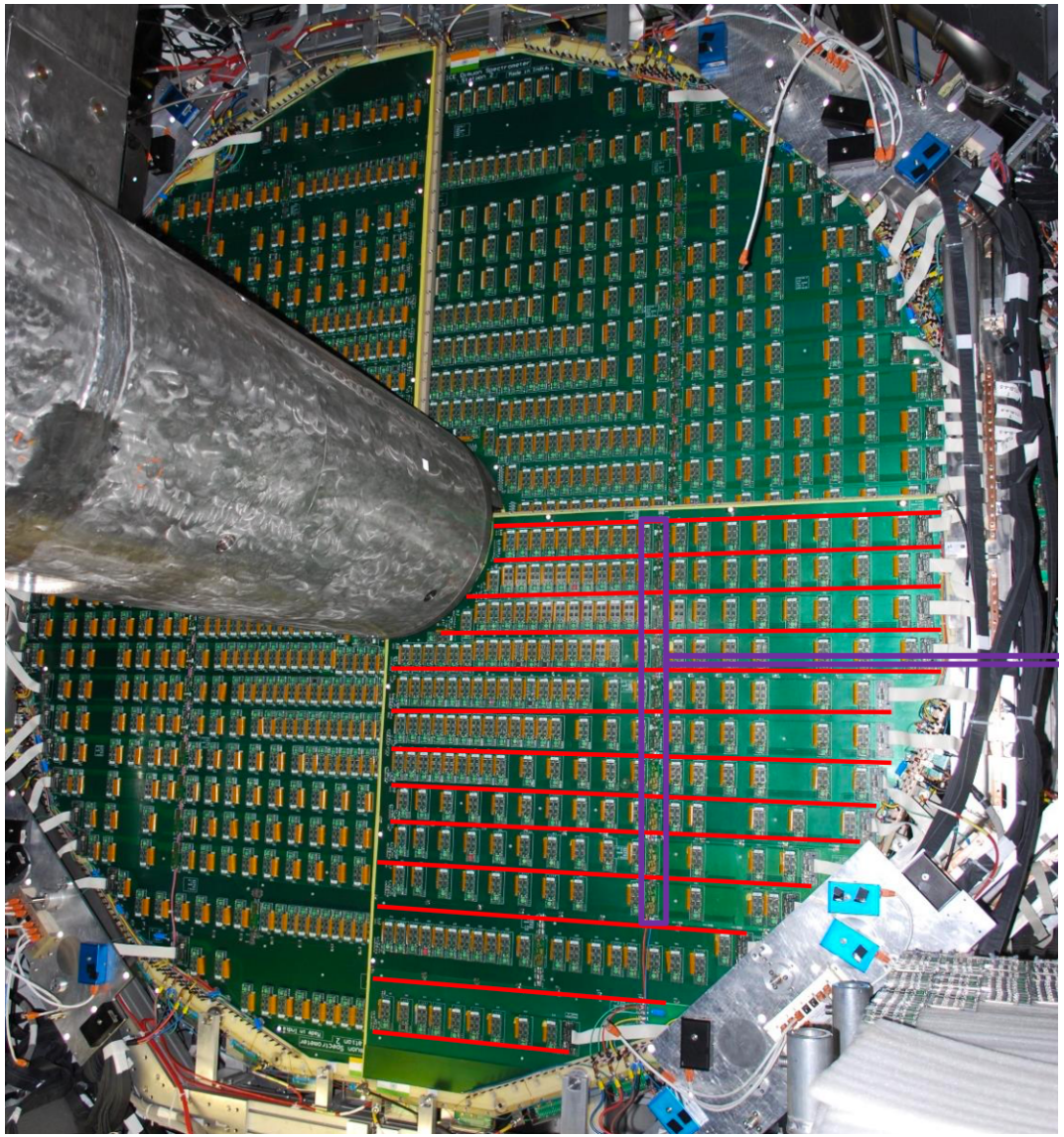


The MIP sensor : ALPIDE

- **In-Pixel signal processing** 29 x 27 µm² pitch
  - $C_{det} \approx 2$ fF ➔ **$Noise_{th} \approx 12$ e-**
  - Analog : Preamp + Discri **(40 nW)**
  - Digital : 3 memories + zero suppr.
- **Event driven** : no HIT, no power
  - Continuous or Triggered mode
- **Reticle size ASIC** : 524 kpixel, 30x15 mm^2

Source: F.Guilloux, W. Snoeys, L. Musa

ALICE Muon Chambers



MCH:

wire chambers

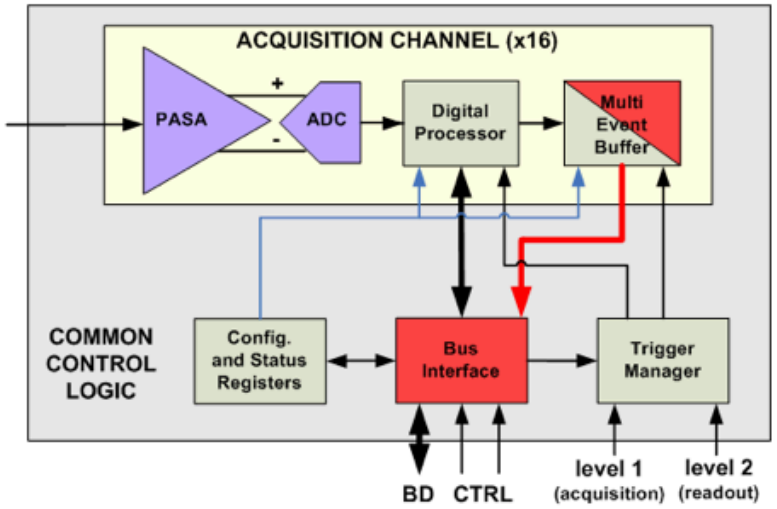
SAMPA front-end ASIC

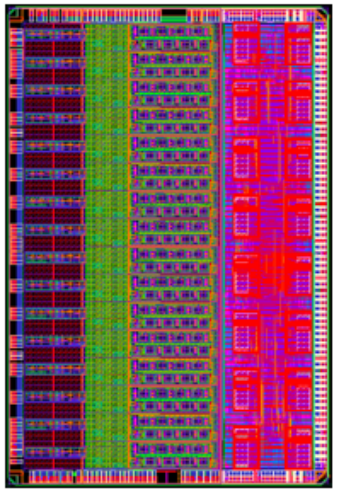
(SAMPA also used for the TPC)

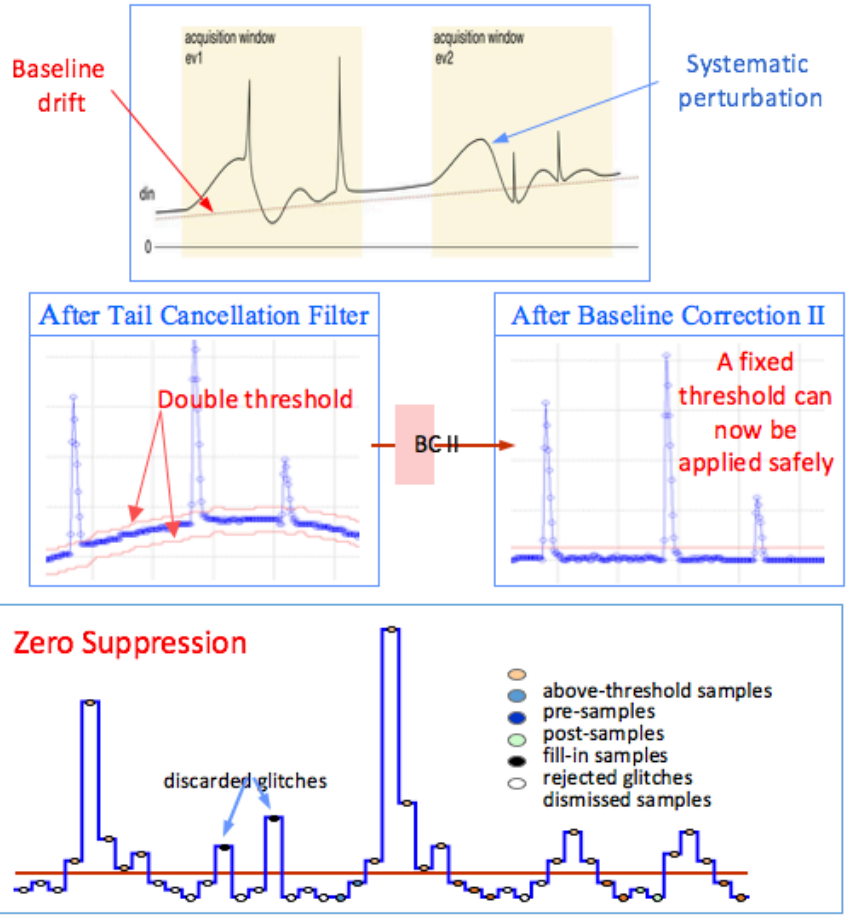
- 19000 Front-end cards
- 600 Read-out cards

Ref: ESE seminar 10/4/18 - Alex Kluge

SALTRO : 16 channel demonstrator of the Front-end + ADC + DSP per channel







Luciano Musa ..... S-Altro Specs. & Architecture
Paul Aspell ..... Coordinator of design
Designers :
Massimiliano De Gaspari ..... Front-end + ADC
Hugo França-Santos ..... ADC core
Eduardo Garcia ..... Data Processing & Control

SAMPA is an evolution of the the SALTRO architecture

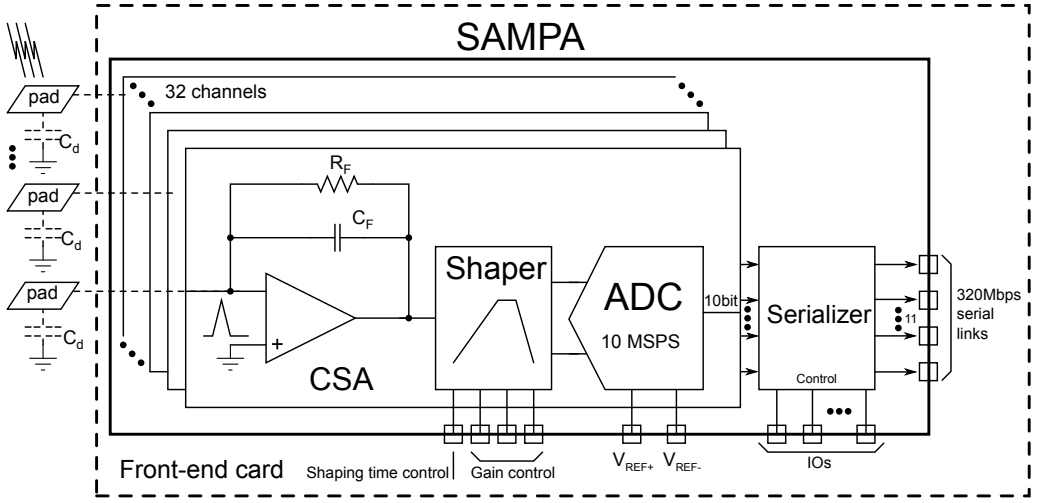
Front-end + ADC + DSP / channel

Recent advancement in ADC performance make this architecture attractive for future applications.

Digital Processor

BCF1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
TCF	Tail cancellation: Compensates the distortion of the signal shape due to undershoot.
BCF2	Baseline correction 2: Reduces low frequency baseline movements based on a moving average filter.
ZS	Zero suppression: Removes samples that fall below a programmable threshold.

SAMPA



- TSMC CMOS 130 nm, 1.25 V technology
- 32 channels, Front-end + ADC + DSP
- package size ≤ 15 x 15 mm^2
- ADC: 10-bit resolution, 20 MS/s, ENOB > 9.2
- DSP functions
  - pedestal removal, baseline shift corrections, zero-suppression
- read-out via up to 11 e-links at 320 Mbps
- Power < 32 mW/channel (Front End + ADC)

TPC Mode	MCH Mode
▪ Negative Input charge	▪ Positive input charge
▪ Sensor capacitance: 12 – 25 pF	▪ Sensor capacitance: 40–80 pF
▪ Sensitivity: 20mV/fC & 30mV/fC	▪ Sensitivity: 4mV/fC
▪ Noise: ENC ≤ 580 e^- @ 18.5pF	▪ Noise: ENC ≤ 950 e- @ 40pF 1600 e- @80pF
▪ Peaking time: ~160 ns, return to	▪ Peaking time: ~300 ns
▪ Baseline return: <500 ns	▪ Baseline return: <550 ns

- **Design in Brazil**
- **22 wafers = 5500 ASICs, Oct, 2017, 1000 ASICs successfully tested**
- **production started, March 2018**

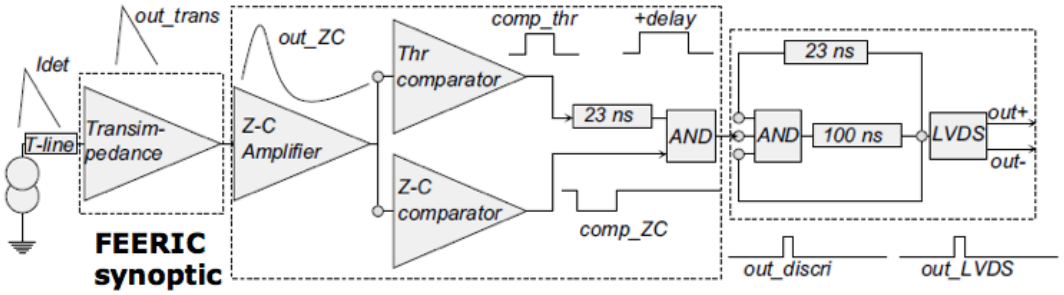
FEERIC

(Front-End Electronics Rapid Integrated Circuit)

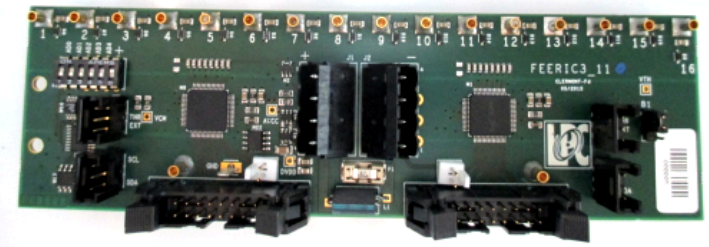
for RPC detectors of ALICE Muon IDentifier (MID)

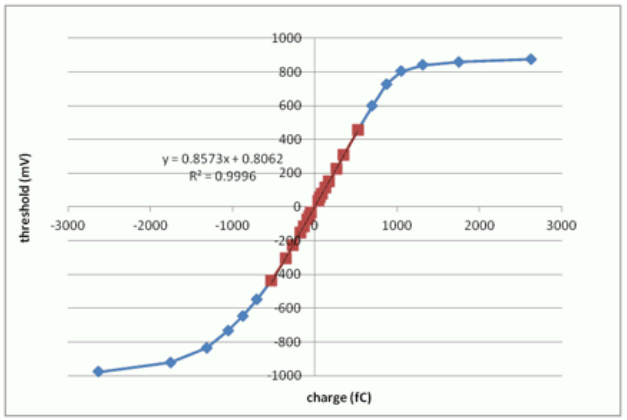
Goal: slow down MID RPC aging after LS2

- **FE with amplification**
- **total MID : 21k ch, 2624 ASICs, 2324 FE cards**

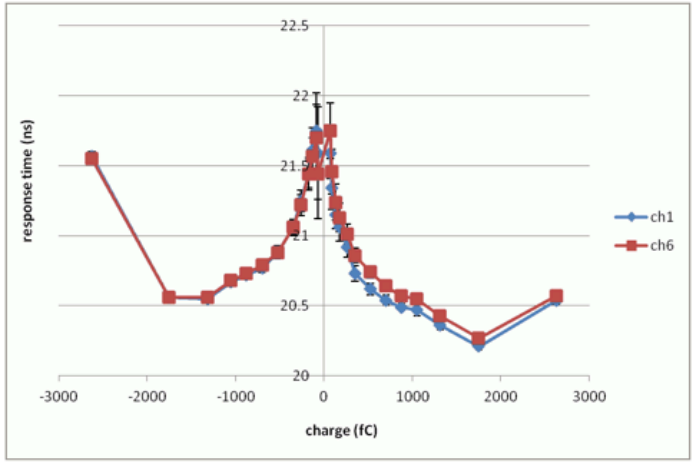


Technology	AMS CMOS 0,35 µm
Size, packaging	8 mm², TQFP 64
Channels per ASIC	8
Polarity	+/-
Linear dynamic range	Q < 1 pC
Noise (r.m.s.)	< 2 fC (simu for ASIC only)
Power dissipated	60 mW/ch
Power supply	3 V
Time jitter (r.m.s.)	50 ps for Q=200 fC (simu for ASIC only) 300 ps for Q=200 fC (ASIC on FE card)
Time walk	<1 ns for 100 fC < Q <1pC
Output format	LVDS, 23 ± 2 ns
Gain	~1 mV/fC





Gain (top) and response time (bottom) measured for ASIC on FE card



ALICE Muon Identifier

MID:

RPC Detectors

Electronics upgrade allows operating RPCs with lower gain to extend the RPC lifetime due to aging.

Uses common ALICE backend

FEERIC:

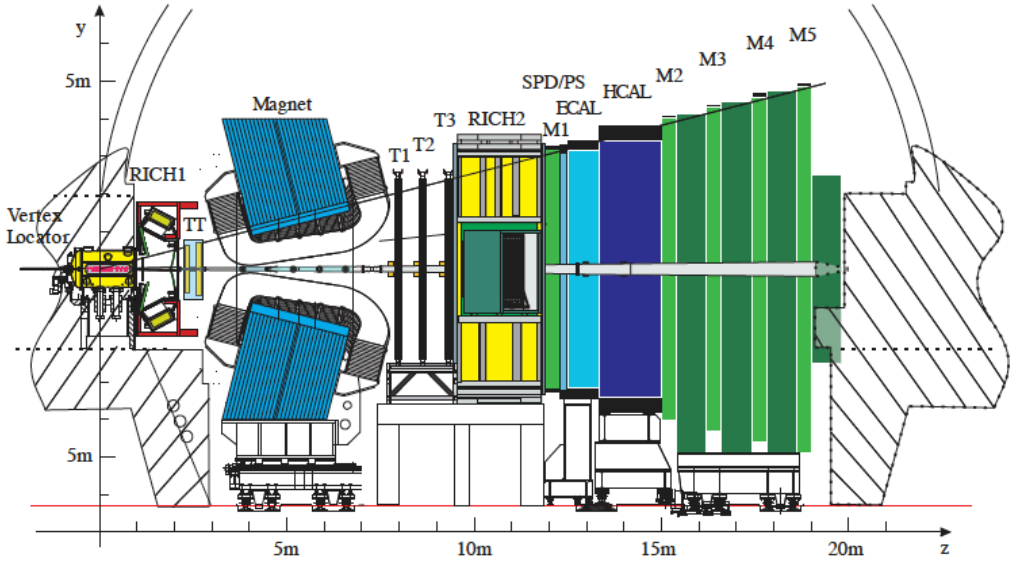
Transimpedance front-end + zero crossing discriminator + LVDS output

ASIC production of 5000 pieces done in 2015

Installation planned for LS2, 2019.

Source: Samuel Manen (IN2P3)

The LHCb Muon Upgrade



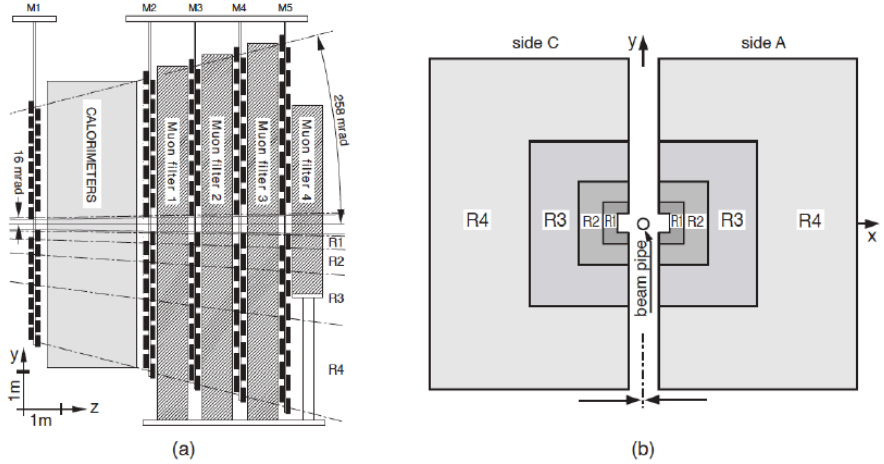


Figure 4.1: (a) Side view of the LHCb Muon Detector. (b) Station layout with the four regions R1–R4 indicated.

Existing Muon System composed of:

5 Stations M1-M5:

Each station divided into 4 regions (R1-R4)

Detectors : MWPC

GEM (R1 of M1)

20 different types of detectors, with different time response

Different dimensions: M1 (24x20cm2), M5 (151x31cm2)

Main Reason for Upgrade :

Upgrade electronics chain to process trigger information at 40MHz instead of the previous 1MHz using the GBT chip set.

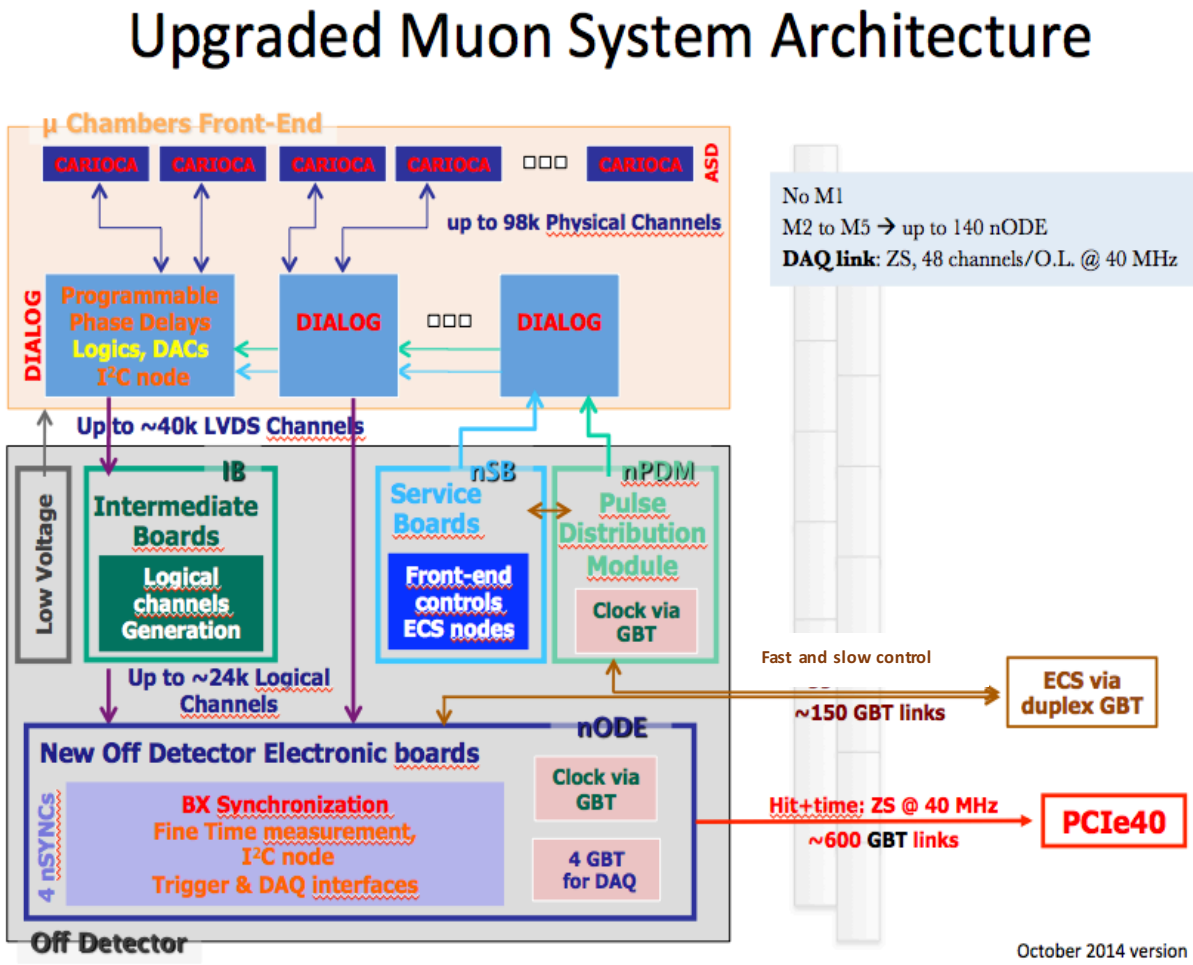
M2-M5 detectors remain

M1 to be removed.

Ref : CERN-LHCC-2013-022 ; LHCB-TDR-014

Source : A. Cardini, K. Wyllie

Upgraded Muon Readout Scheme



Cardiac front end board already there containing Carioca and Dialog ASICs.

nODE replaces old ODE.

LS2 Electronics Upgrade Goals:

Leave FEE unchanged and upgrade the rest of the readout chain to allow all data to be shipped out in real time.

Move backend to the surface.

nODE board

Receives LVDS signal from each channel

nSync :

Main upgrade ASIC design for clock synchronisation and time measurement.

Optical transmission : Via GBT chip set.

Fast and slow controls share the same bi-directional links.

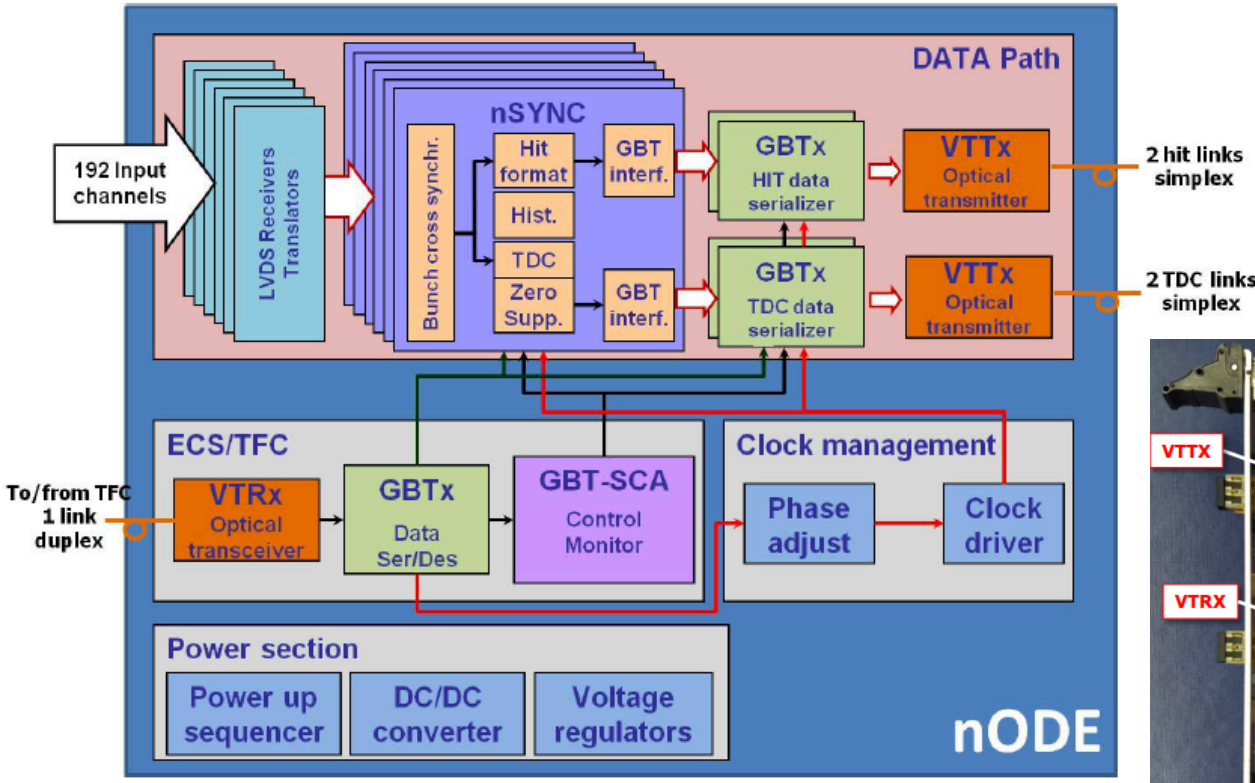
Separate links for data. No distinction anymore between trigger and tracking data.

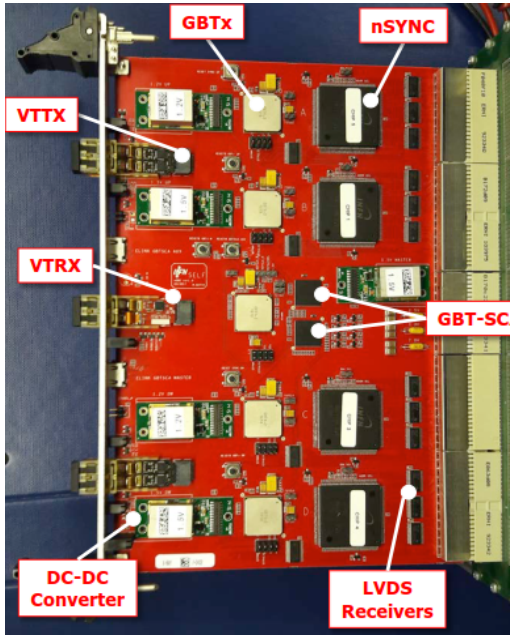
Optical links, ~ 350m @ 4.8Gbps

TELL40 boards at the surface link to PCIe

LS3: possible upgrade of FEE boards.

nSYNC



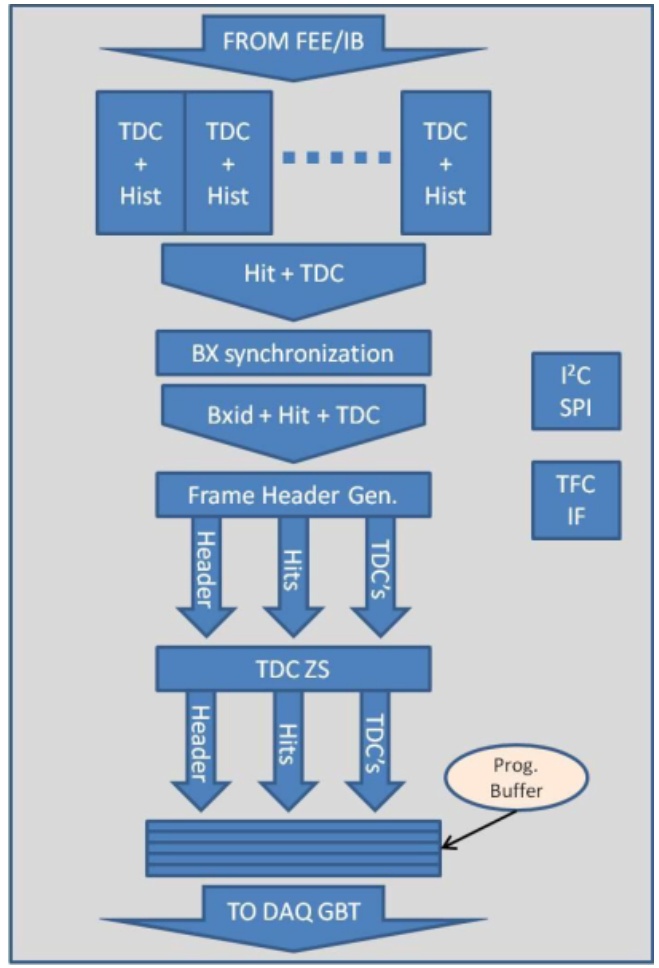


nODE to upgrade from 1MHz to 40MHz readout
Based on the nSYNC ASIC

Technology : UMC 130nm
Production underway through IMEC

LS2 installation
150 nODEs with 4 nSyncs/board

nSYNC
48 input channels
Synchronisation to 40MHz bx
TDC time measurement for sub bx time measurement
Data packet creation
Zero suppression



INFN Cagliari

Summary of the Muon ASIC developments covered in this talk

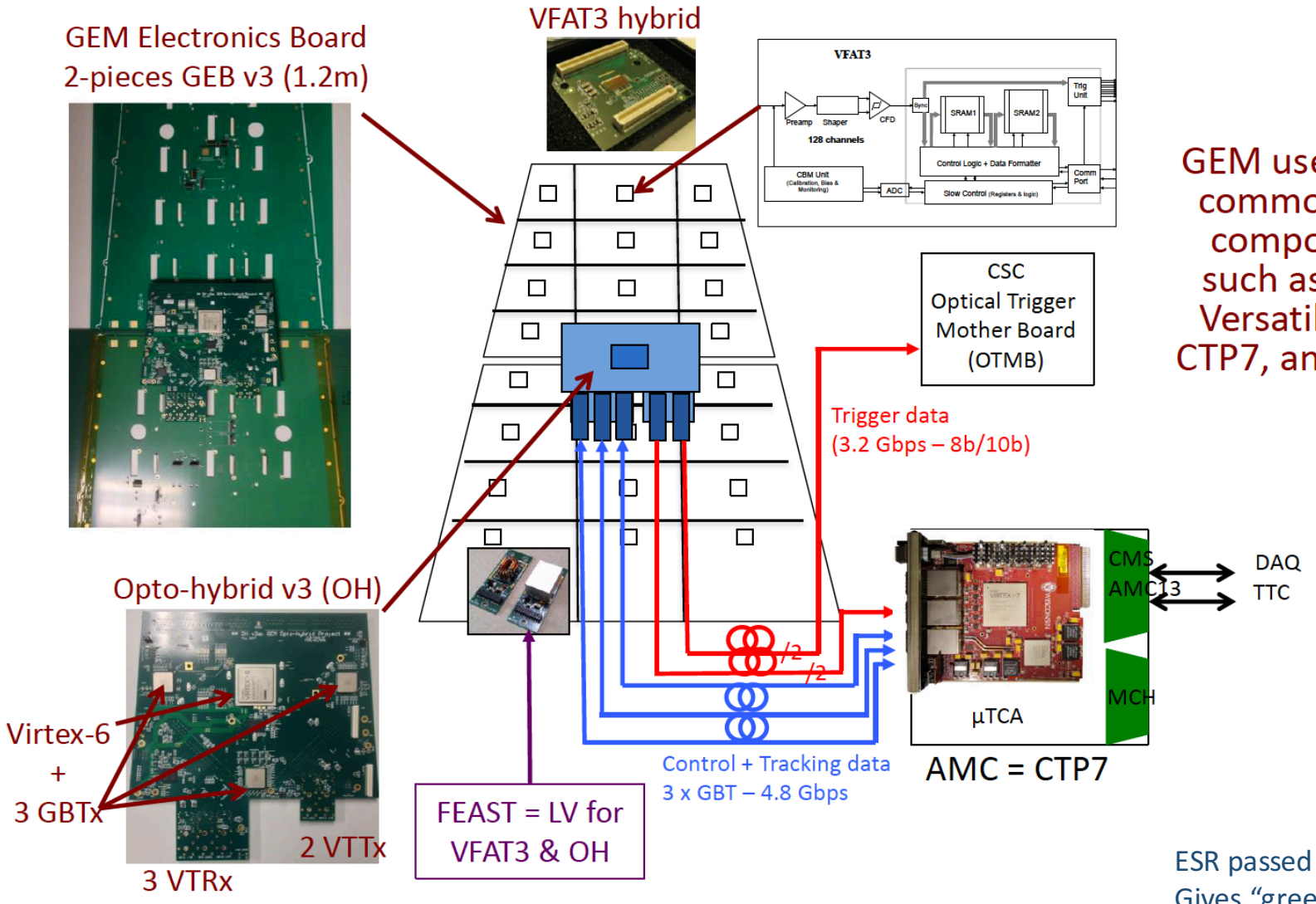
ASIC	Experiment	Muon System	Detector / Detection type	Upgrade	Function
VFAT3	CMS	GEMS	GEM	LS2: GE11 LS3: GE21, ME0	GEM front-end Tracking & Trigger
VMM	ATLAS	NSW	MM, sTGC	LS2	MM and sTGC front-end Trigger & tracking
ART, TDS, ROC	ATLAS	NSW	MM, sTGC	LS2	VMM information processors
ASD	ATLAS	MDT	DT	LS3	Front-end
TDC	ATLAS	MDT	DT	LS3	Timing of ASD output
ALPIDE	ALICE	MFT	Monolithic silicon	LS2	Vertexing - fine spatial resolution
SAMPA	ALICE	MCH	Wire chambers	LS2	Frontend + ADC + DSP
FEERIC	ALICE	RPC	RPC	LS2	Front-end + digital output
nSYNC	LHCb	MWPC/GEM	MWPC	LS2	Synchronisation, time measurement

Thanks

Additional Slides

GEM V3 Electronics System

Assembled together and working as a system, end 2017

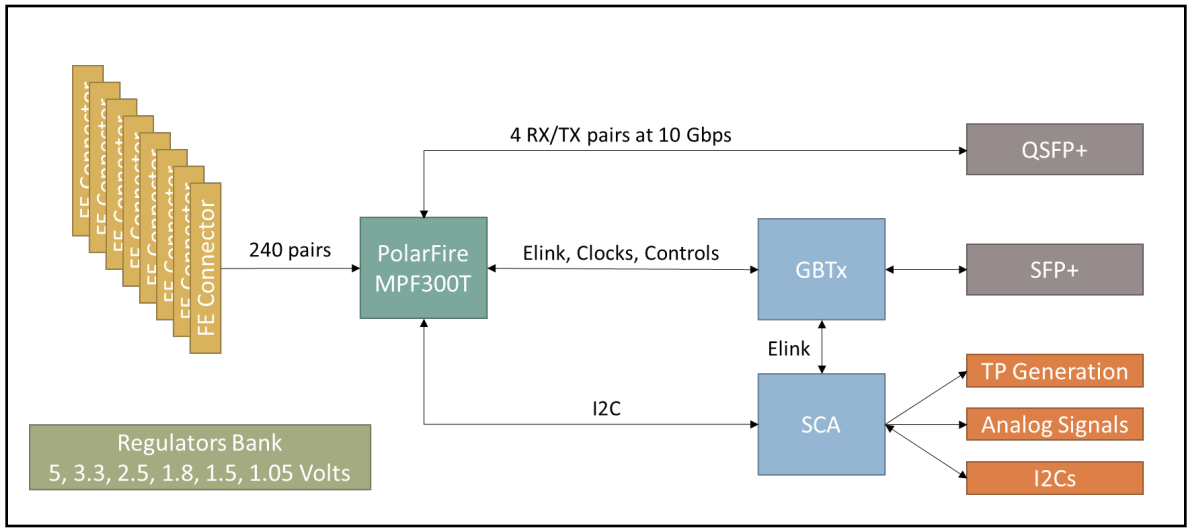


GEM uses many common CMS components such as GBTx, Versatile Link, CTP7, and FEAST

ESR passed in January 2018
Gives "green light" to start production

CMS DT

- The OBDT (On-Board electronics for Drift Tubes) module is a simple and low power board (the estimated power is half of the present)
- The fundamental part is a Flash-FPGA (Microsemi PolarFire) implementing the Time-to-Digital-Converters
- Flash based FPGA: radiation harden by construction (adopted also by HCAL)
- The integration factor can be higher than the present one (up to 240 channels/board)
- Tests show the implementation of several tens of channels with 1-ns resolution is possible
- A prototype with the not final components is going to be produced in 2018 (LpGBT, VTRx+ and FEASTUP not yet available)



- The GBT chipset is used for clock distribution and for controlling the board
- The OBDT module will perform slow control (FE access, monitoring, test pulse, RPC connection)
- Data will be sent to backend directly from the fast SERDES (10Gbps) of the FPGA
- VTRx+ optical link between UXC and USC for both data-path (x4) and primary slow control (x1)
- Redundancy in up/down stream links is foreseen

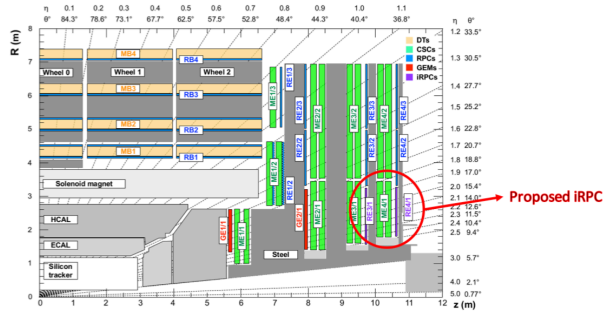
250 minicrates (one per chamber)
3-4 OBDTs per chamber
Total number of OBDTs ~ 850
1 lpGBT/OBDT therefore ~ 850 lpGBT total (GBT if lpGBT is not available)
Feast (perhaps) 7 / OBDT, therefore 0 or 6000

Source A.Trossi

PetiROC
for the CMS iRPC proposal

CMS muon upgrade at high eta

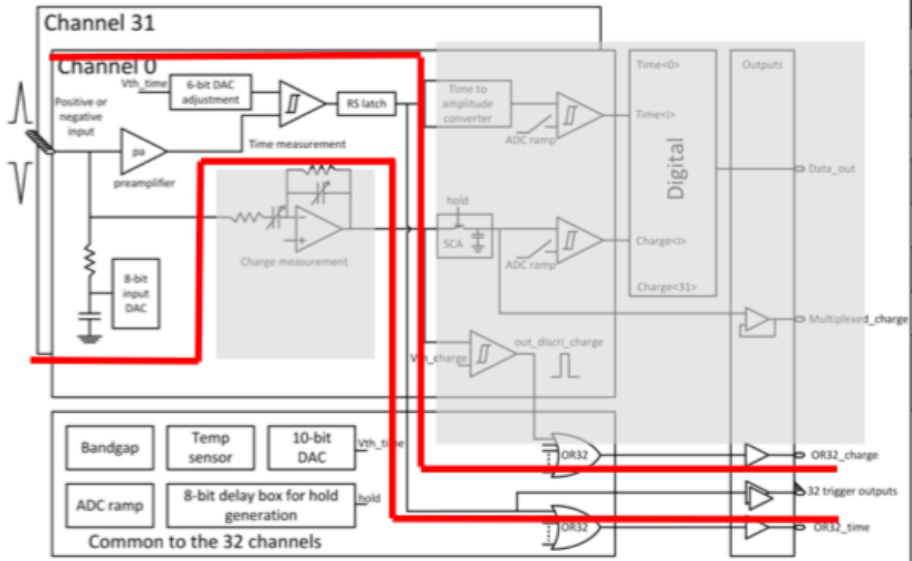
72 chambers to equip area with 1.8 < |η| < 2.4
→ Add track hits in muon reconstruction
→ Search for Heavy Stable Charge Particle

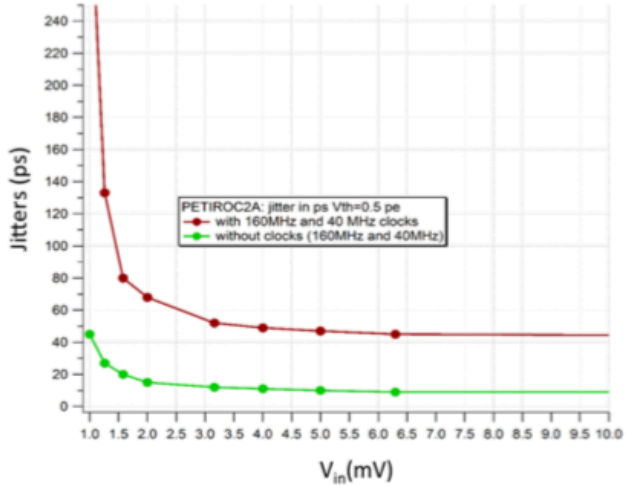


C. Combaret RPC2018 , feb 19-23rd 2018

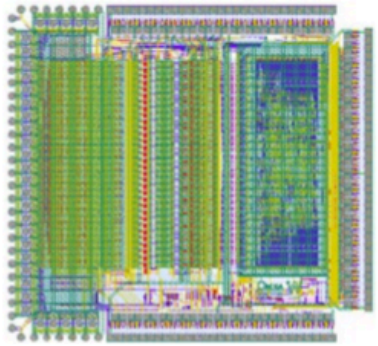
Christophe COMBARET, IPNL – CNRS IN2P3
On behalf of the CMS Muon Group

Petiroc ASIC





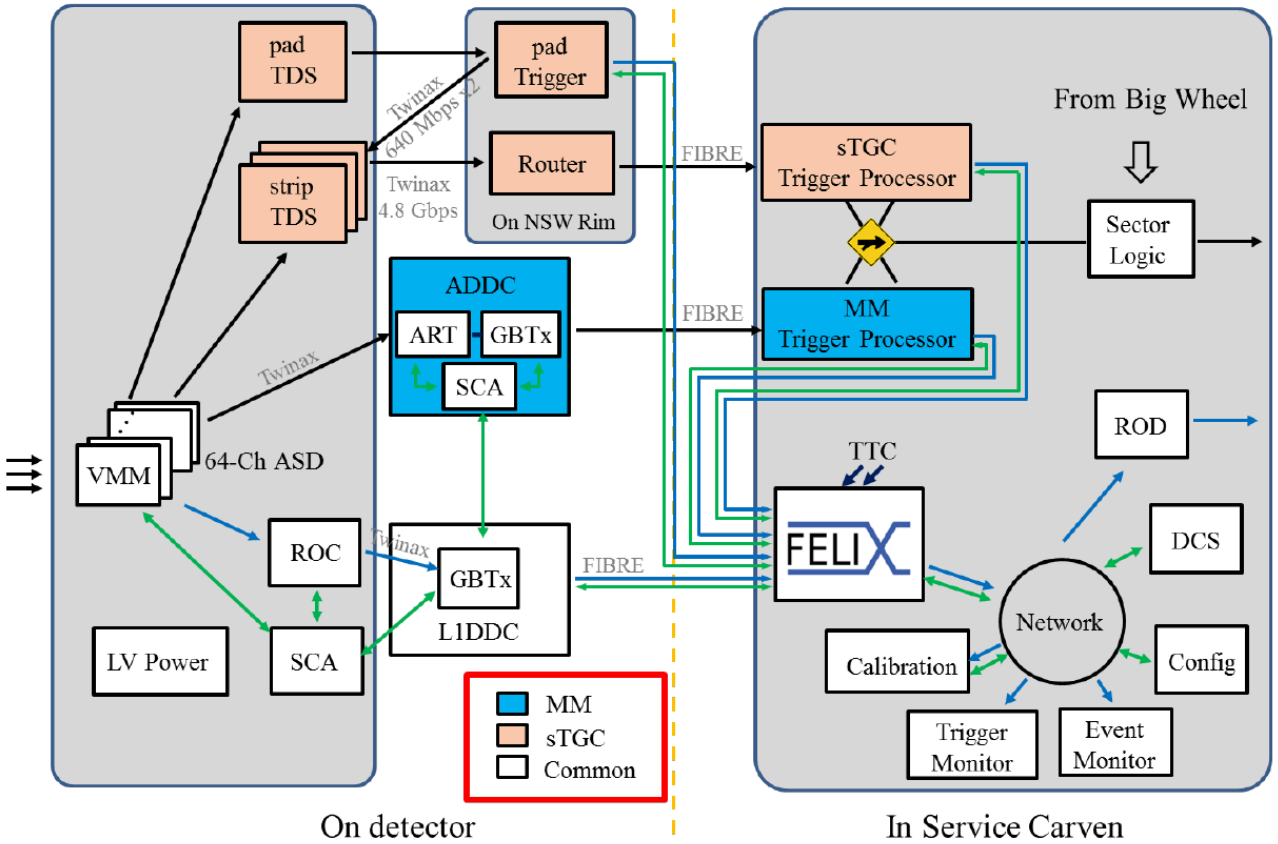
Parameter	Value
Number of Channels	32
Signal Polarity	positive or negative
Sensitivity	Voltage input amplifier, 200 Ohm matching
Timing Resolution	~ 18 ps RMS on trigger output (4 photoelectrons injected)
Dynamic Range	160 fC up to 400pC
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) TFBGA 353 (12x12x1.2mm)
Power Consumption	6 mW/channel
Inputs	32 analogue inputs, No external component required Inputs DC level adjustable
Outputs	32-channel trigger outputs ASIC level general trigger (OR of all channel) ASIC level second level general trigger (OR of all channels) Charge measurement (10 bits) Time measurement (10 bits)
Internal Programmable Features	Common trigger threshold adjustment and 6bit-DAC/channel Shaping time & gain of the charge shaper 32 x 8bit-input DAC over 1V span



C. Combaret RPC2018 , feb 19-23rd 2018

NSW Trigger and Readout

Same front-end chip for MM and sTGC



- 4 custom ASICs: VMM, ROC, TDS, ART
- 4 custom on-detector boards: L1DDC, ADDC, MM FEB, sTGC FEB,
- 2 custom on-rim boards: pad trigger, router (plus a GBT board for configuration)
- 2 custom on-USA15 boards: sTGC trigger processor, MM trigger processor

Custom ASIC Developments :

- **VMM** – 64ch front-end chip for sTGC and MM.

1st channel "hit" /bx, address sent to the **ART**

Amplitude sent to **TDS**

Addr, ampl., and time tag sent to **ROC**

- **ART** – Concentrator of 32 VMM "hit" addresses, forms data packet for GBT.
- **TDS** – Trigger Data Serialiser. Collects pulse height information from VMM.
- **ROC**– L0 readout + e-link interface to GBT.

FPGA & Board Developments:

sTGC – Rad-tol FPGA board for routing and optical transmission

Pad Trigger – Tower coincidence selection of strips

Trig Proc –finds tracks, rejects tracks not pointing to vertex. ATCA

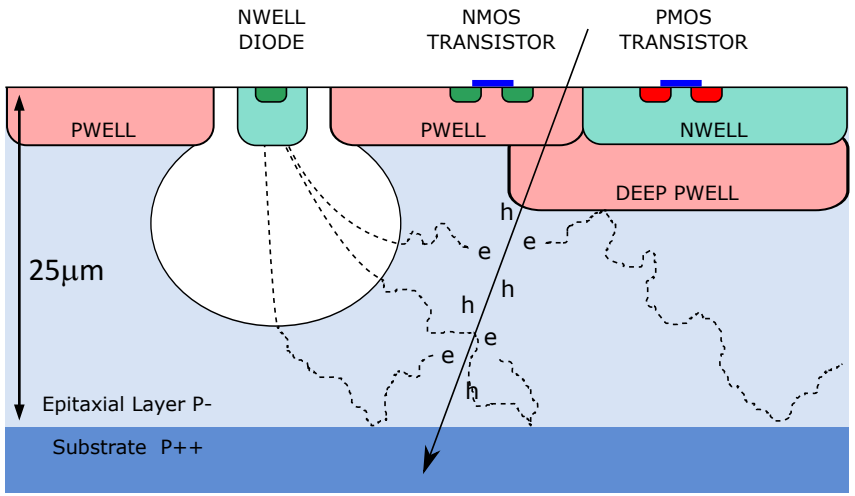
FELIX – Interface to industrial standard; PCIe

Sources : R.Richter, L.Levinson, J Zhu, S.Zimmermann, V.Polychronakos

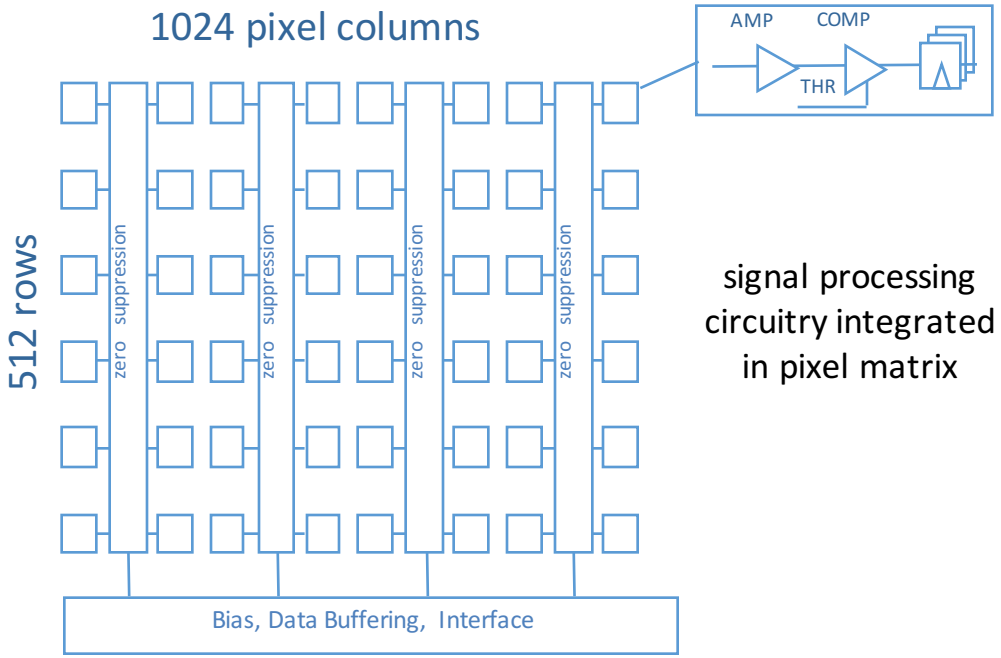
March 9, 2016 Junjie Zhu - University of Michigan 6

ALPIDE – A novel CMOS Pixel Sensors for the ALICE ITS and Muon Tracker

R&D: **CERN**, CCNU, IPHC, INFN, IRFU, NIKHEF, RAL, Yonsey

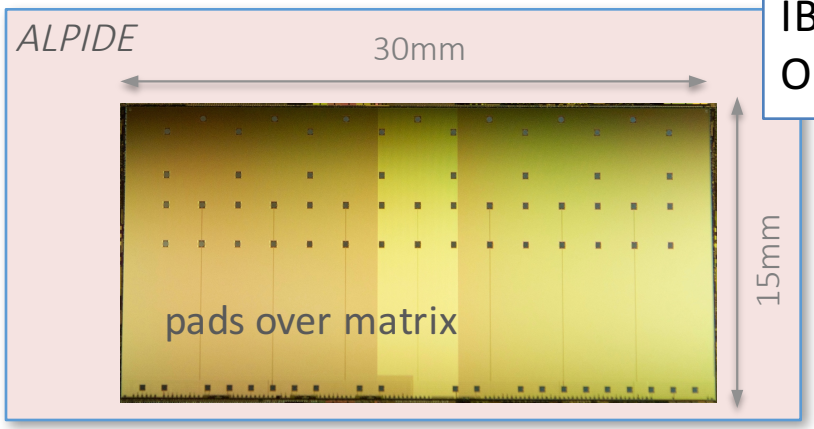


CMOS 180nm



signal processing circuitry integrated in pixel matrix

pixel capacitance 2.5 fF (@ V_{bb} = -3 V) ⇨ MIP signal ~ 50mV



IB: 50µm thick
OB: 100µm thick

130,000 pixels / cm^2 27x29x25 µm^3

Charge collection time <30ns (V_{bb} = -3V)

spatial resolution ~ 5 µm

max particle rate ~ 100 MHz / cm^2

fake-hit rate: < 10^{-9} pixel / event

Further detail in the ACES 2018 talk : Monolithic Pixel Developments (Thanushan Kugathasan)

Source: W. Snoeys, L. Musa

Radiation levels in ALICE

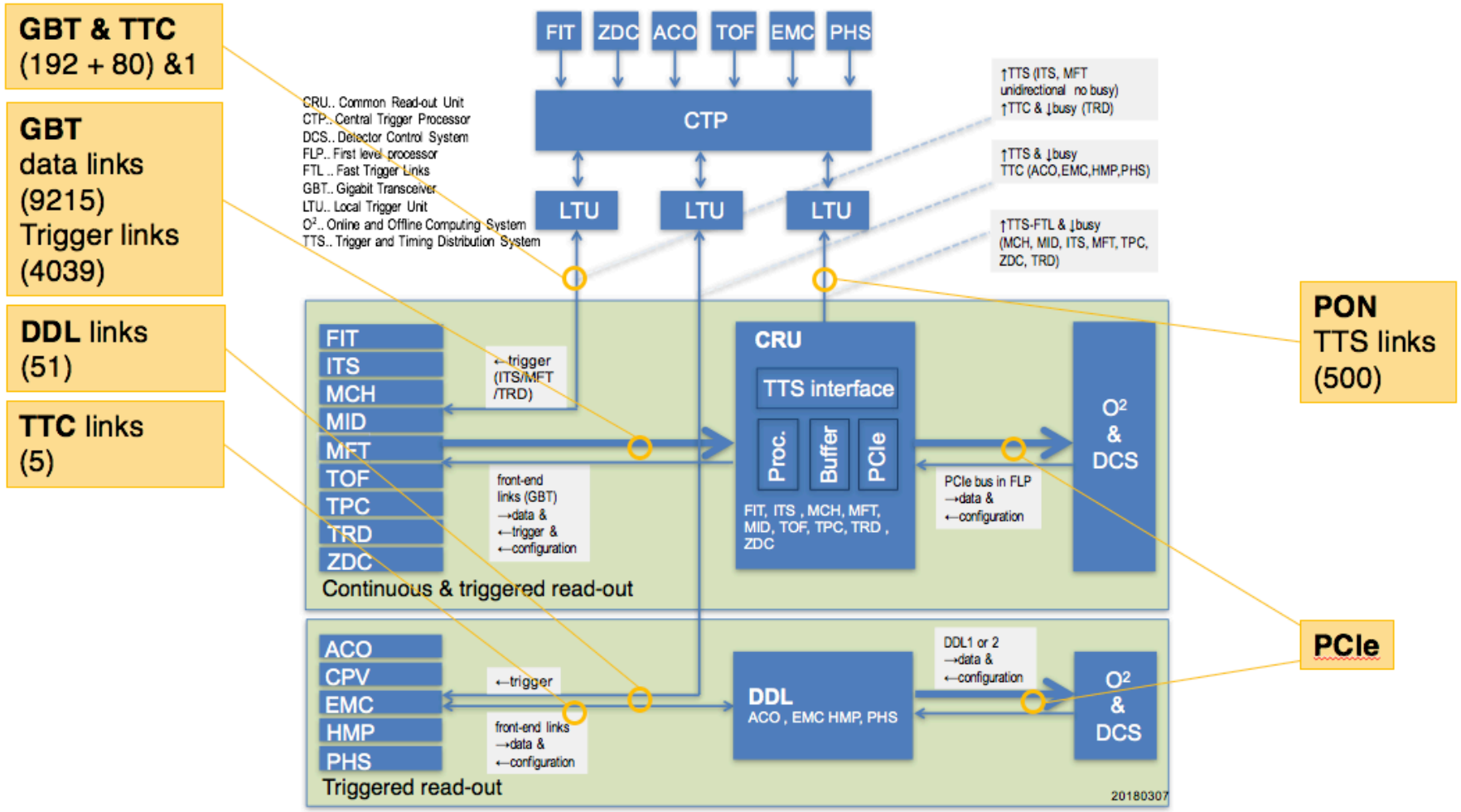
Element	r (cm)	z (cm)	TID (krad)	1 MeV neq (cm^{-2})	>20 MeV had. (kHz/cm^2)
ITS L0	2.2	[-13.5, 13.5]	646	9.2×10^{12}	1600
ITS L1	2.8	[-13.5, 13.5]	387	6.0×10^{12}	1000
ITS L2	3.6	[-13.5, 13.5]	216	3.8×10^{12}	500
ITS L3	20	[-42.1, 42.1]	13	5.2×10^{11}	28
ITS L4	22	[-42.1, 42.1]	9	5.0×10^{11}	24
ITS L5	41	[-73.7, 73.7]	6	4.6×10^{11}	10
ITS L5	43	[-73.7, 73.7]	4	4.6×10^{11}	9
MFT D0	2.5	-50	395	6.7×10^{12}	1100
MFT D1	2.5	-58	392	6.4×10^{12}	1040
MFT D2	3.0	-66	767	5.9×10^{12}	760
MFT D3	3.5	-72	427	4.3×10^{12}	520
MFT D4	3.5	-76	541	4.8×10^{12}	560
FIT1	5	-80	181	3.0×10^{12}	280
FIT2	5	340	103	1.4×10^{12}	200
TPC In	79	[-260, 260]	2.1	3.4×10^{11}	3.4
TPC Out	258	[-260, 260]	0.3	5.2×10^{10}	0.7
TRD	290	[-390, 390]	0.4	4.8×10^{10}	0.54
TOF	370	[-370, 370]	0.13	2.6×10^{10}	0.26
EMC	430	[-340, 340]	0.06	1.5×10^{10}	0.02
MCH S1	19	-536	0.42	4.2×10^{11}	3
MCH S2	24	-686	0.19	1.4×10^{11}	1
MCH S3	34	-983	0.14	1.6×10^{11}	0.9
MCH S4	45	-1292	0.18	3.0×10^{11}	1
MCH S5	50	-1422	0.91	2.5×10^{11}	0.7
CTP Rack	600	-1295	4.8×10^{-3}	7.8×10^{9}	0.03

Table 3.1: Total Ionising Dose (TID) and 1 MeV neq hadron fluence for 10 nb^{-1} Pb-Pb + 6 pb^{-1}pp + 50 nb^{-1}p-Pb collisions (including a safety factor 10) as well as high energy hadron fluence for 50 kHz Pb-Pb collisions (including a safety factor 2).

ALICE does not have significant radiation levels to worry about.

ALICE Readout Architecture

Read-out architecture



ALICE has a common back-end architecture for all sub detectors