Preamplifier, Shapers and ADCs for Phase-2 calorimeters

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Effect of luminosity increase for Phase 2 CMS Main readout

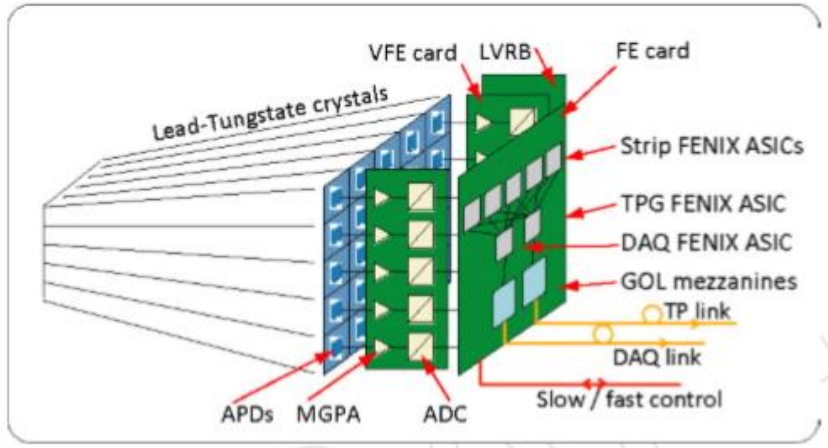
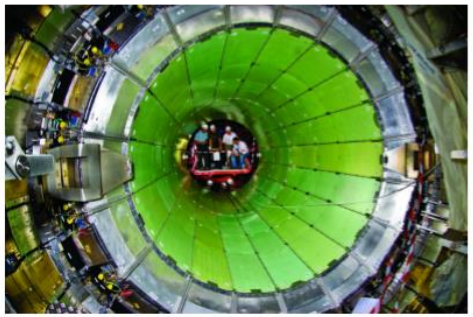


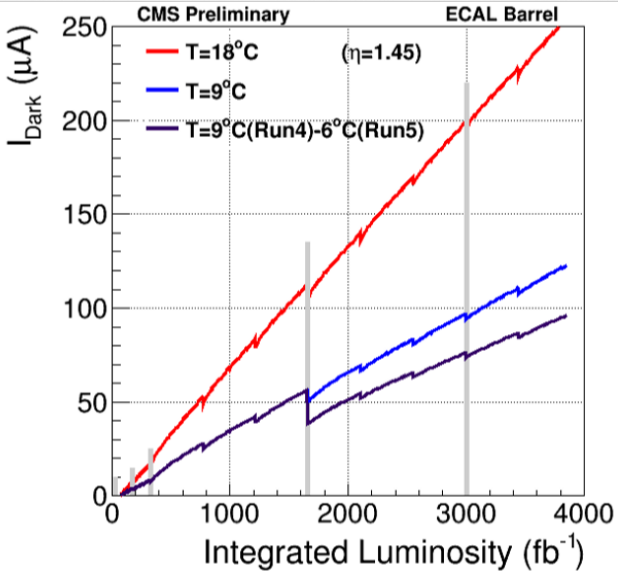
Figure 1.2: Cartoon layout of the legacy front end implementation.



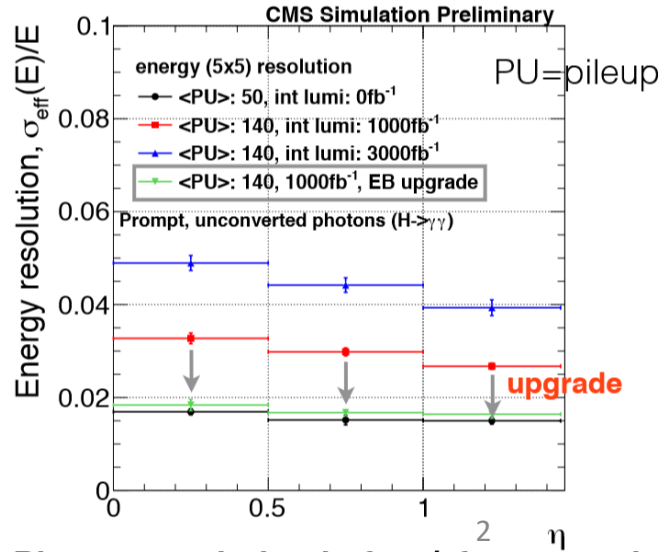
Barrel (EB)

36 supermodules (1700 crystals)
Total of 61200 $PbWO_4$ crystals
Avalanche PhotoDiode readout
coverage: $|\eta|<1.48$

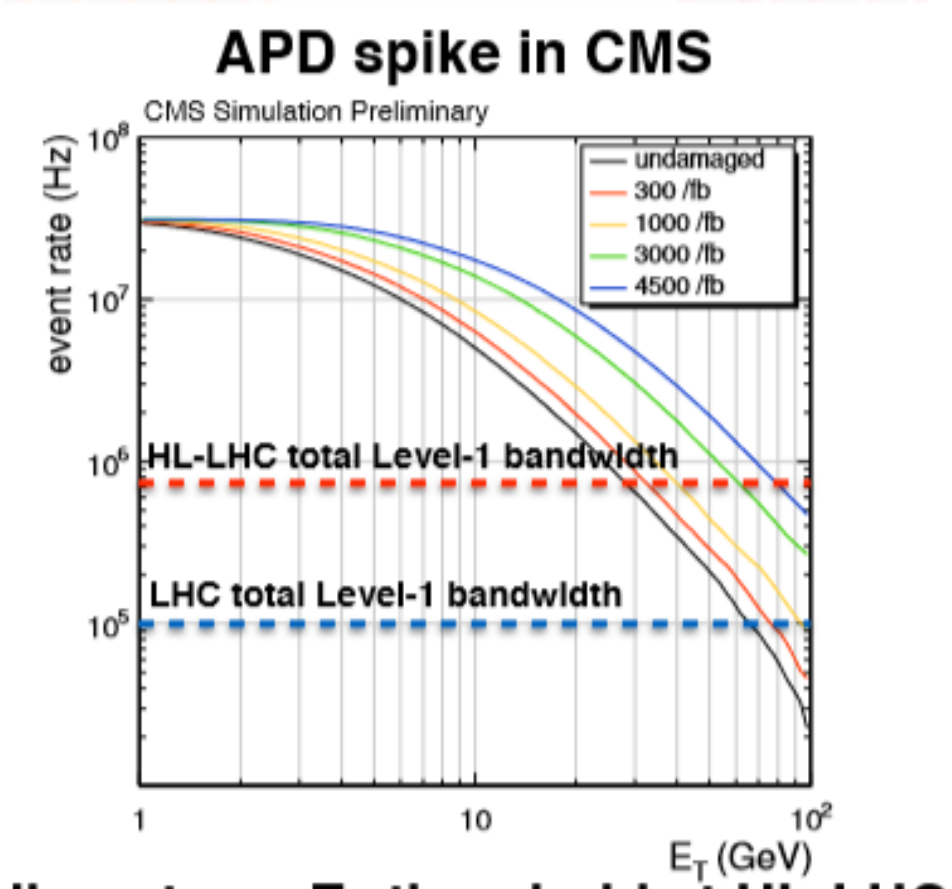
- APDs will still be used over HL-LHC
  - Larger leakage current due to irradiation
  - ×10 increase in noise would dominate resolution at HL-LHC
- Mitigation strategy
  - Cool supermodules from 18°C to 9°C
  - Implement shorter pulse shaping (new front-end)
- Necessary to maintain electron/photon resolution at right level for physics



Predicted APD dark current in HL-LHC



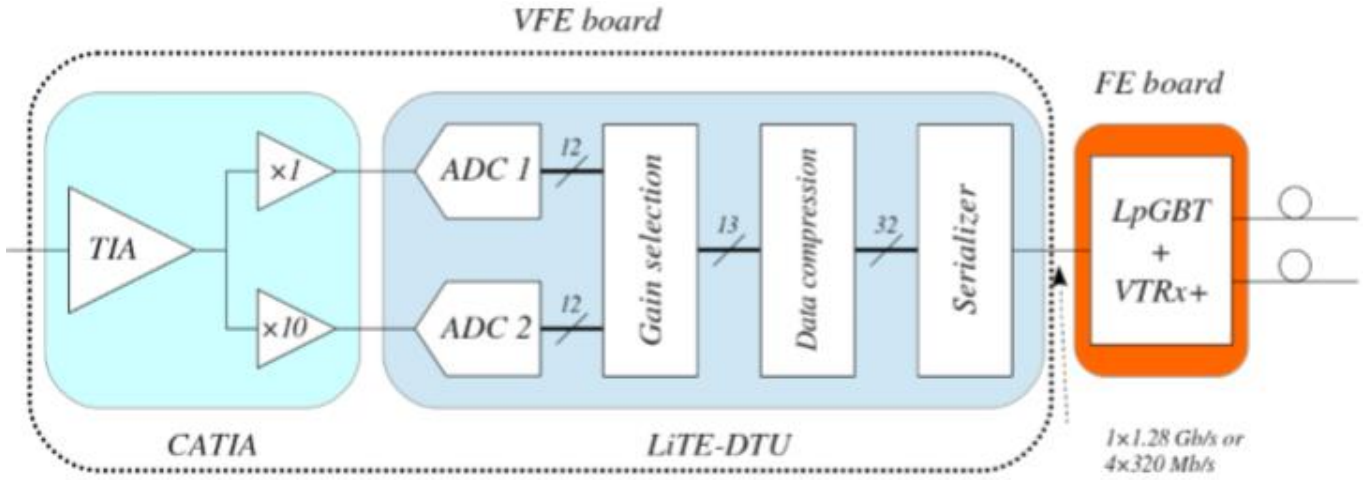
Effect of luminosity increase fror Phase 2 CMS Trigger path



Spike rate vs E_T threshold at HL-LHC

- Spikes are large isolated signals due to hadrons interactions within APD volume
- Will dominate L1 trigger rate at HL-LHC if unsuppressed
- Improved spike rejection needed (99.9% @ 5GeV) to maintain trigger sensitivity→
- Digitization at 160 MHz and fast shaping to do signal shape discrimination

Upgraded CMS ECAL Front-End architecture



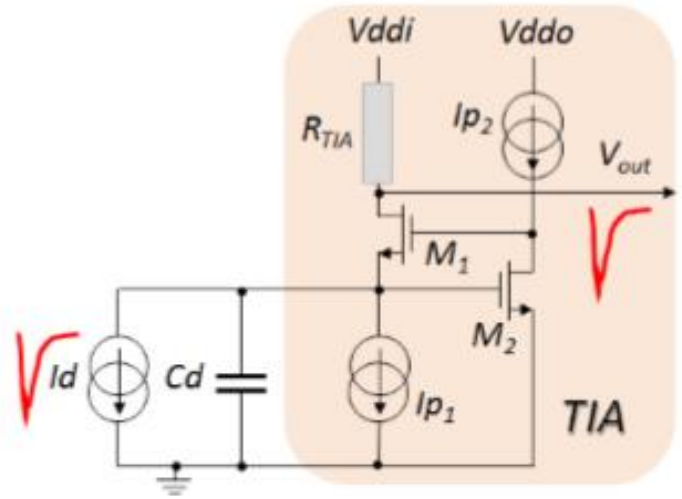
- TIA (Trans Impedance Amplifier) architecture, 50 MHz BW, bi-gain output
- Focus on fast timing : 30 ps @ 30 GeV
- Requires 160 MHz sampling
- Commercial IP ADC Core from S3 (12 bits, 10.6 ENOB)
- Both TIA outputs are converted
- Gain selection based on a time window
- Direct connection to transceiver (lpGBT & VTRx++)
- Simple digital data compression for bandwidth optimization

Data compression and output format

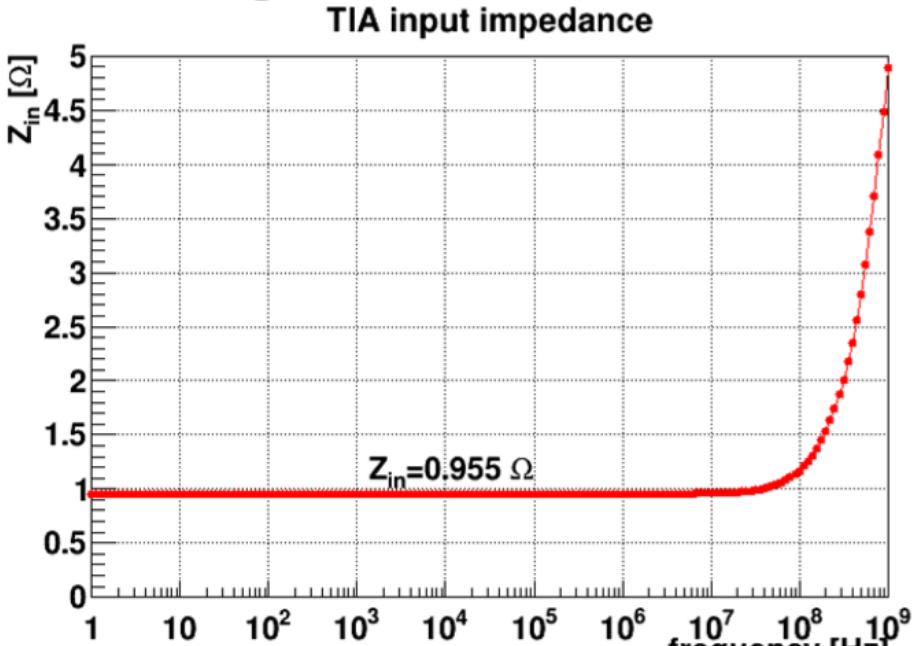
"Baseline" data format	01	6 bits sample	6 bits sample	6 bits sample	6 bits sample	6 bits sample
"Baseline" data format 1	10	sample map	6 bits sample/00	6 bits sample/00	6 bits sample/00	6 bits sample
"Signal" data format	001010	13 bits sample		13 bits sample		
"Signal" data format 1	001011	0101010101010		13 bits sample		
Frame delimiter	1101	8 bits #samples		CRC12		8 bits frame #
Idle pattern	1110	101010101010				

- 32 bits word size, to minimize bandwidth use for samples close to baseline (coded on 7 bits or less)
- Two baseline formats for non filled words
- Empty fields with alternating 1/0 pattern to maintain link synchronization

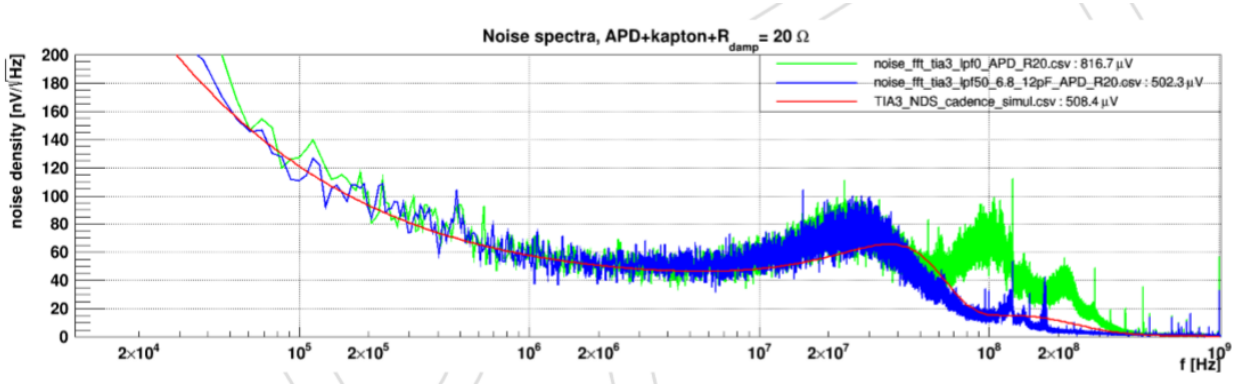
CAlorimeter Trans-Impedance Amplifier (CATIA)



- Regulated Common Gate stage
- Reduced input impedance (1 Ohm)
- Compatible with high input capacitance (200 pF)
- Bandwith of 50 MHz
- Trans-impedance value given by R_{TIA}

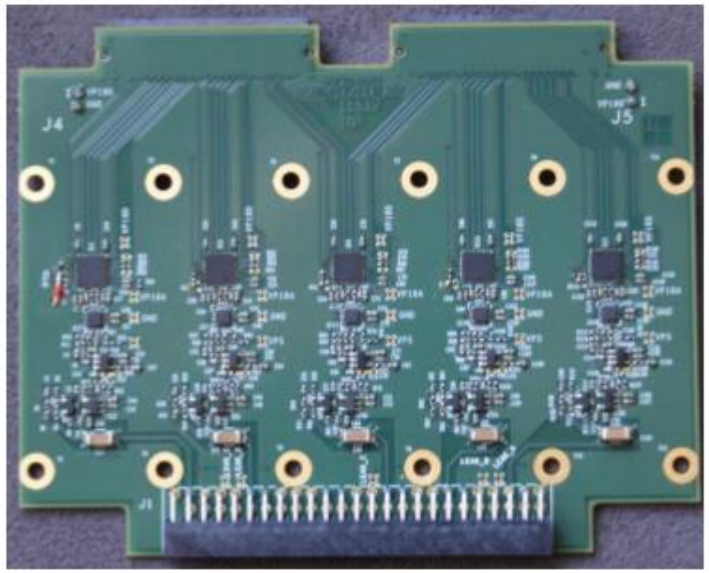


Without bandwidth limiting
With 50 MHz lowpass filter included
Cadence simulation results

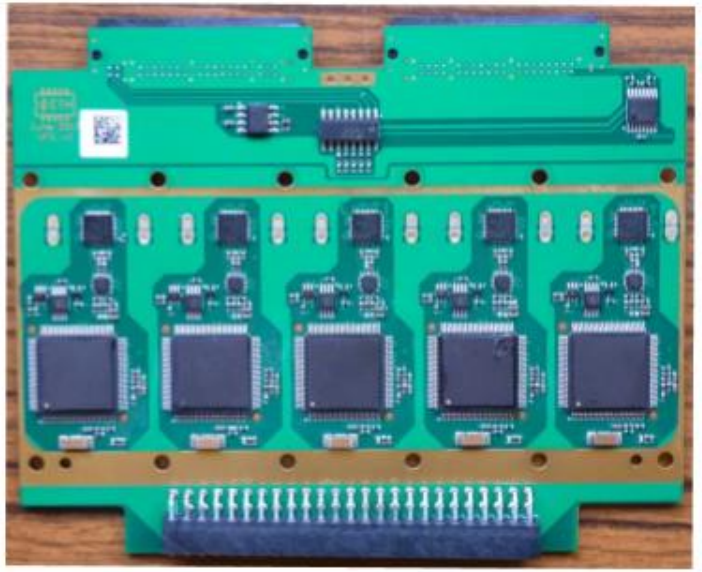


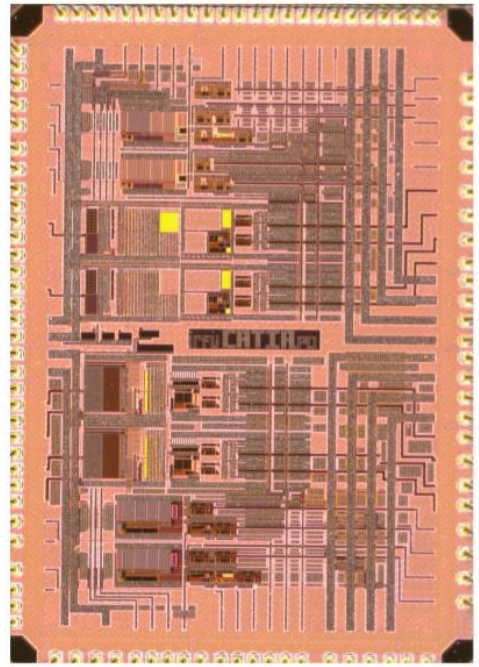
CATIA Development plan

- VFE board with TIA implemented as discrete components
- Used in test-beam in June 2017
- Readout with 14 bits COTS ADC



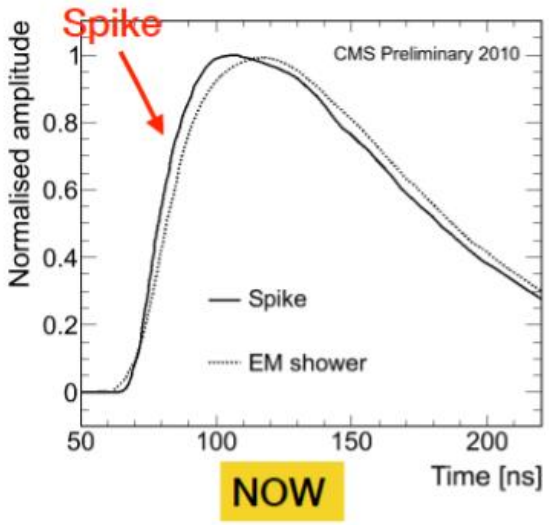
- VFE board with TIA implemented as 130 nm TSMC ASIC
- Test-beam in October 2017
- Two TIA implementations
  - 2.5V (thick oxide), in principle less rad-tol
    - Better analog performance:
    - dynamic range, linearity, SNR)
  - 1.2V (standard)
- Readout with 14 bits COTS ADC

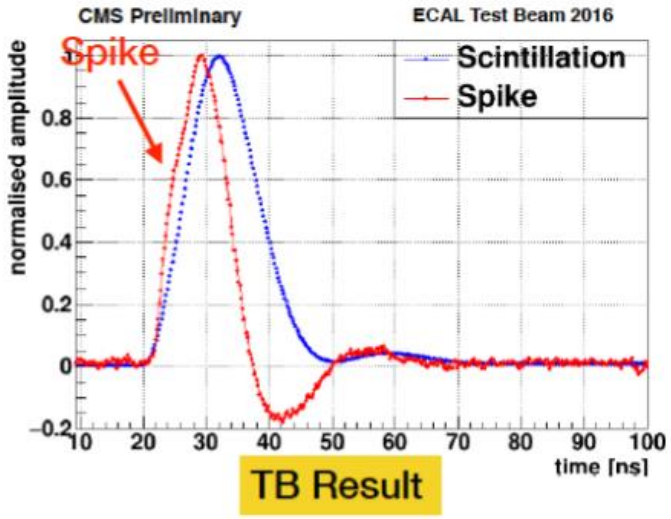




Microphotograph of the CATIA ASIC

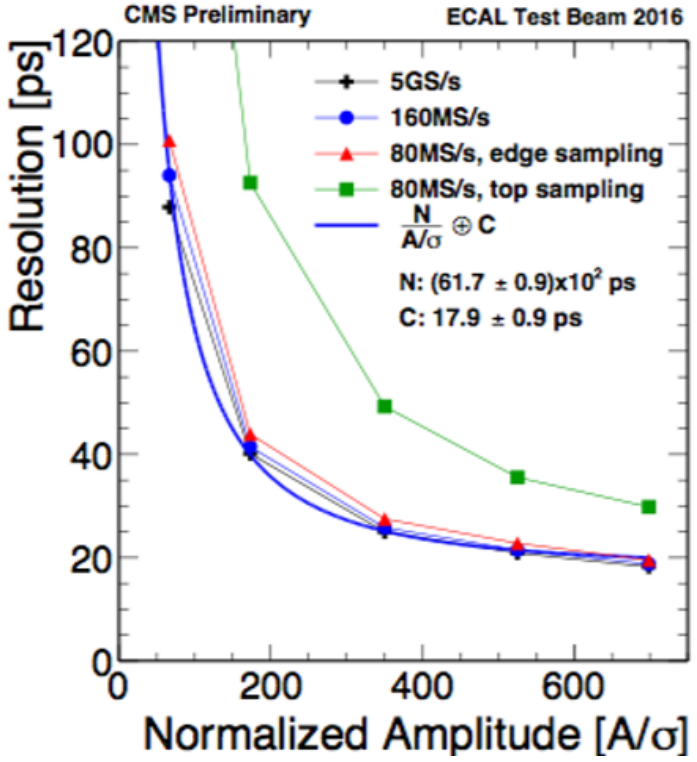
Test-beam performance





Timing resolution of discrete component TIA

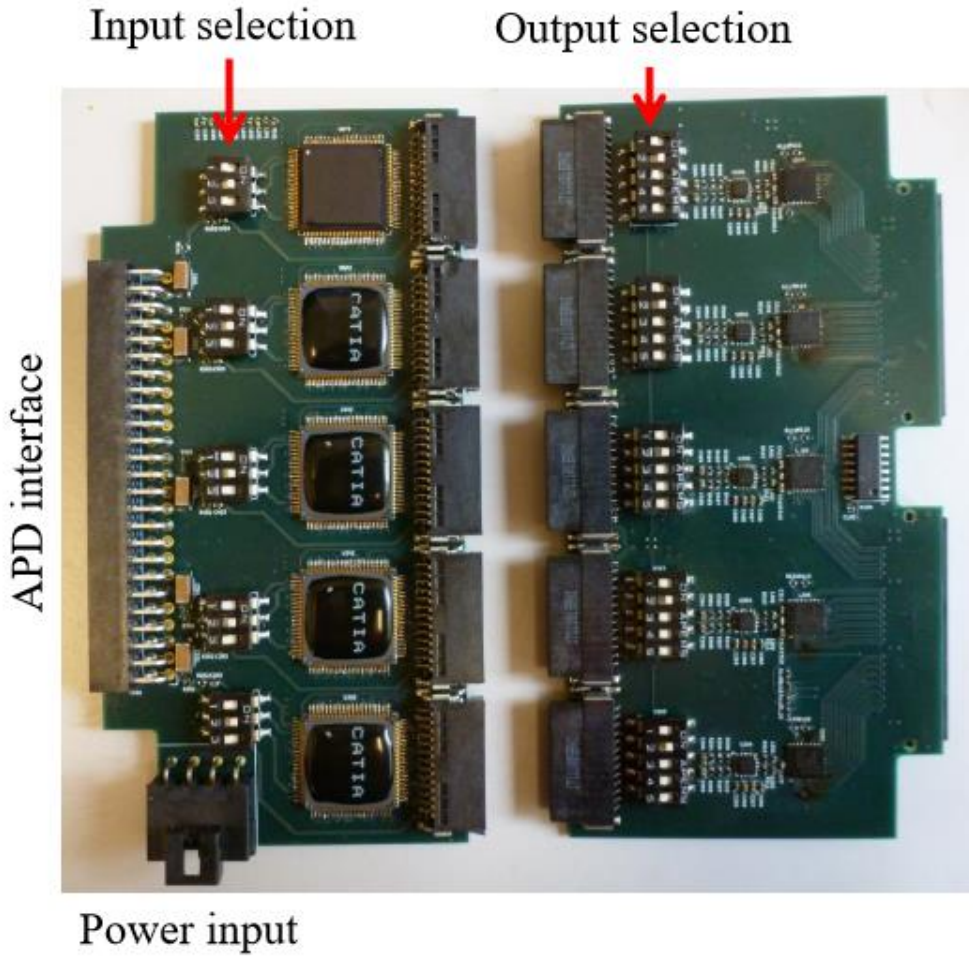
in H4 test beam



- Minimal (fast) pulse shaping
- Exploit fast rise time of PbWO4 scintillation signal
- 160 MSPS sampling is needed to simultaneously resolve pulse leading edge (timing) and pulse maximum (energy)

30 ps resolution achieved at 25 GeV (HL-LHC start)
30 ps resolution achieved at 60 GeV (HL-LHC end)

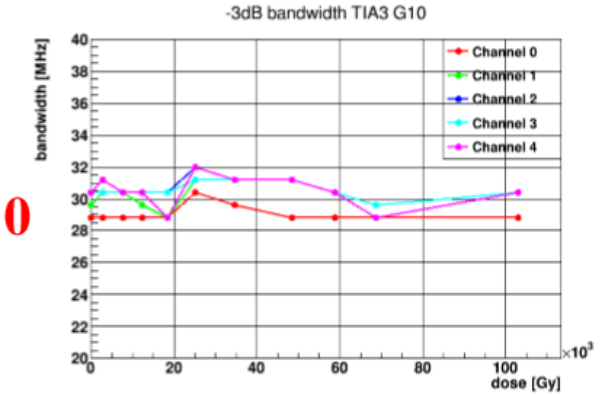
CATIA Radiation tests

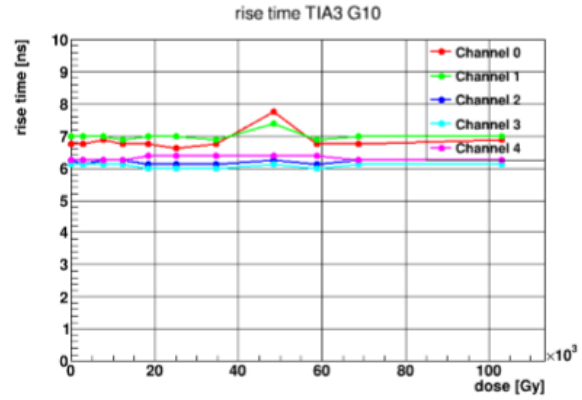


Bandwidth

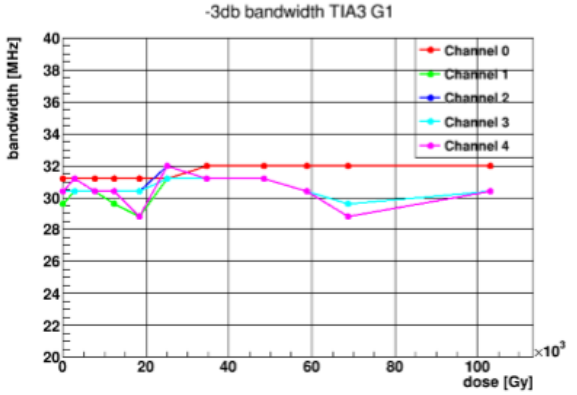
Rise time

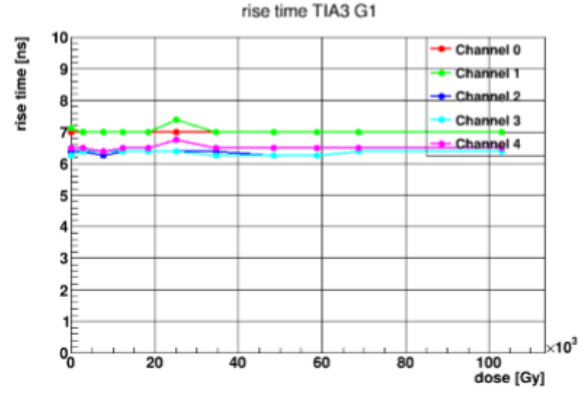
G10





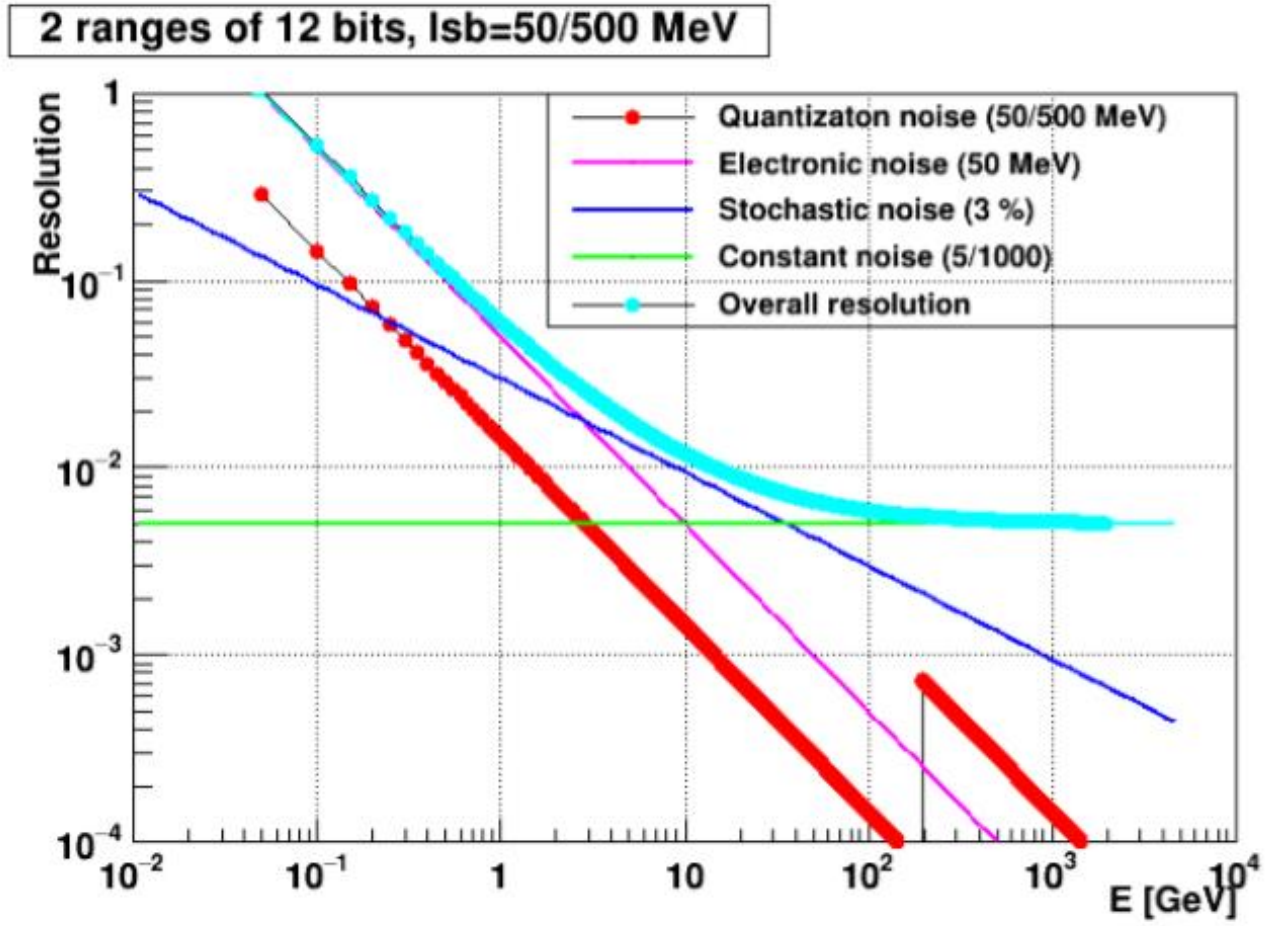
G1





2.5V CATIA version is OK and chosen as baseline

CMS ECAL Quantization scheme



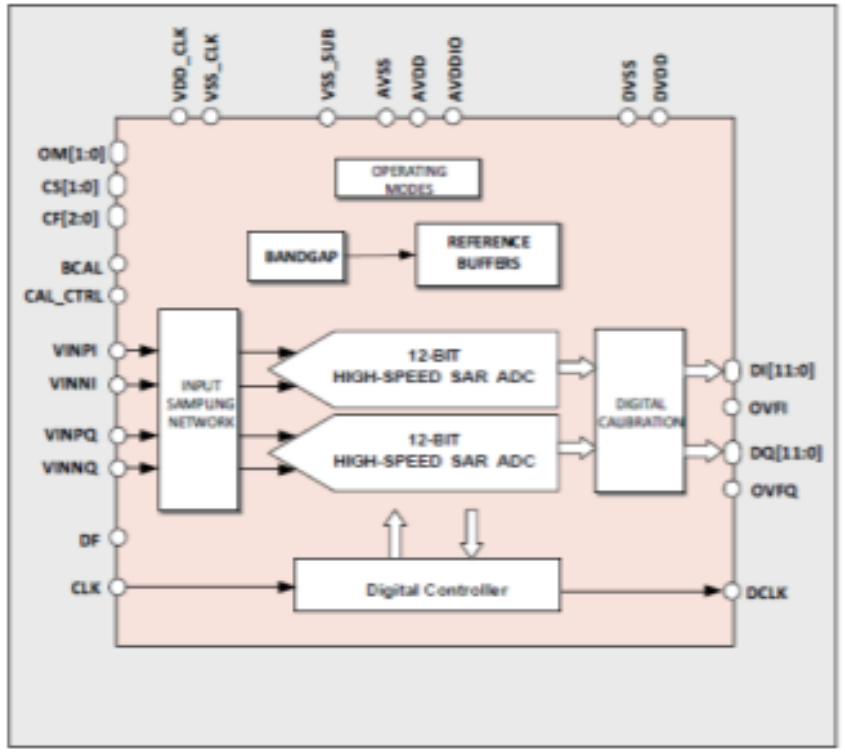
- 15 bits analog dynamic range
- Not achievable with low-cost, low-power, high speed available ADCs

- Dual gain system with two 12 bits ADC,
- Gains 1 and 10

Commercial ADC IP

Ultra-Small Ultra-Efficient SAR ADC

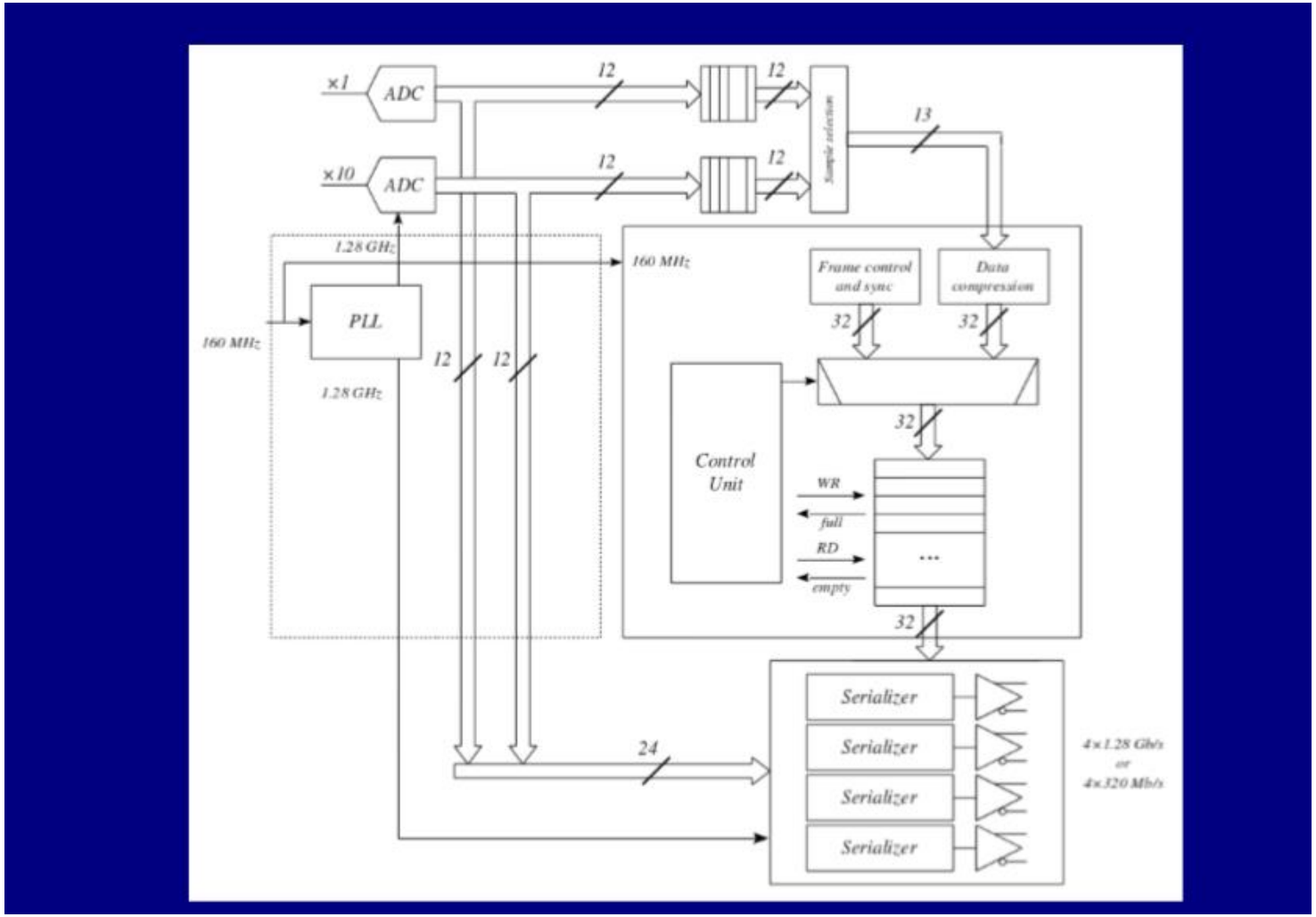
Block Diagram



- Exists with slightly different parameters in different technologies
- Chosen for CMS, adaptation underway to 65 nm TSMC (CERN validated technology)
- Radiation hardening done at design level on the IP by S3

Specification	*min*	*typ*	*max*	*unit*
Sampling rate	160			MS/s
Resolution	12			bit
Supply voltage	1.08	1.2	1.32	V
Differential input range		±0.5		V
DNL			± 0.9	LSB
INL			± 1.5	LSB
Operational temperature	-20	25	85	°C
Power consumption		20		mW
Latency		15		T_{CK}
Calibration time			38200	T_{CK}
Technology	CMOS 65 nm *(9+1 metal stack)*			
TID tolerance	20			kGy
SEU tolerance *(control only)*	15			MeV cm^2/mg

ADC/serializer test chip under development within CMS



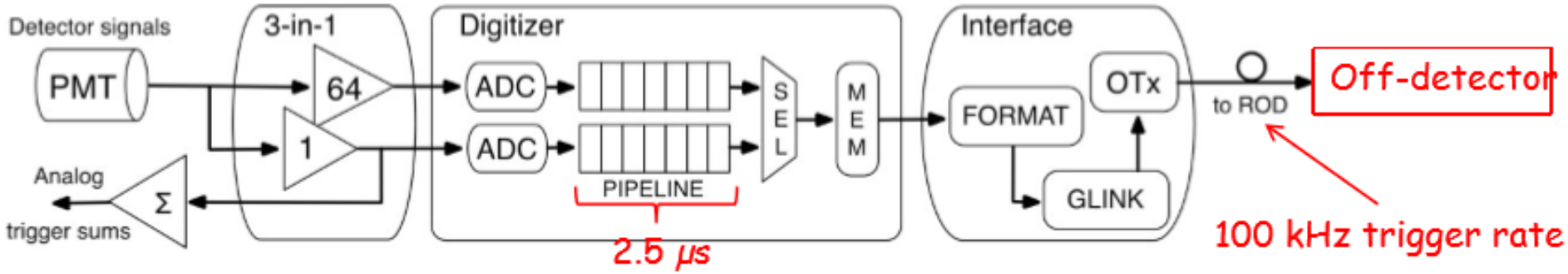
- Contract signed with S3
  - 30 March 2018
- Verilog, abstract, timing view
  - 30 May 2018
- Final GDSII
  - 6 September 2018

CMS Calorimeter Very Front-End Schedule

- CATIA
  - Finalize prototyping during 2019
    - Two MPW runs
  - Engineering run in 2020
- ADC
  - Finalize prototyping during 2019
    - Two MPW runs
  - Engineering run in 2020

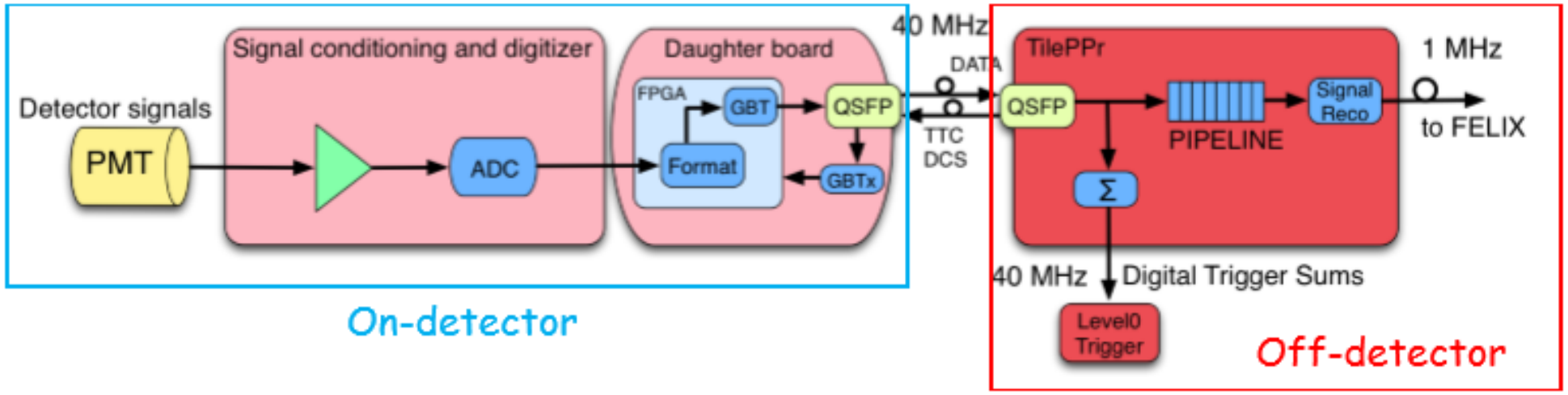
Scope and motivation of the HL-LHC upgrade of the ATLAS Tile Calorimeter

- Detector components (absorber, scintillating tiles, fibers and PMTs) do not need replacement
- Readout electronics has to be replaced
  - Present digital readout is not compatible with HL-LHC architecture
  - Electronics is ageing (time+radiation degradation). Some parts are no longer produced
  - Need to provide full granularity digital data to level 0/1 triggers at 40 MHz
  - Present on-detector electronics designed for max rate of 100 kHz



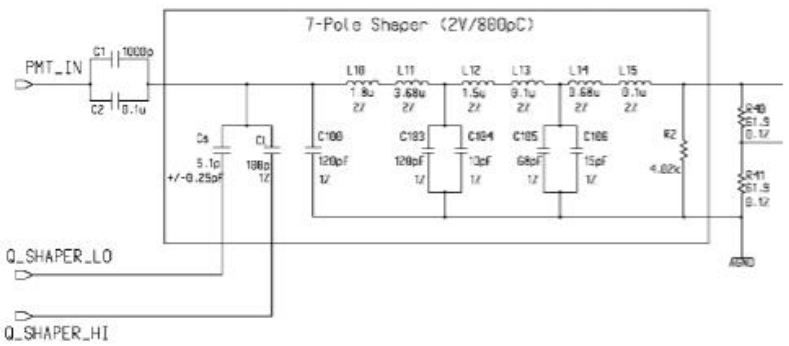
Upgraded readout architecture

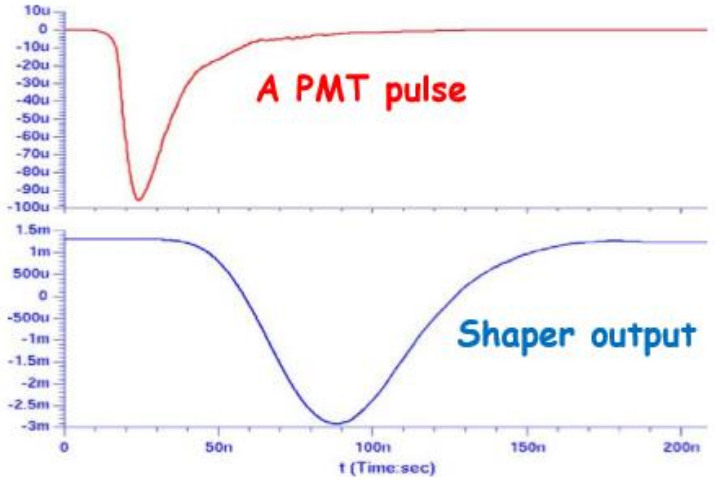
- All digital data transmitted off-detector at 40 MHz
- Simpler architecture
- Improved flexibility for off-detector data processing for L0/L1 trigger



3-in-1 Front-End signal processing

- Optimized version of the present version of the 3-in-1 board, option chosen to be implemented for the upgrade
- Seven pole shaper circuit (only passive components)
- Transforms the PMT pulse into a gaussian pulse, amplitude proportional to PMT signal total charge

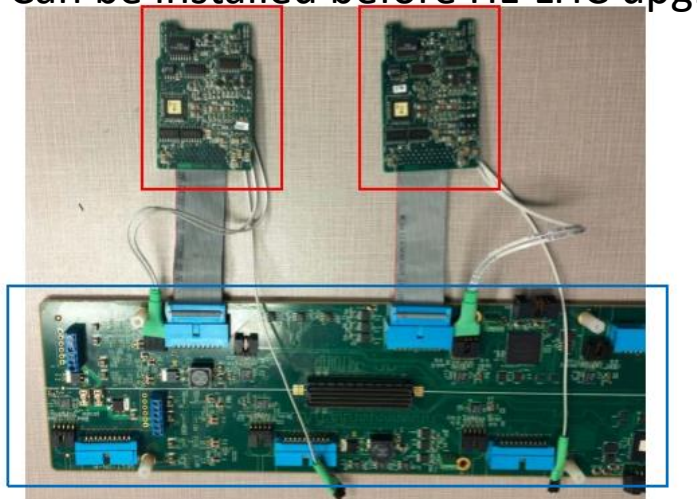




Upgrade digitization : 12 bits (COTS) ADC instead of 10 bits

Compatible with present analog trigger (no longer used for Phase-2)

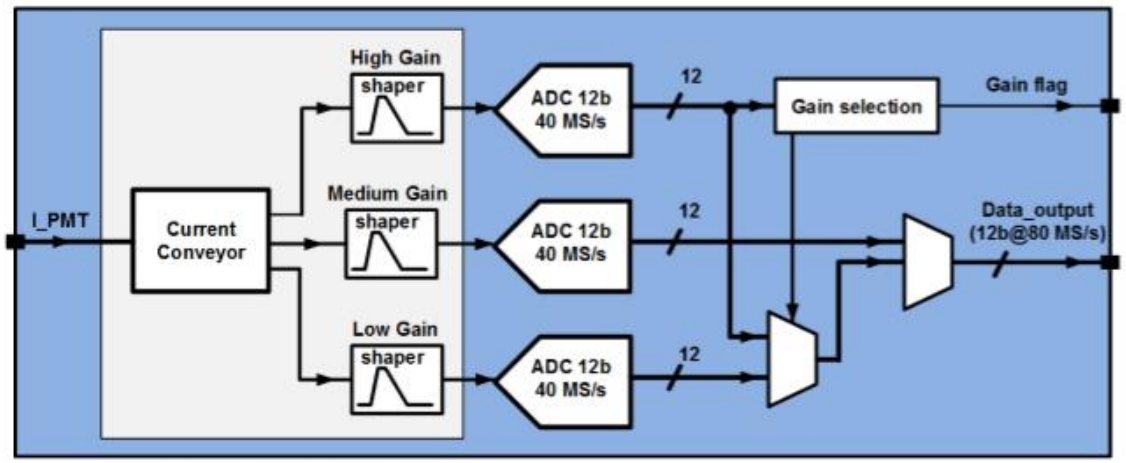
Can be installed before HL-LHC upgrade

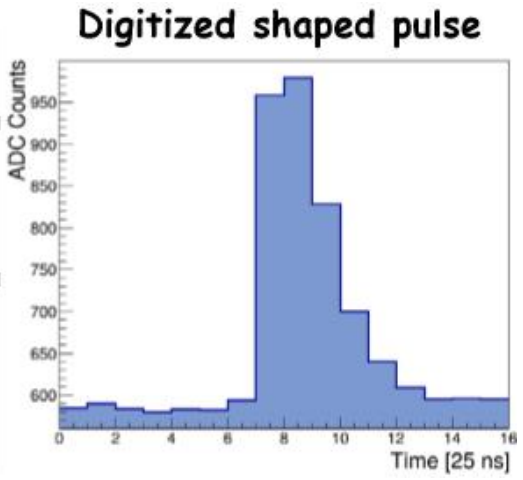


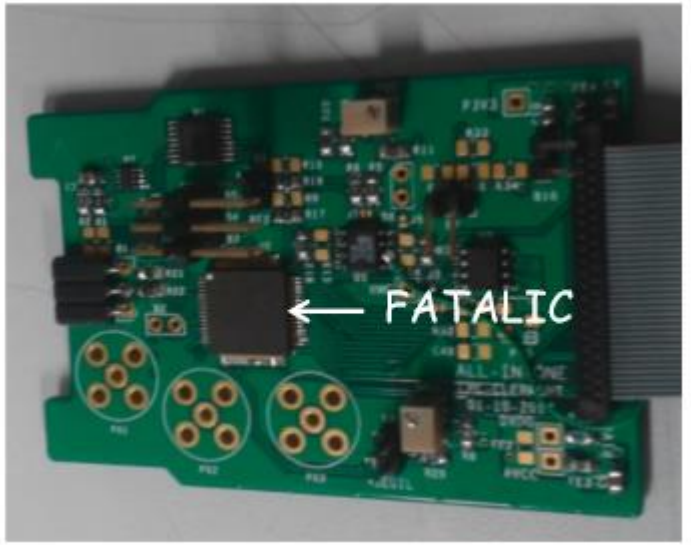
- Validated performance prototypes
- Slow integrator channel (used for Van Der Meer scans) has higher sensitivity than other options

Front-end ATLas Tile Circuit (FATALIC) development

- Faster shaping than 3-in-1 board
- Amplification, shaping and digitization (In-house 40 MHz 12 bits, pipeline design) in one unique ASIC
- 130 nm GF technology

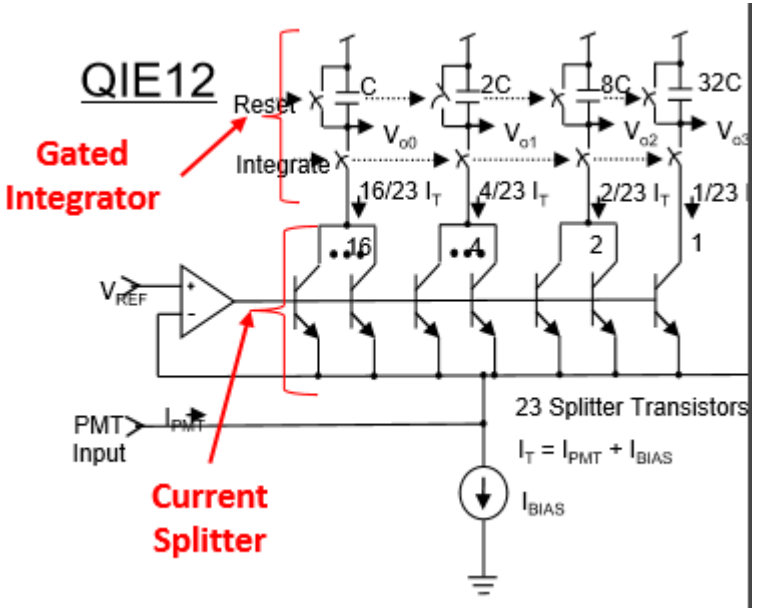


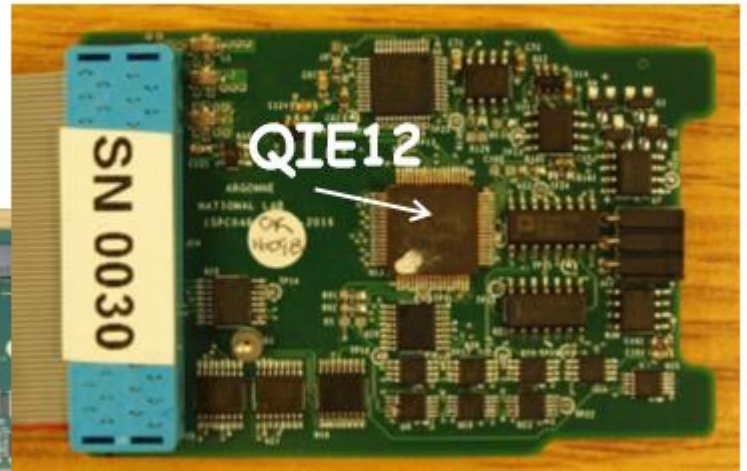




QIE signal processing development

- PMT current integrated in a capacitor bank
- Capacitors multiplexed in time to allow operation at 40 MHz without deadtime
- Current splitter to achieve 17 bits dynamic range
- Radiation tolerant design
- QIE boards have mostly point to point signal connections and power distributions
- Signal processing done on Front-End board





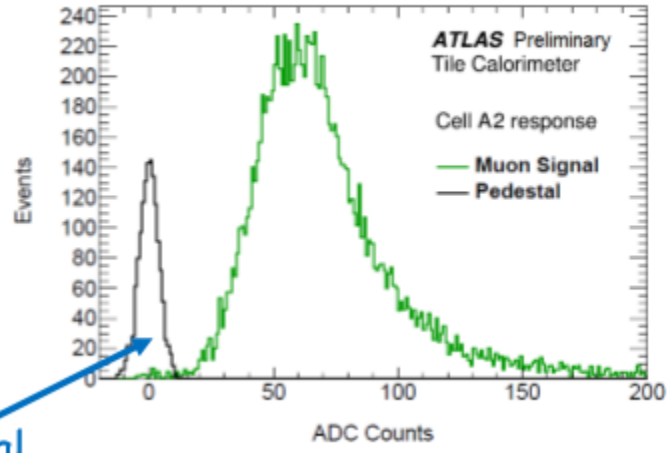
Testbeam results

- 3-in-1 and QIE system show good performance
- Signal to noise ratio improved with respect

to present system

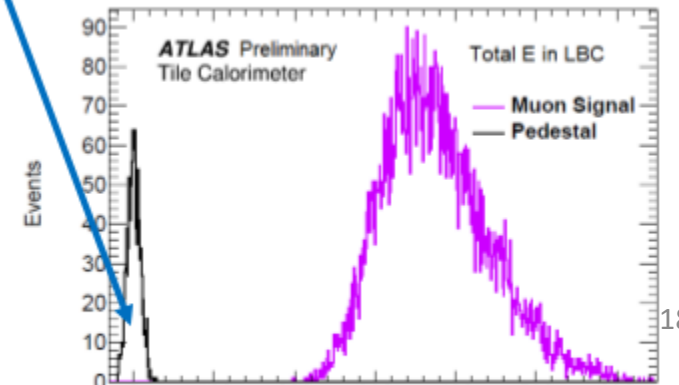
- Muon signal well visible
- FATALIC option shows higher noise

Muon signal in smallest cell @ 20°

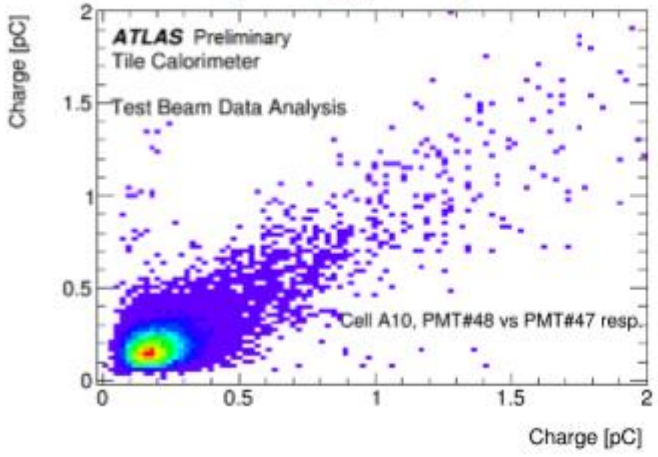


pedestal

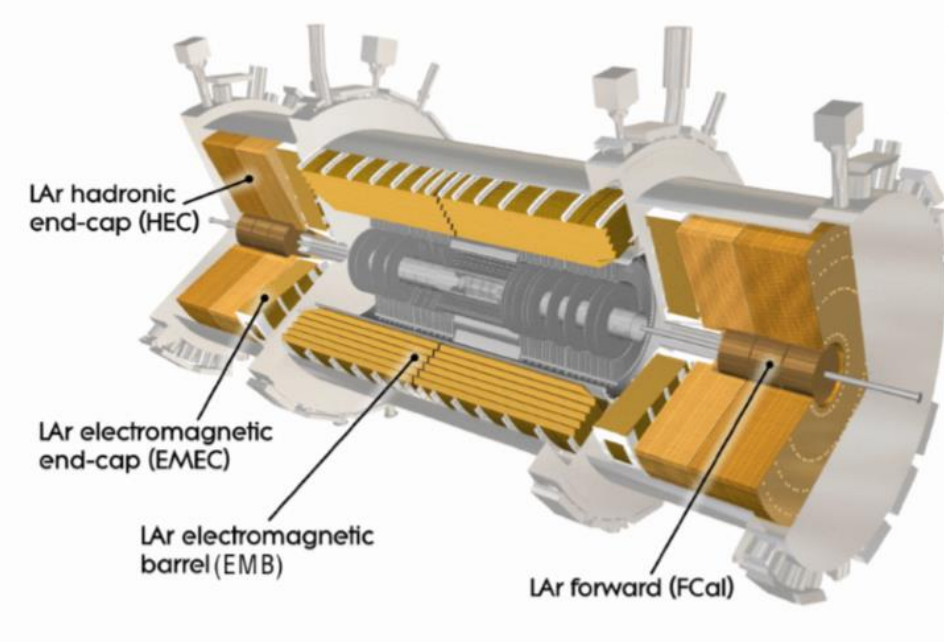
Total Muon signal in TileCal @ 20°

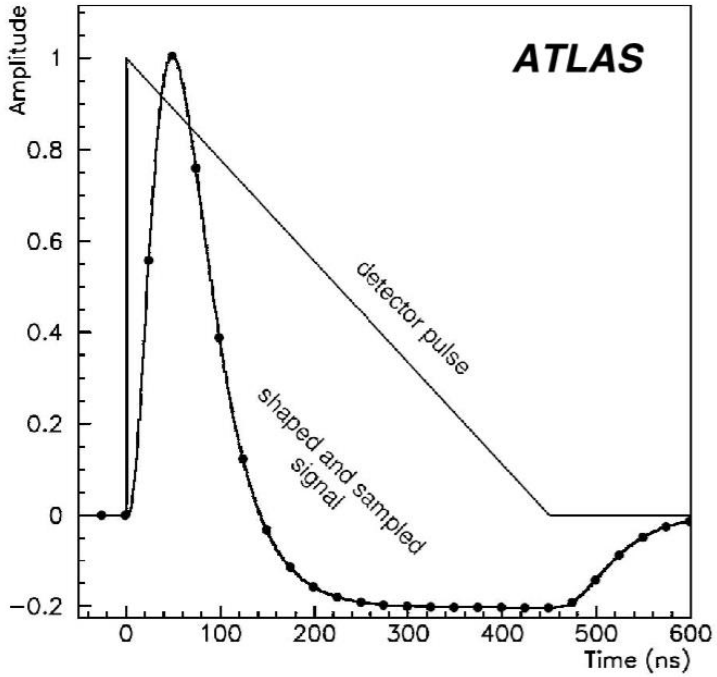


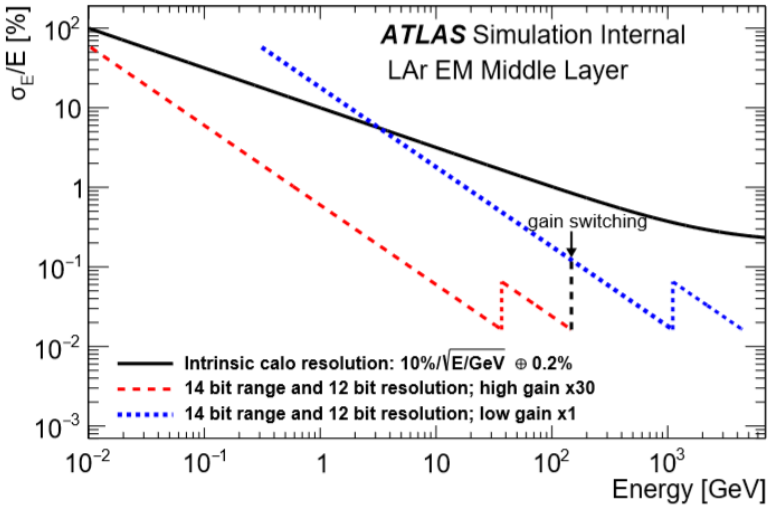
Correlation of 2 PMTs of the same cell



Context of ATLAS Lar Phase-2 upgrade



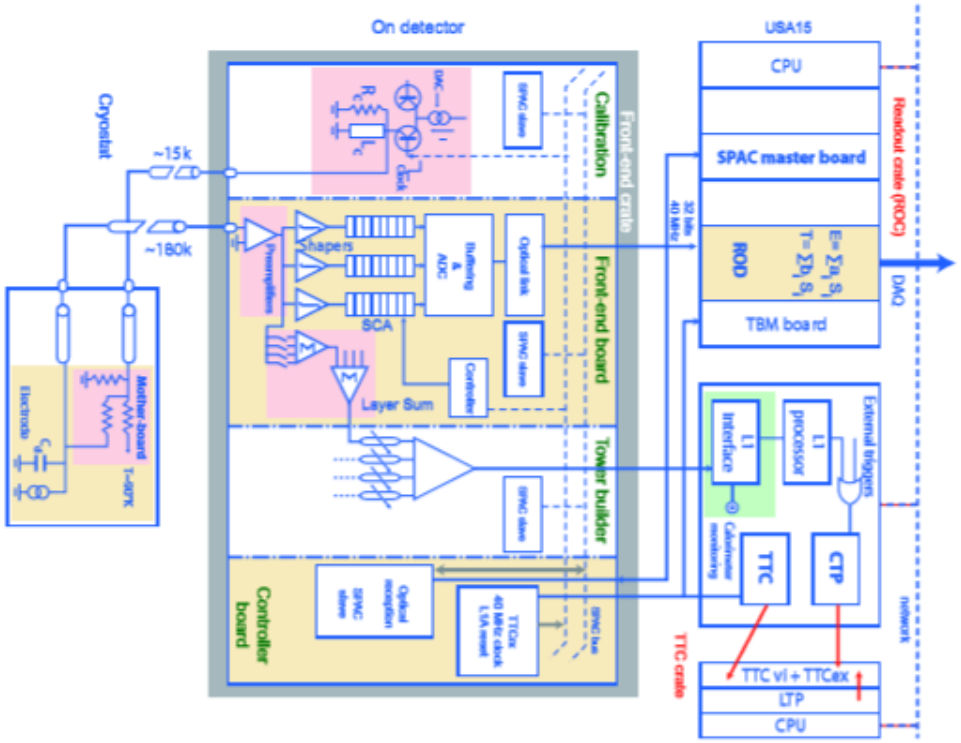




- Analog dynamic range : 16-17 bits
- Keep present analog processing philosophy : preamplifier + CR-RC2 bipolar shaping. Add adjustable shaping time constant
- Change digitization scheme from three gains/12 bits ADC to two gains/14 bit ADC (12 bits ENOB)
- All data digitized at 40 MSPS, sent off-detector for all bunch crossings→ full granularity available for trigger decision
- No on-detector pipelines

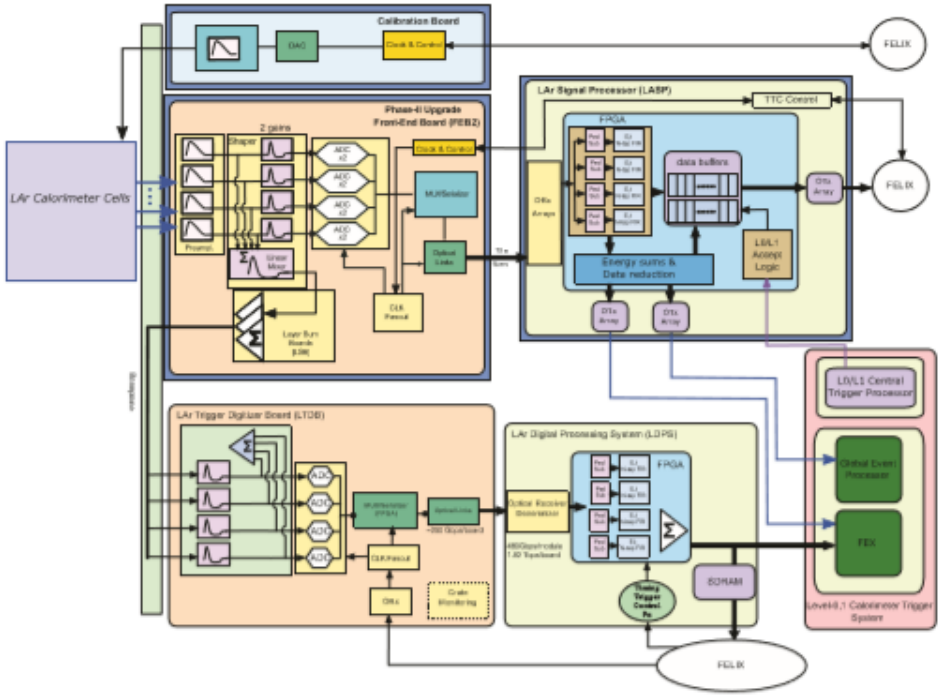
Readout system architecture

Present readout system



- Analog trigger sums
- Replaced in Phase-1 by digital trigger board (LTDB), with improved granularity
- Shaped signal stored in analog memories
- Digitized and sent to back-end after L1A decision

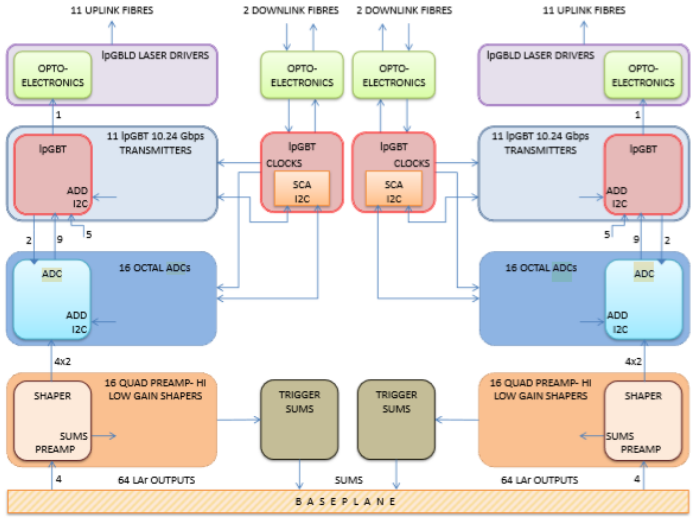
Phase-2 readout system

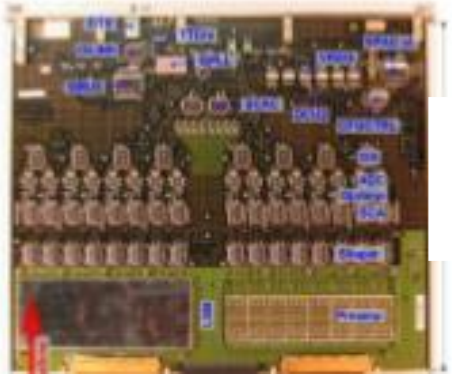


- LTDB still present, as Level-0 trigger and coarse readout system
- Shaped signal digitized on the fly and sent directly to Back-End

ATLAS LAr analog Front-End R&D

- New designs to allow for real time digitization at 40 MSPS
- Reduction of power dissipation by a factor of ≈ 10
- No longer analog memory on Front-End boards
- Two designs under development
  - 130 nm TSMC CMOS LAUROC chip
  - 65 nm TSMC CMOS HLC chip
- Common test-bench, to allow reliable performance comparisons
- Technical requirements
  - Capacitance [nF] 0.25 (0.5) 1.3 (2.5)
  - Termination [Ω] 50 25
  - Current ranges [mA] 0.06 & 2 0.6 & 10
  - Maximum ENI [nA rms] 60 200
  - Peaking time 10-100% [ns] ~ 40
  - Max non-linearity [%] < 0.2 (0.5)
  - Trimmable termination [Ω] ~ +/-2.5





ATLAS LAr FEB 128 ch 490 mm×410 mm 0.7 W/ch

LAUROC development (130 nm CMOS)

- New « negative noise figure preamp » (patent filed)

Ωmega

- Preamp Input impedance
  - Super Common Base: low input impedance
  - Amplifier = low noise voltage sensitive
  - Fine tuning of Zin (±5%) possible with C2

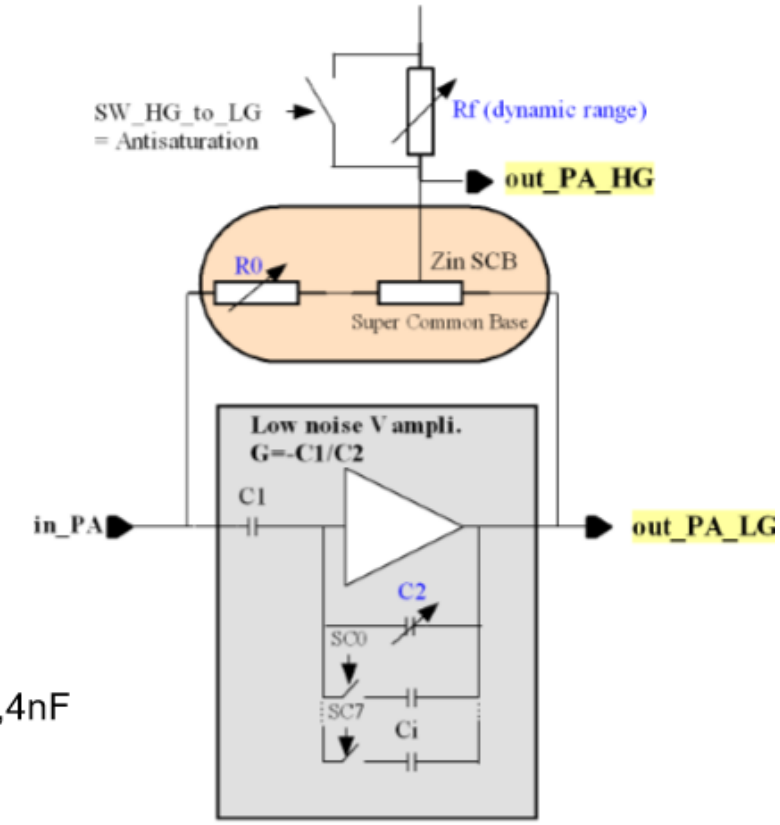
$$Z_{in}\,PA = \frac{R_0 + Z_{in}(SCB)}{1 + |G|}$$

- Noise $\dfrac{4kTR_0}{(1+|G|)^2}$
  - Electronically cooled resistor

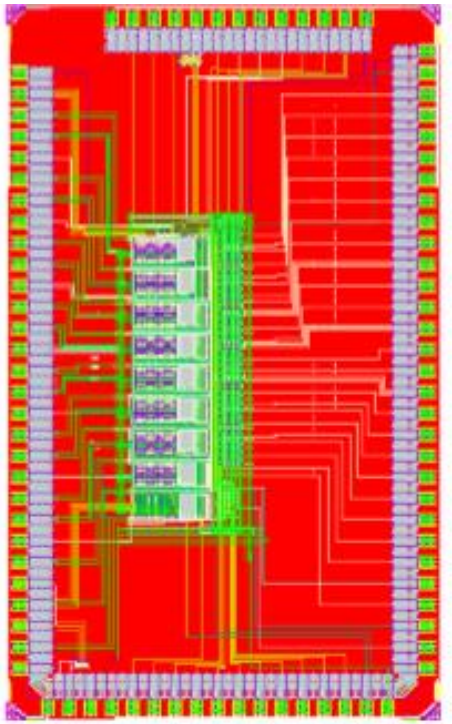
- Preamp 50 Ω, 2 mA max (Front), Cd=400pF
  - Z_{in} tuning: R_0= 500 Ω, G = -C_1/C_2=-9
  - Noise : 5 Ω
  - HG dynamic range: R_f =5K (or 10K)

- Preamp 25 Ω, 10 mA max (Middle/Back), Cd=1,4nF
  - R_0= 100 Ω, G = - C_1/C_2 = -3
  - Noise : 6 Ω
  - HG dynamic range: R_f =1K (or 2K)

- HG and LG outputs

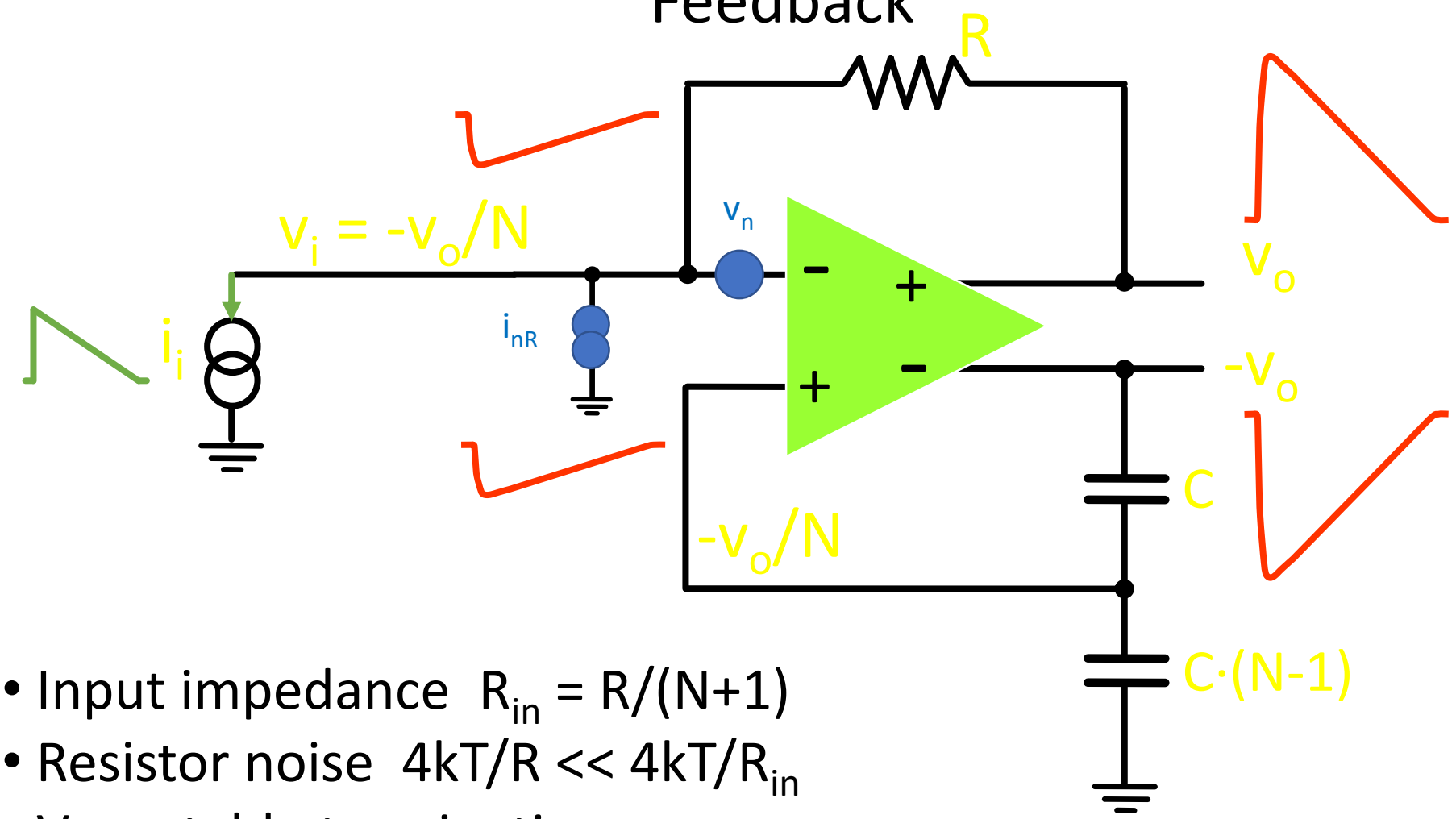


R0, C2 tunable to set absolute value of Zin
Ci: 8-bit fine adjustement of Zin (±5%)
using Slow Control parameters



Chip size : 3.3 X 2 mm²
Packaging in PGA144 cavity 10x10mm2
Pad opening : 72X58 µm2 pitch 100µm

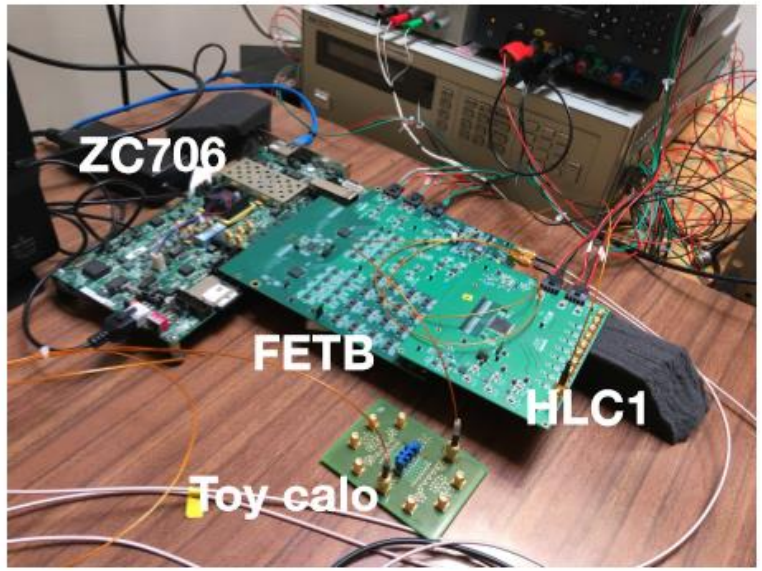
HLC architecture :Fully-Differential FE Amplifier with Passive Feedback

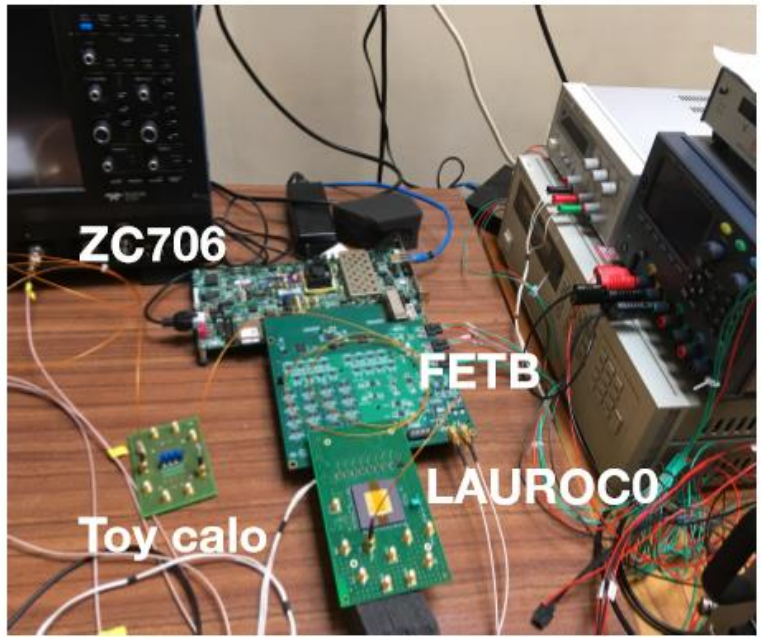


- Input impedance $R_{in} = R/(N+1)$
- Resistor noise $4kT/R << 4kT/R_{in}$
- Very stable termination (R, N indep. of signal current and active components)
- Fully-differential output
- 65 nm TSMC CMOS

Test setup

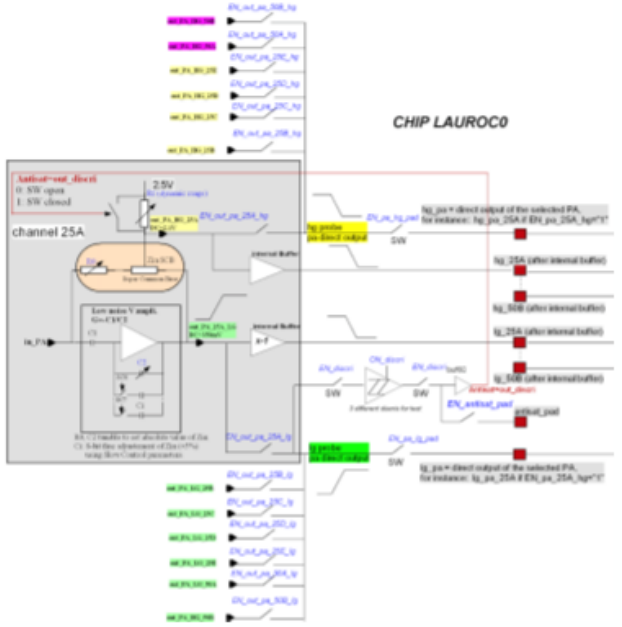
- Setup components: toy calo, LAUROC0/HLC1 test board, 25/50 Ohm axon cables, FE Test Board, Xilinx ZC706 board
- 2 toy calo boards with Rinj= 1kOhm/3kOhm and Cdet= 1.5nF/300pF for 25/50 channel
- Same setup for LAUROC0 and HLC1
- Measurement protocol for linearity: take the minimum of the pulse and do a fit around it to get the amplitude value



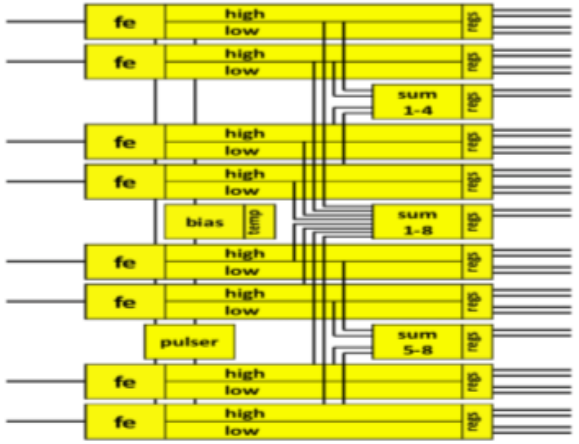


LAUROC and HLC preamp features

- **LAUROC0:**
  - 25, 50 and 25_50 Ohm channels
  - PA delivers two gains: high gain and low gain
  - A discriminator is triggered to cut hg when the hg is not linear in order to not distort the lg
  - Discriminator triggering is controlled by a Voltage threshold on the lg output
  - Rf = 1kOhm/2kOhm for 25 Ohm and 5kOhm/10kOhm for 50 Ohm channel allows to choose the gain of the hg
  - Input impedance tuning through set of capacitor (C2)



- **HLC1:**
  - 8 identical 25_50 Ohm channels
  - PA delivers a lg then makes an amplified copy to give the hg
  - Integrated shaper
  - Peaking time is adjustable over 2-bits
  - Trimmable termination (3-bits)
  - Sums of channels for trigger output



LAUROC and HLC performance

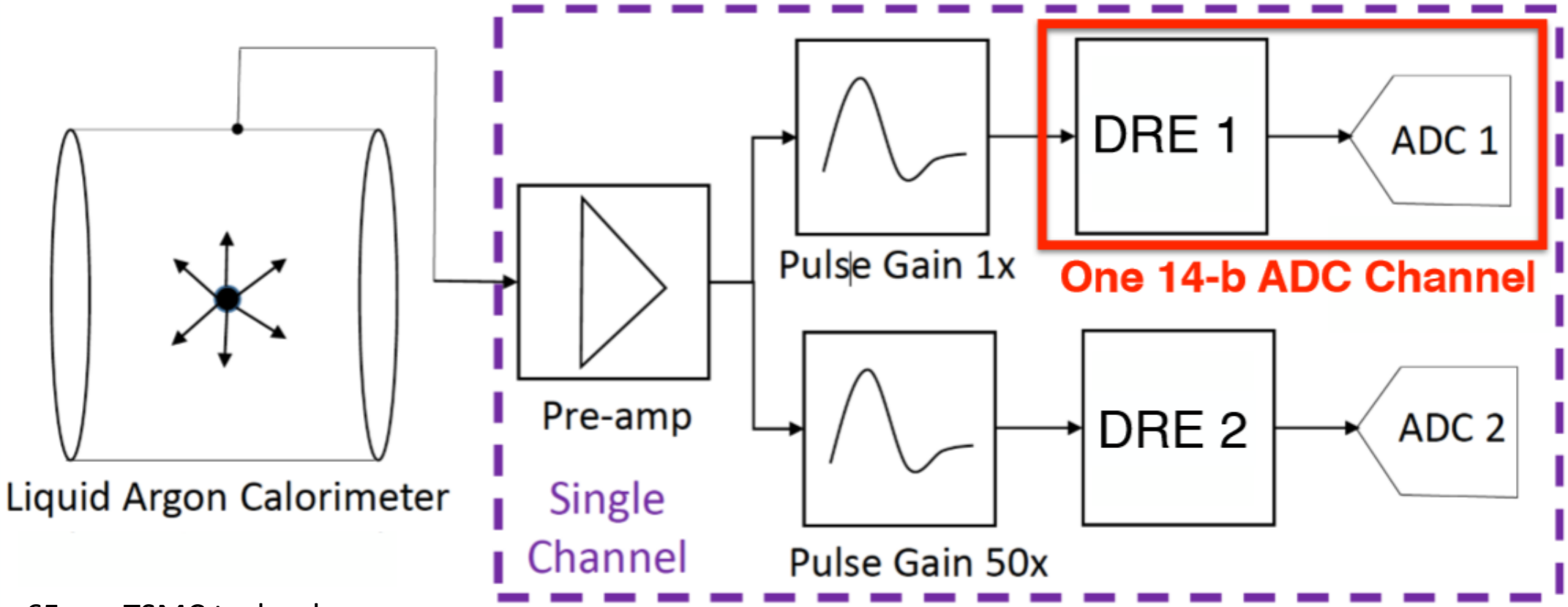
Term.	ASIC	Cdet	Gain (mV/mA)	RMS Noise (mV)	Noise with pa off (mV)	ENI (nA)	ENI after Sub. (nA)
25Ω	LAUROC0	1.5 nF	911	0.31	0.158	337	289
	HLC1	1.5 nF	909	0.27	0.135	300	261
50Ω	LAUROC0	330 pF	5300	0.54	0.150	102	98
	HLC1	330 pF	3966	0.40	0.135	102	86

- LAUROC0 noise 10% higher than HLC1
- Will be reduced by ≈30% in next iteration

- HLC1 and LAUROC0 non-linearity within specs
- Some range limitations for LAUROC0, understood and will be corrected for next iteration

- Submission planned in 130 nm CMOS (PA+Shaper) in September 2018
- Final technology choice will be done early 2019

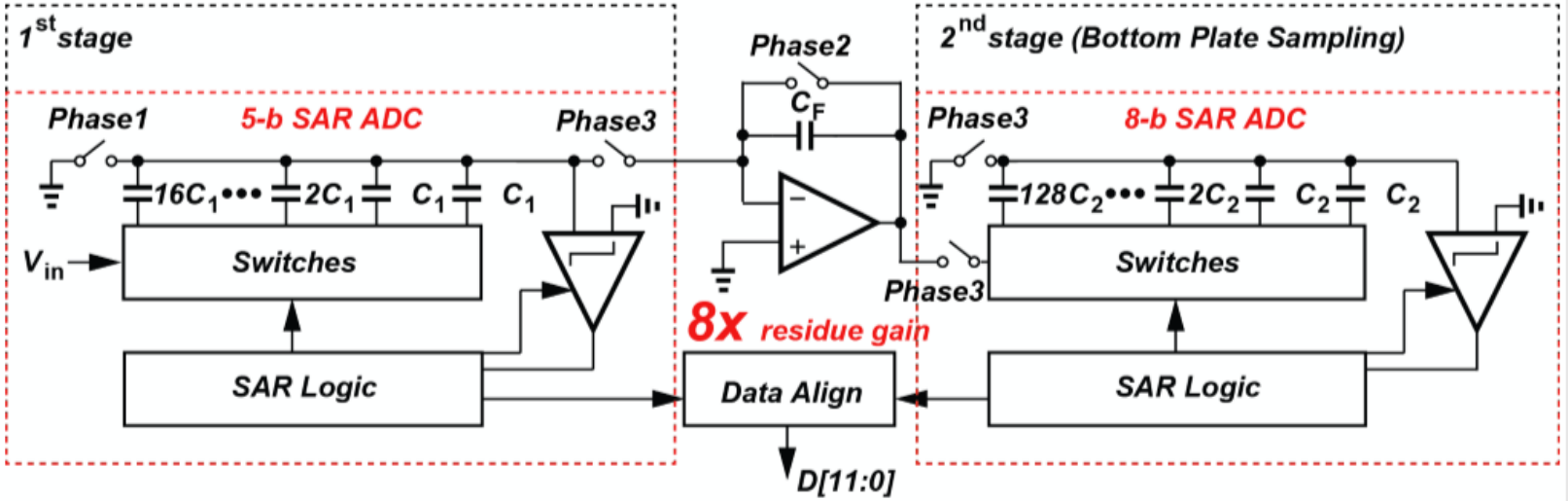
In-house 14 bit COLUTA ADC design

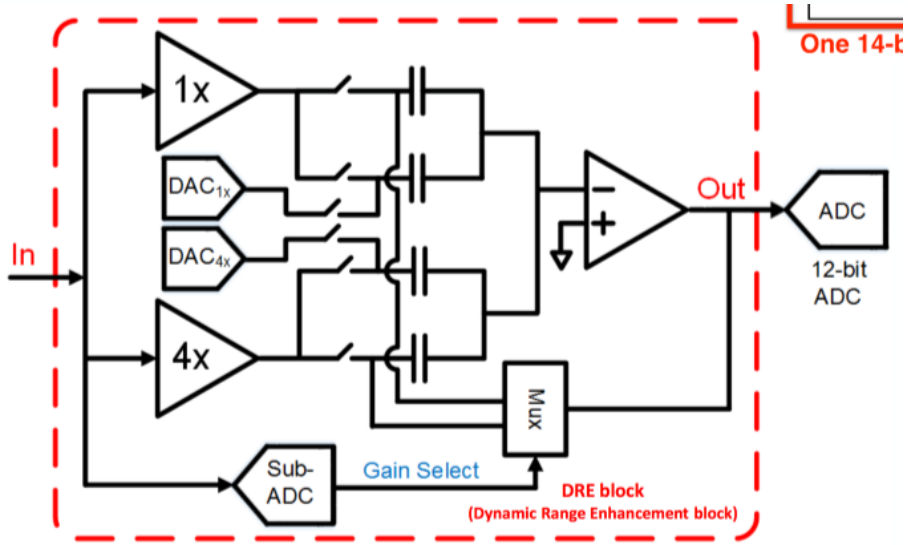


65 nm TSMC technology

Effective 4 gain system, can be considered as 2-gain if DRE well calibrated

COLUTA SAR and DRE design





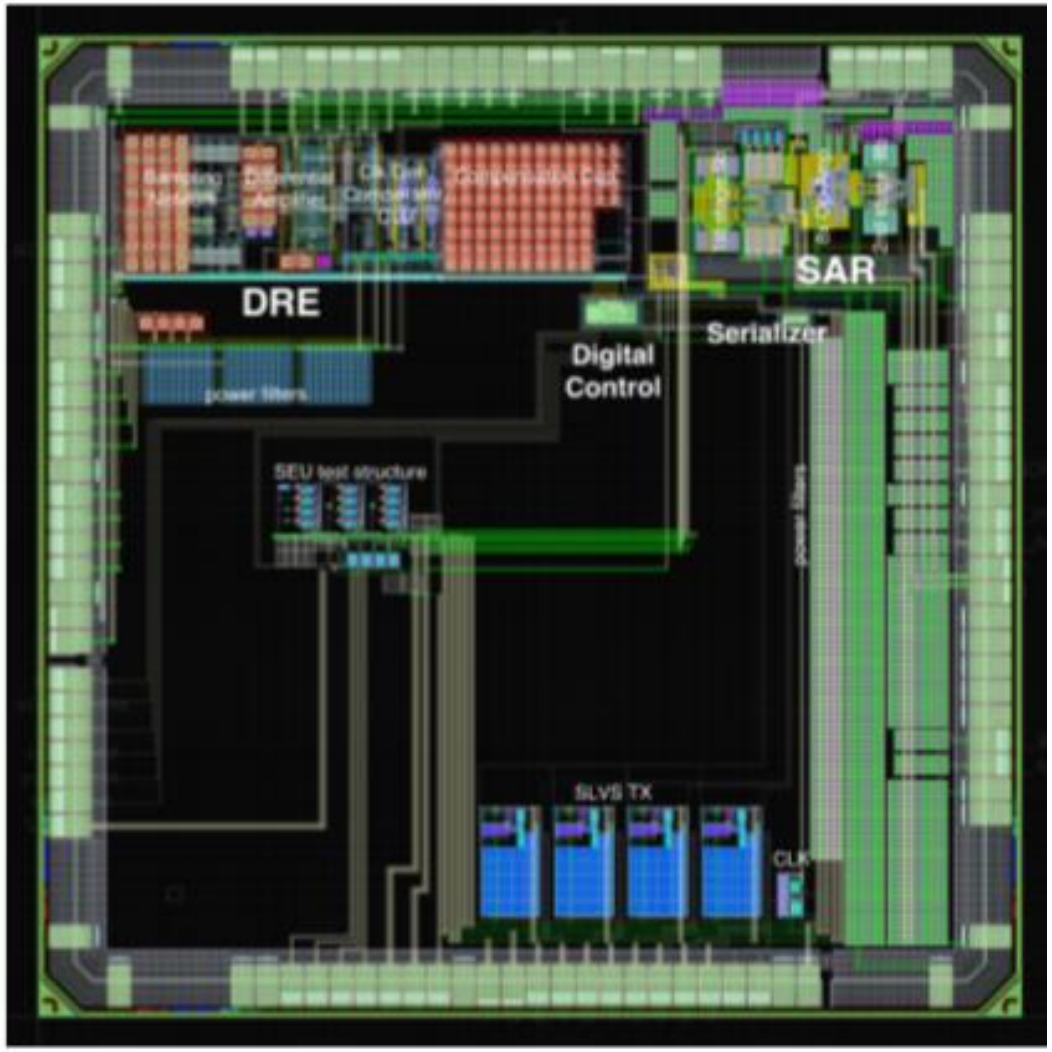
- **SAR design**
- 40 MHz, two step design (v1):
  - 5-bit first stage + 8-bit second stage with 1-bit interstage redundancy
- Improved design in progress (v2):
  - 6-bit first stage+10-bit second stage, with 2-bit interstage redundancy
- Designed to be able to run at 80 MHz to have some margin

- **DRE concept**
- Need to resolve 2 bits:
- Internal gain selection (g=4) with 12-bit accurate output for sampling

COLUTA test chip design and submission

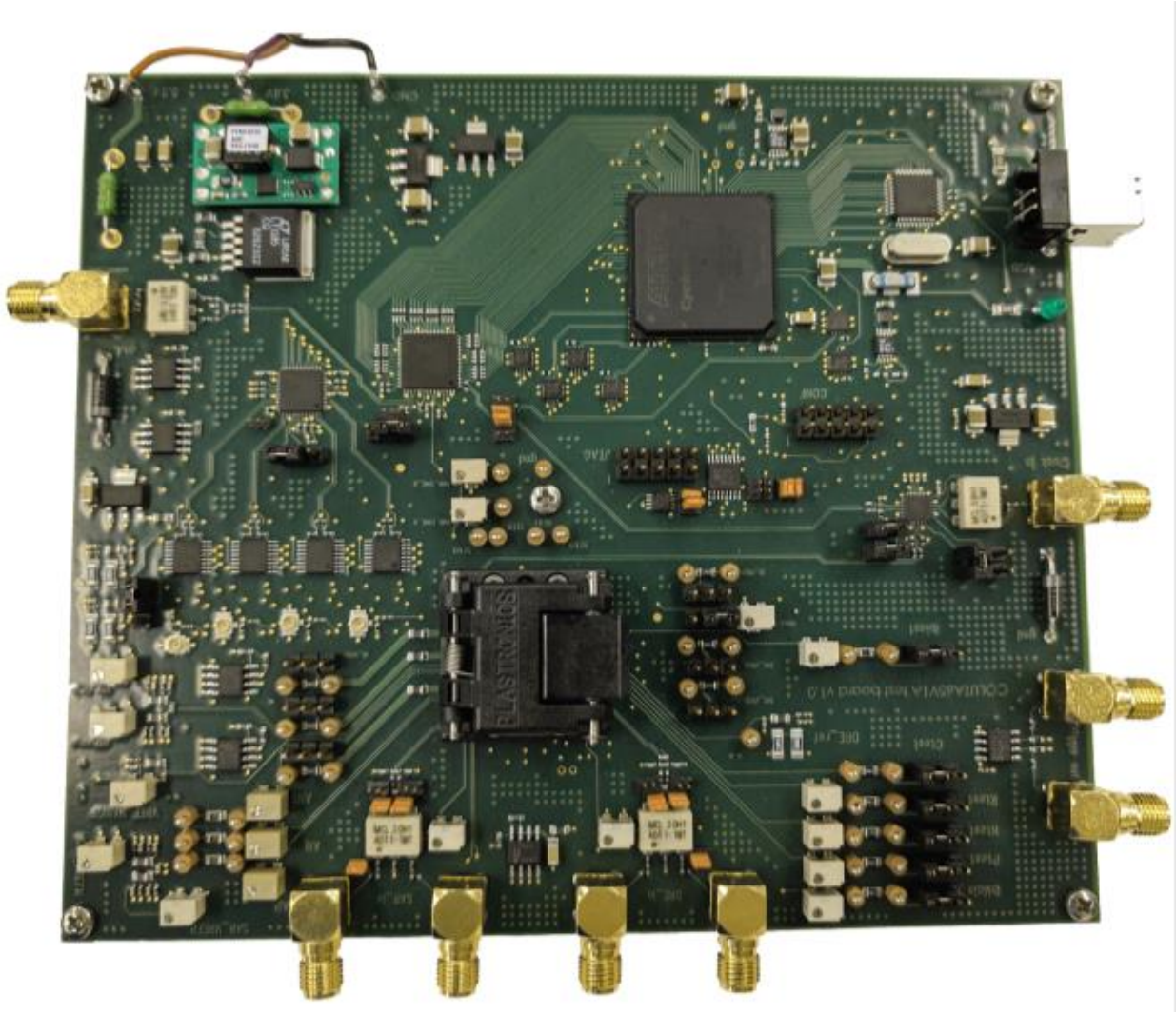
- First test chip (COLUTA651A) submitted May 24 2017

- ADC blocks (DRE, SAR) + Serializer, digital control, SLVS
- 2 mm × 2 mm
- QFN 72 package
- Received September 15 2017

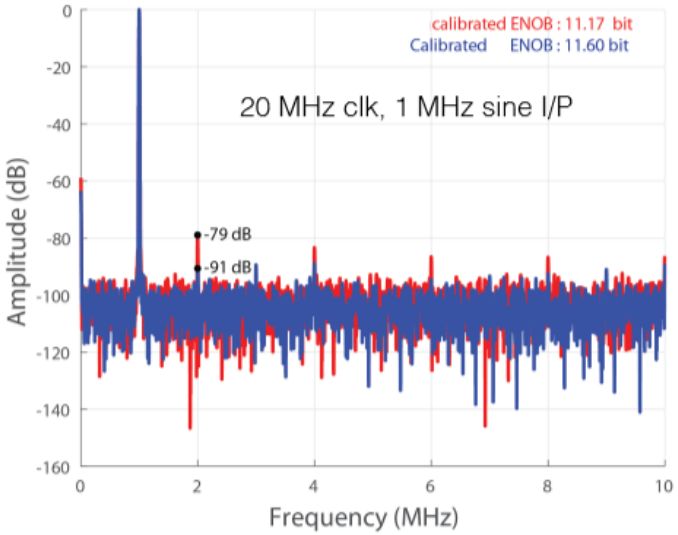


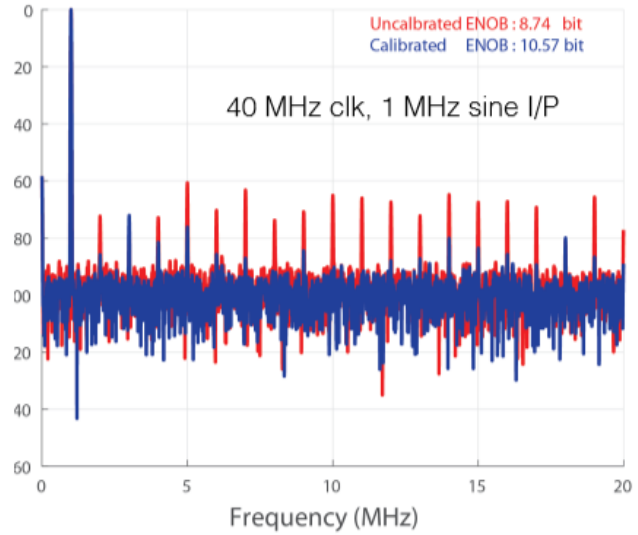
COLUTA test board

- Socket mounted chip, or directly soldered
- Various test modes
- Digitize DRE analog output with 16 bits commercial ADC on board
- Read out SAR, either direct input or through DRE
- SEU test structures
- Measured 12.7 ENOB on 16 bits commercial ADC with a sine wave signal.

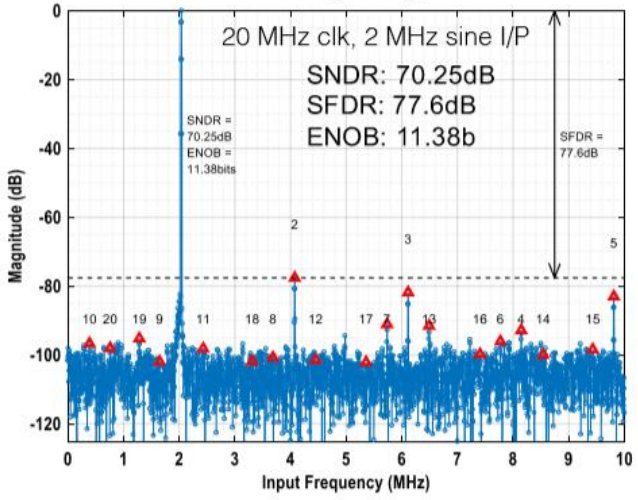


Building blocks performance

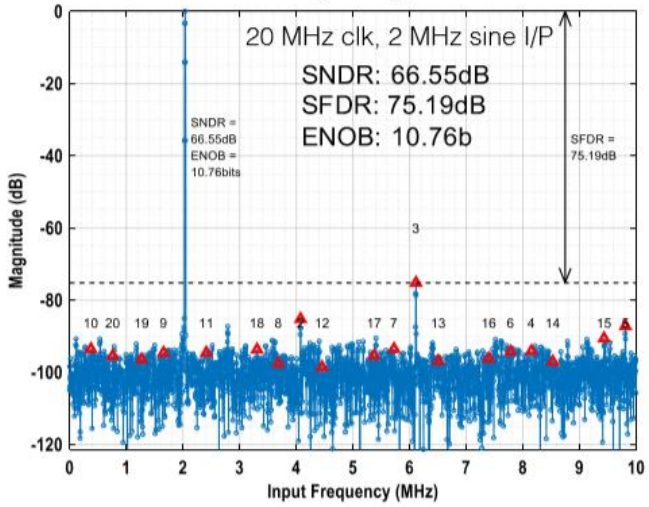




1x Gain, 1.6 Vpp



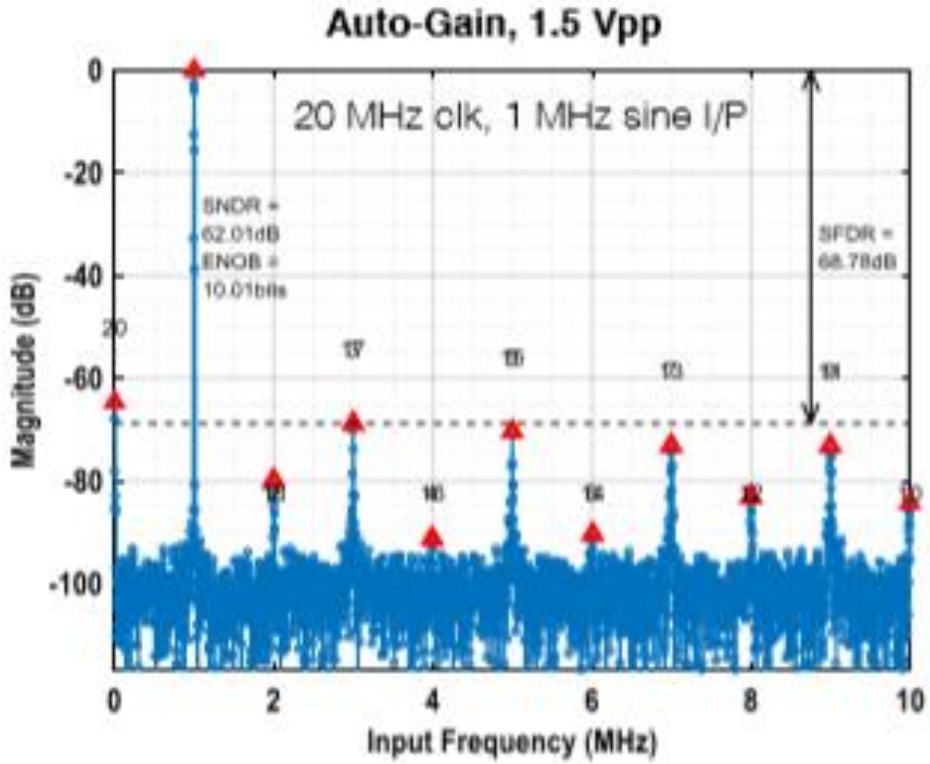
4x Gain, 0.3 Vpp



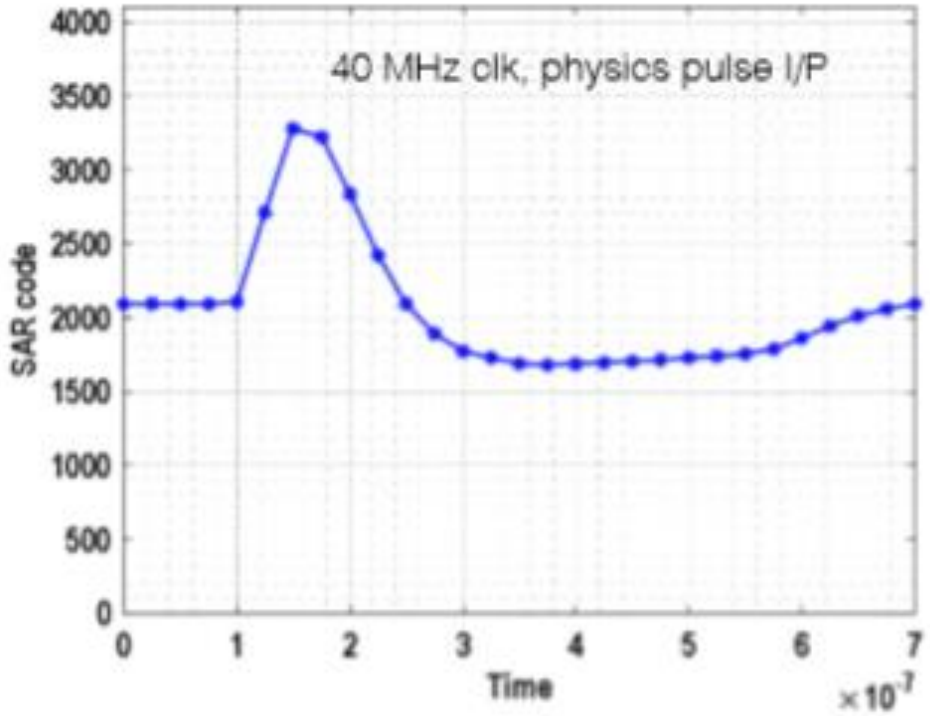
- SAR preliminary results with 20 MHz clock show good performance
- Improved by calibration
  - Investigating capacitor matching specification
- With 40 MHz clock performance is degraded
  - Confirmed in simulation
  - Dependance on digital and analog supply voltage observed, following up as possible solution

- DRE tested with commercial ADC, 1× and 4× gain channels separately
- Testing with 20 MHz clock shows good performance of each channel separately,

DRE+SAR testing



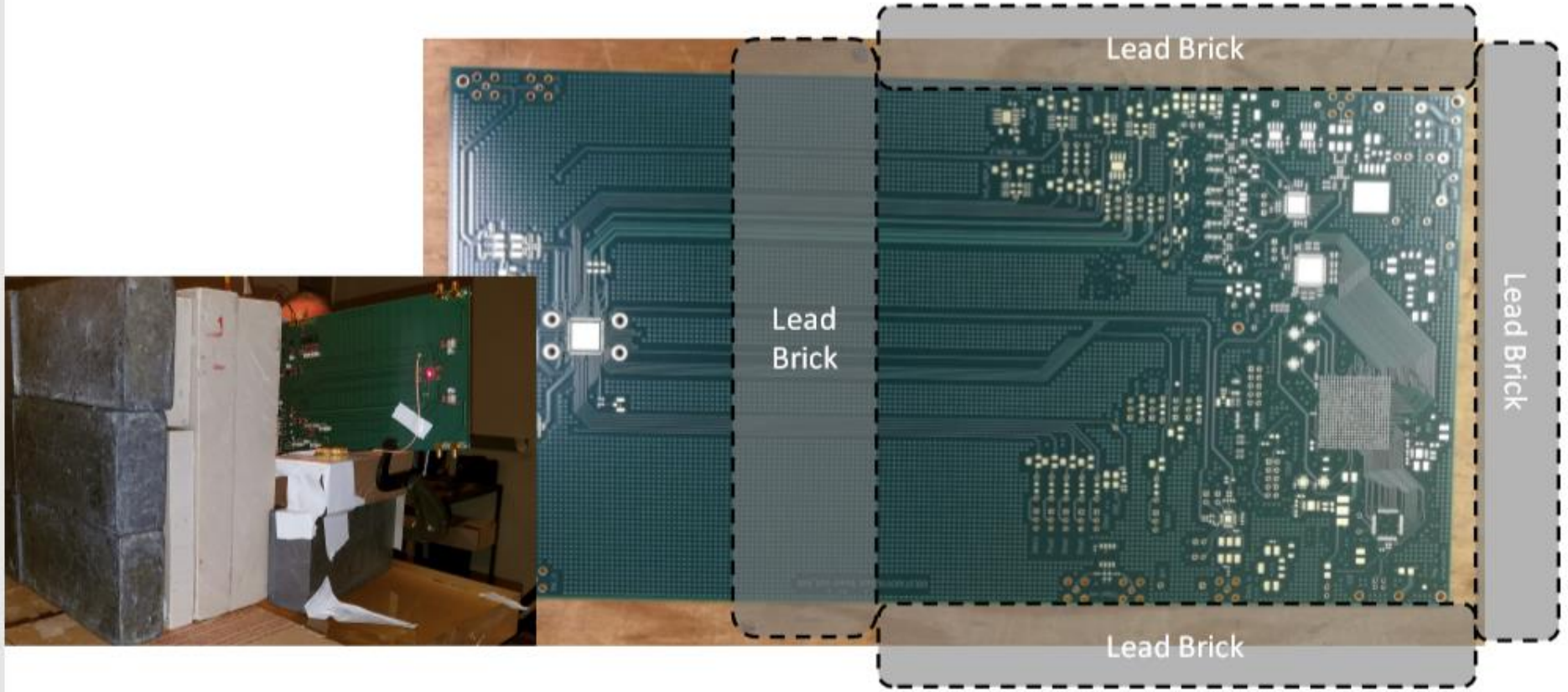
- DRE O/P to SAR ADC, Auto-Gain (automatically choose 1x or 4x) tested.
  - SAR calibration applied



- Simulated physics pulse from AWG with 40 MHz sample (auto-gain).
- Jitter of AWG triggering and of overall setup measured (on oscilloscope) to be ~20-30 ps

COLUTA first irradiation test

- First test of COLUTA ADC in Mass. General Proton Beam **October 28 and 29**. **2017**
- Irradiated 4 specialized boards up to ~0.9 MRad.
- Tested TID, $n_{protons}/cm^2$, and SEU/SEE.



Radiation test results

TID

Compare ENOB before/after irradiation (no calibration applied)

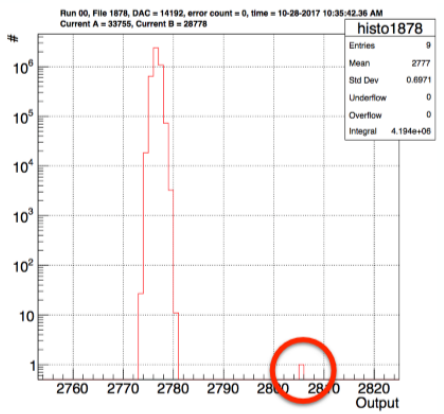
650 kRad

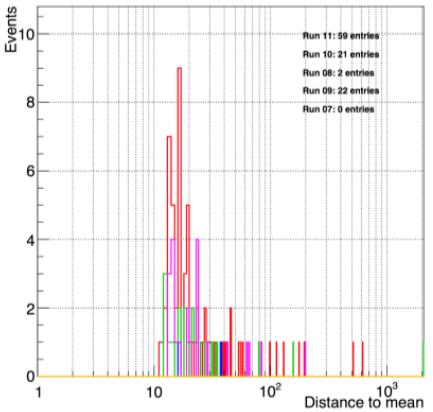
Board 2-3	2 MHz			5 MHz		
	ENOB (b)	SFDR (dB)	SNDR (dB)	ENOB (b)	SFDR (dB)	SNDR (dB)
Pre	10.55	76.77	65.24	10.5	74.46	64.97
Post	10.5	74.92	64.99	10.25	70.01	63.48

SEUs/SEE

Board 1-1	Rate (p/cm²/s)	Effective time (s)	SEU CUT	SEFI	Digital Error Counter	Scan chain error	Cross-section SEUs CUT(cm²)
Run 7	6.76E+08	15.4	0	0	1	1	-
Run 8	6.04E+08	281.6	2	0	0	0	1.18E-11
Run 9	2.80E+09	455.18	22	0	0	0	1.72E-11
Run 10	3.34E+09	339.24	21	0	1	0	1.85E-11
Run 11	6.52E+09	559.02	59	0	2	0	1.62E-11

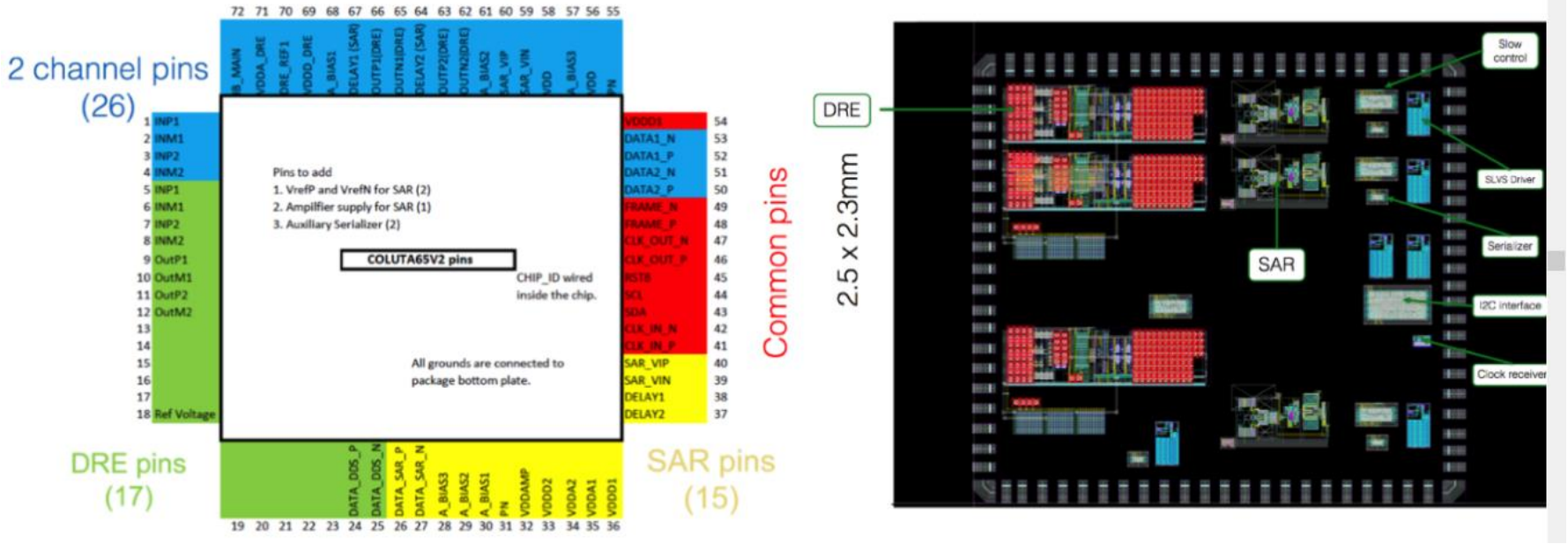
SEUs tagged by histogramming ADC output during a slow ramp





Next COLUTA (v2) iteration

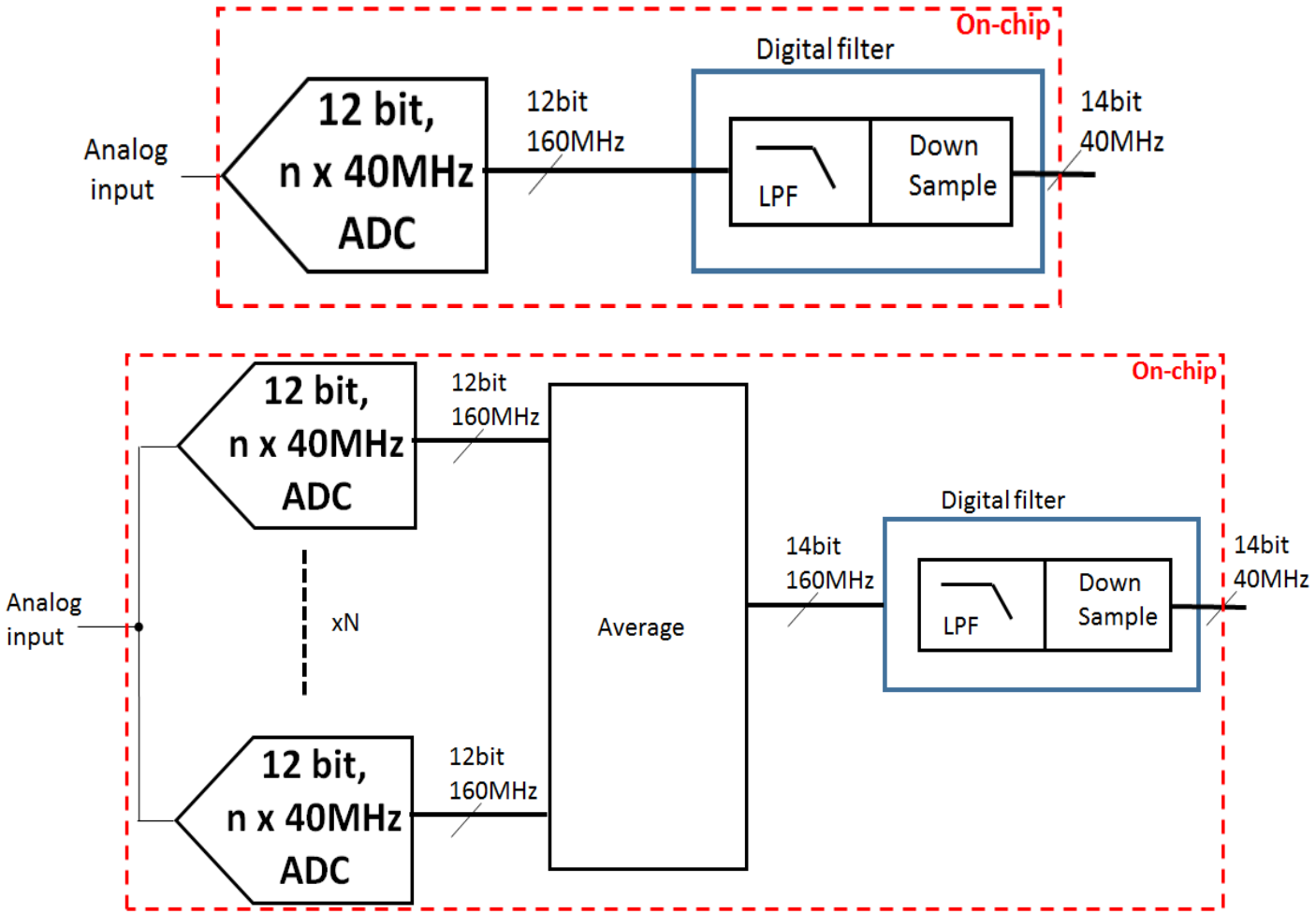
Submission in May 2018
Two-channels design
ePort interface with lpGBT chips : 16 bit, 640 MHz (16 ADCs to 11 lpGBTs)
Three readout formats : Calibration, Raw, Normal (calibration applied)
Use of 40 and 640 MHz clock from lpGBT (no PLL)
New serializer at 640 MHz



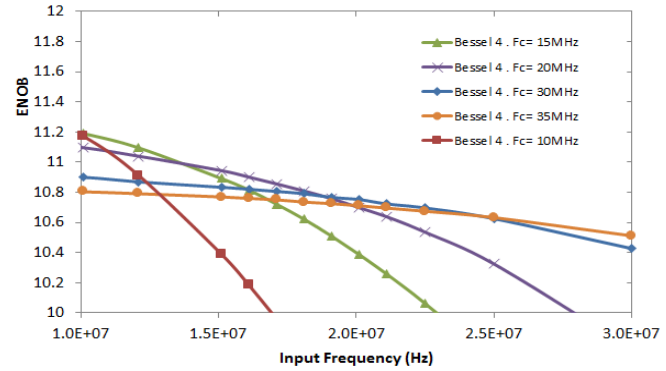
COTS ADC or IP ADC

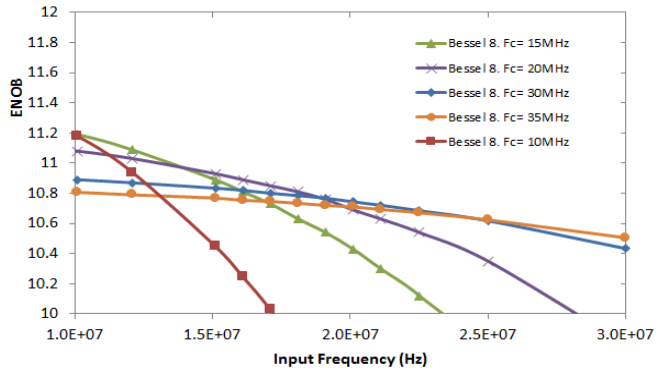
- Some COTS ADC have been evaluated under irradiation
- Radiation tolerance of Texas Instruments ADS5294 promising (Octal 14 bit ADC, 180 nm technology, 1.8V, 60 mW/channel at 40 MSPS)
- Hardening design w.r.t. SEU would be too expensive
- Using an ADC IP is an intermediate solution between COTS and in-house design
- Combines expertise of ADC industrial designers with possibility to configure design to ATLAS needs
- Hard to find 14-bit low power 40 MSPS IP, 12-bit higher speed easier
- →CMS 12 bit IP (10.6 ENOB) a good candidate, to be complemented with digital filtering to reach 14 bits (12 bits ENOB)

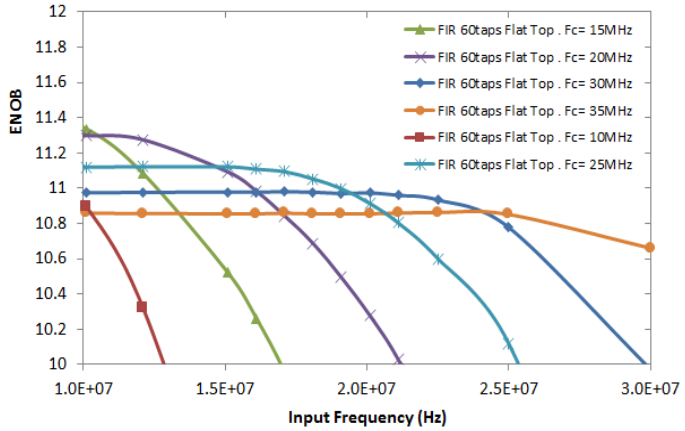
Architecture of possible 14 bit ADC based on 160 MHz ADC IP block

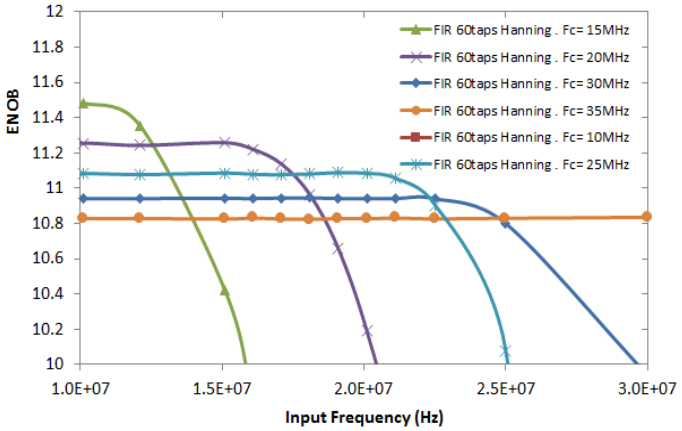


ENOB evaluation on sine waves





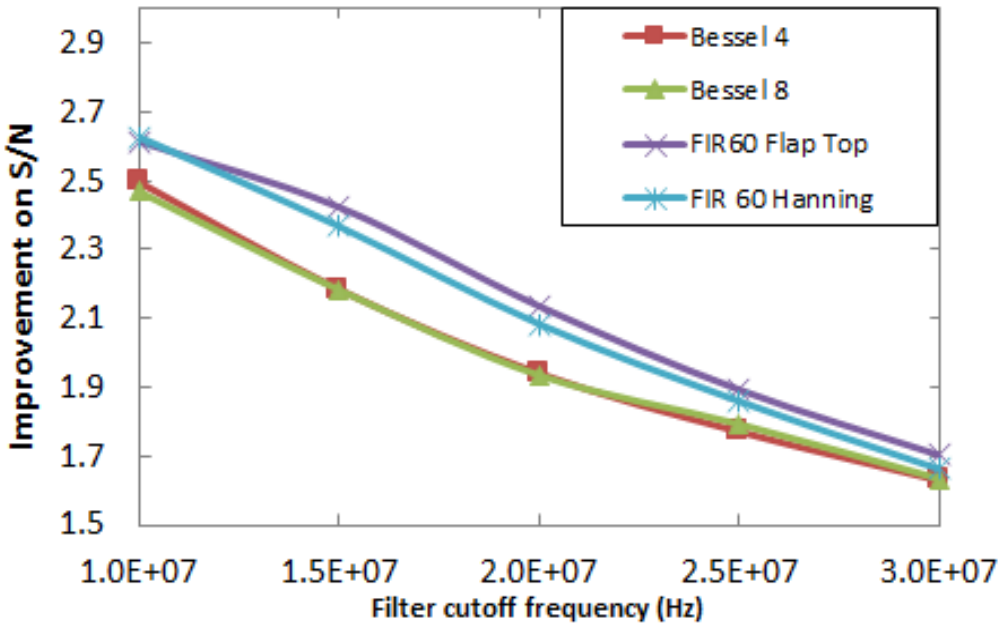




- Simulate sine waves of varying frequency, Vpp=4096 LSB, add 1 mV RMS white noise
- Gain is 1 bit with Bessel filters at low frequency, and gain is lower at high frequency.
- Increasing filter order improves a bit at high frequency
- FIR filters behave better at high frequency (due to better sharpness of spectral response)
- Can gain 1.1 bit ENOB with ×4 oversampling, up to 15 MHz
- Can gain 1.4 bit ENOB with ×6 oversampling (240 MSPS), up to 15 MHz

Simulation with calorimeter signals

Measure signal over noise improvement after filter



- S/N is improved by more than 2
- Can be improved up to ×2.5 (1.3 bits)
- FIR filters a bit better than Bessel

- ×4 oversampling + digital filtering after 12 bits/10.2 ENOB ADC allows to gain more than 1 bit ENOB
- Specific case : 60-taps FIR, flat-top, Fc=15 MHz gains 1.3 bits 10.2 goes up to 11.5
- Could gain 0.7 to 1 additional bit by averaging several ADCs running in parallel, if power consumption allows

ADC development plans

- COLUTA
  - Next submission planned in May 2018
  - One iteration per year until 2020
- IP ADC option
  - Use CMS test chip (under development) to evaluate actual performance of IP
  - Digital filtering implemented on FPGA to check ATLAS performances can be reached (mid-2019)
  - If evaluation is positive, reuse CMS IP to design an ATLAS chip

Conclusions

- Developments are building upon experience gained with present systems
- Need to maintain present physics performance with high pile-up
- Analog processing based on similar designs as present systems
  - Newer technologies
  - More integrated, less power-hungry
- Challenging ADC designs needed, several options pursued