Overview of the Calorimeter Readout Upgrades

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on behalf the ATLAS and CMS Calorimeter Upgrade Groups

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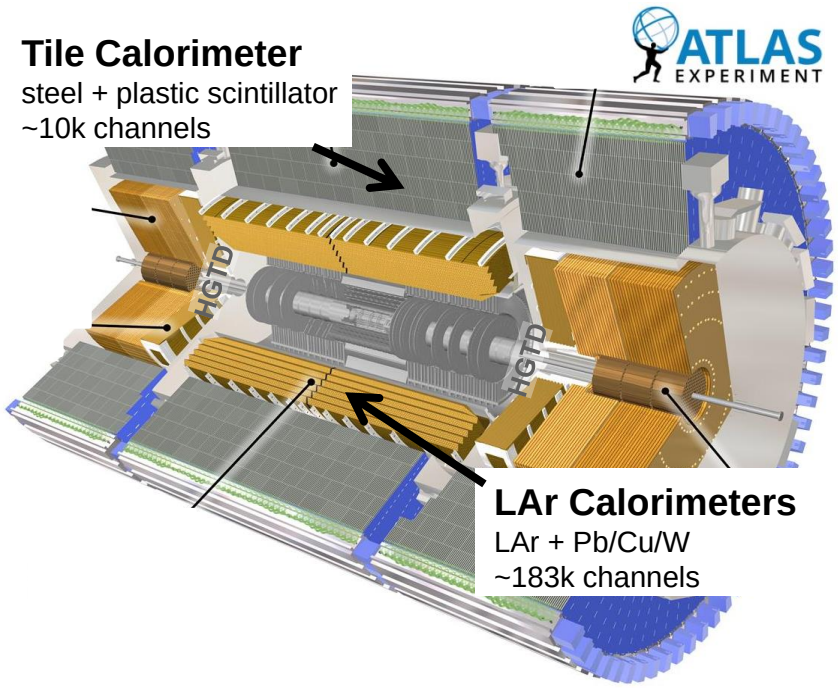
FIS ATLAS

PHYSICS AT THE TERA SCALE Helmholtz Alliance

ACES 2018
CERN
April 24-26, 2018

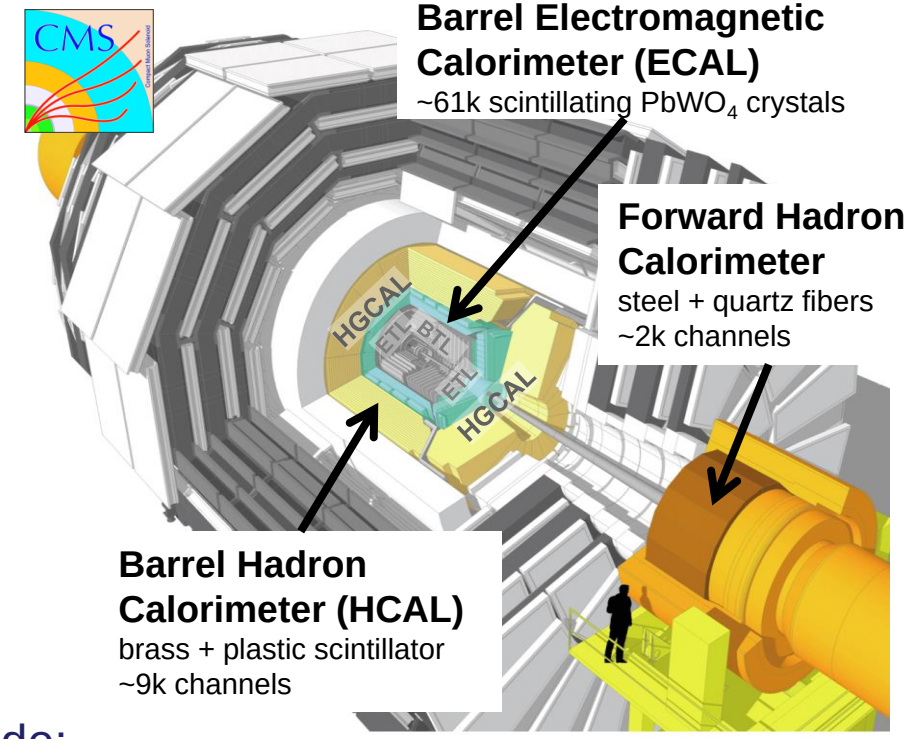
General Concepts

Calorimeter Electronics Upgrades



Tile Calorimeter
steel + plastic scintillator
~10k channels

LAr Calorimeters
LAr + Pb/Cu/W
~183k channels



Barrel Electromagnetic Calorimeter (ECAL)
~61k scintillating $PbWO_4$ crystals

Forward Hadron Calorimeter
steel + quartz fibers
~2k channels

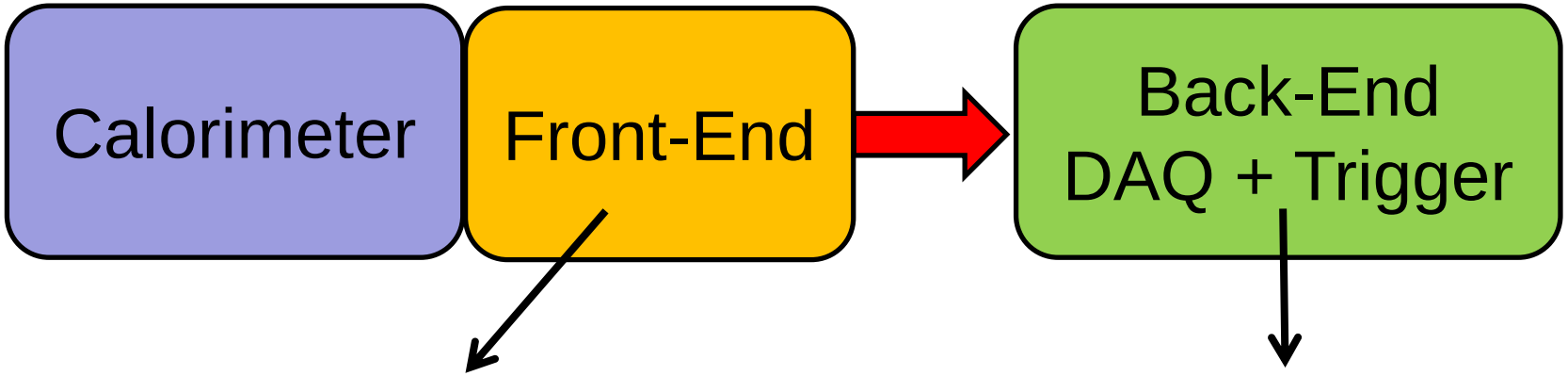
Barrel Hadron Calorimeter (HCAL)
brass + plastic scintillator
~9k channels

- Motivation for calorimeter electronics upgrade:
  - Higher trigger rate of 0.75 - 1 MHz and larger event buffers (> 10 µs)
    → improved trigger system for high pile-up
  - Improved radiation tolerance (2-10 kGy) and system longevity - where necessary
  - Improved timing measurement - where possible

- General concept: move buffers and pipelines off detector and read out at 40 MHz

- New additional timing detectors: Lindsay Gray Tuesday 16h30
- New CMS high-granularity endcap calorimeter: Paul Rubinov Wednesday 14h30

Ingredients



- Radiation tolerant ASICs and Commercial-Off-The-Shelf (COTS) components:
  - signal amplification and shaping
  - ADCs, TDCs
  - optical links with 5-10 Gbps
- Trigger, Timing and Control (TTC) distribution
- Power distribution for HV and LV

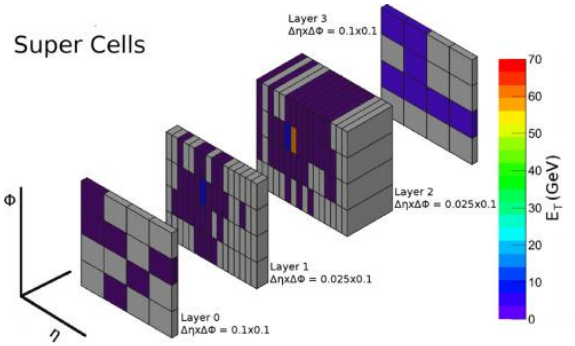
- High-bandwidth, low-latency signal processing with FPGAs
- Data buffering in FPGAs or on-board memory
- High-bandwidth interfaces to hardware trigger and to network based trigger/DAQ systems

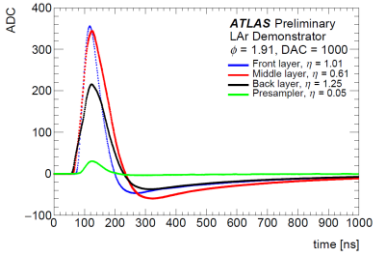
Phase-0/I Upgrades

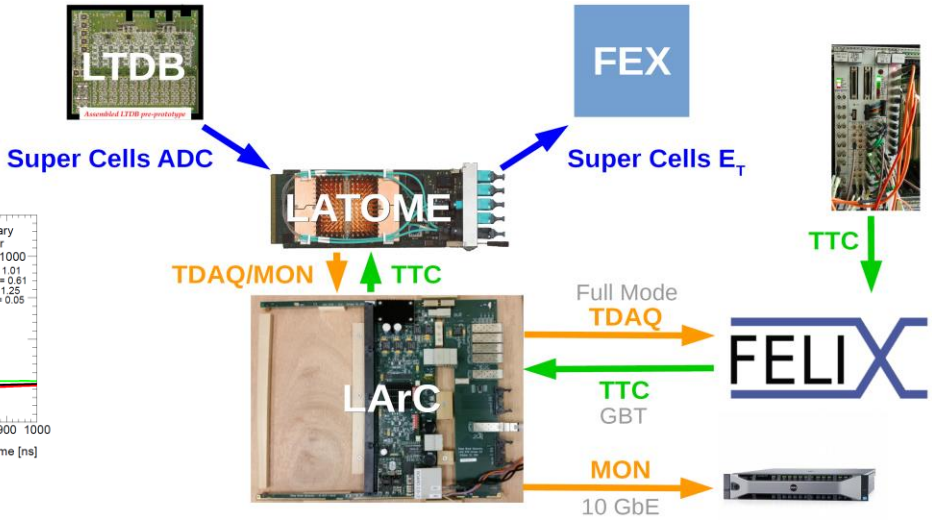
LHC Long-Shutdown 2: 2019-2020

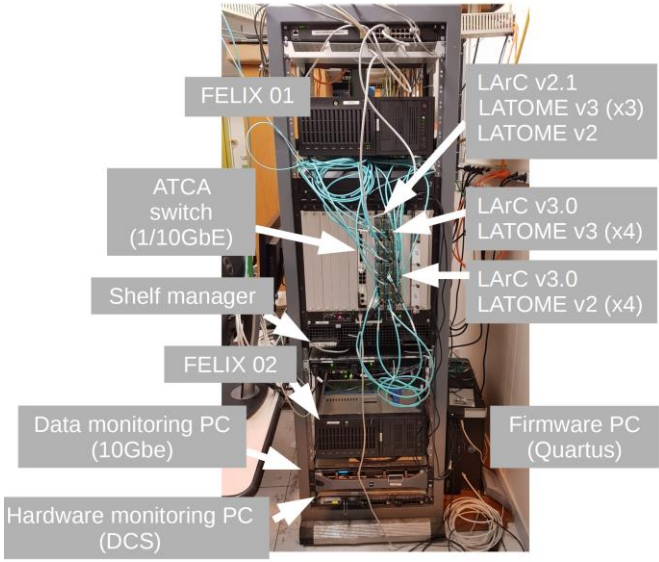
Phase-I Upgrades: ATLAS LAr Supercells

- 124 LAr Trigger Digitizer Boards on front-end to read out new supercell trigger primitives
  - COTS analog components
  - ASICs: 130 nm CMOS 4-bit pipeline + 8-bit SAR ADC, 250 nm Si-on-Sapphire link-on-chip
- 31 LAr Digital Processing Blades for signal filtering, energy calculation, data buffering
  - ATCA carrier blades equipped with 4 FPGA advanced mezzanine cards







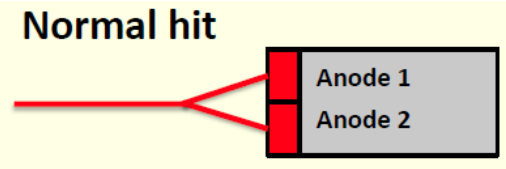


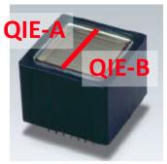
- Board production is being prepared - installation and commissioning in LS2
- Complex installation: removal of all front-end boards and installation of new baseplane
- System will remain during HL-LHC running

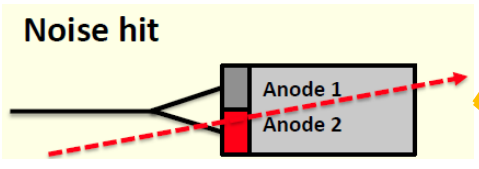
Phase-0/I Upgrades: CMS HCAL

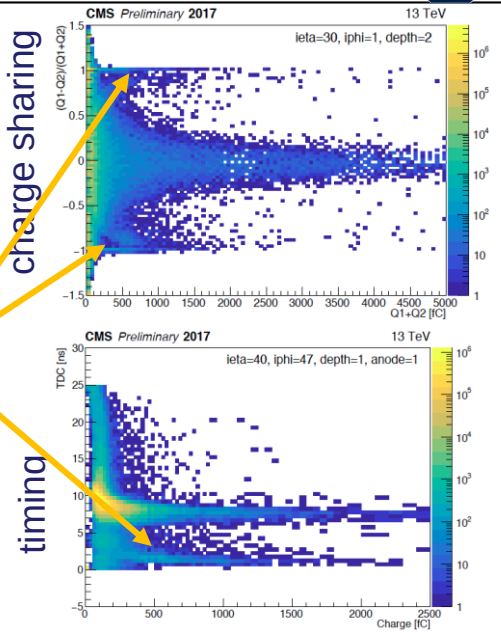
- Forward HCAL upgrade in LS 1 → reduce noise hits
  - new MAPMT
  - QIE10 (8-bit ADC 17 bit dyn. range, 6-bit TDC)
  - µTCA back-end

} stays for HL-LHC

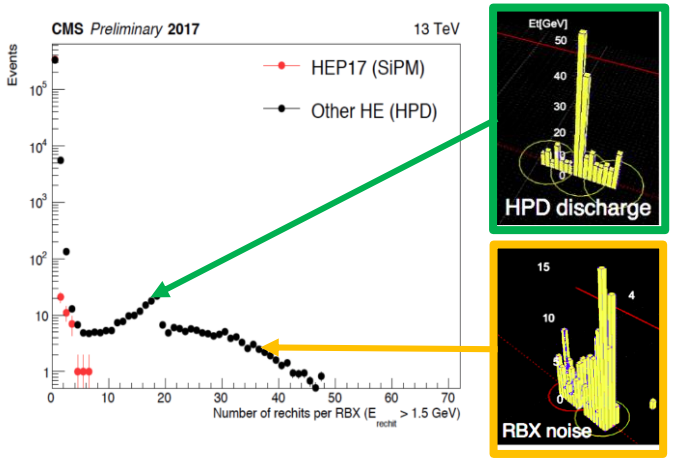


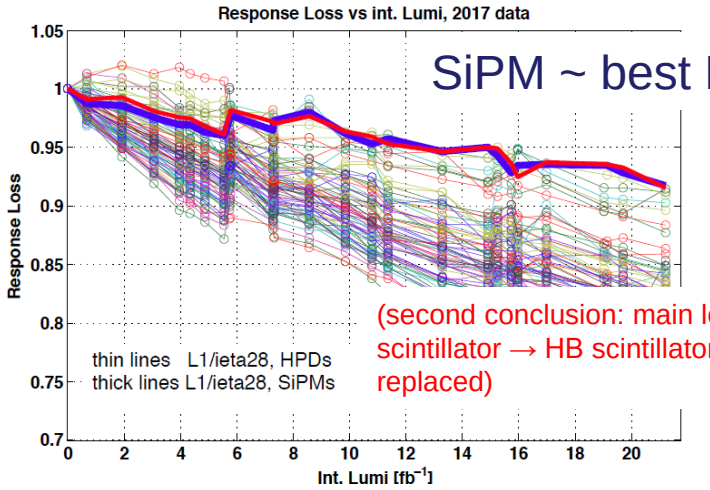






- Endcap HCAL → reduce noise and mitigate HPD damage
  - SiPMs replace Hybrid Photo Diodes (HPD)
  - QIE11 (programmable gain, low impedance)
  - demonstrator run in 2017 → full HE already upgraded in shutdown 2017/18





(second conclusion: main loss by HPD, not scintillator → HB scintillators will not be replaced)

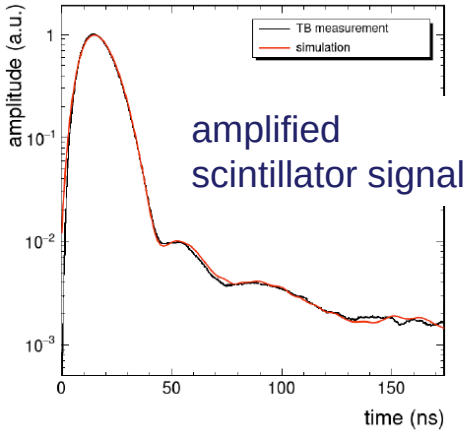
- full HB will be equipped in LS2
- HE will be replaced by HGCAL in LS3

Phase-II Upgrades

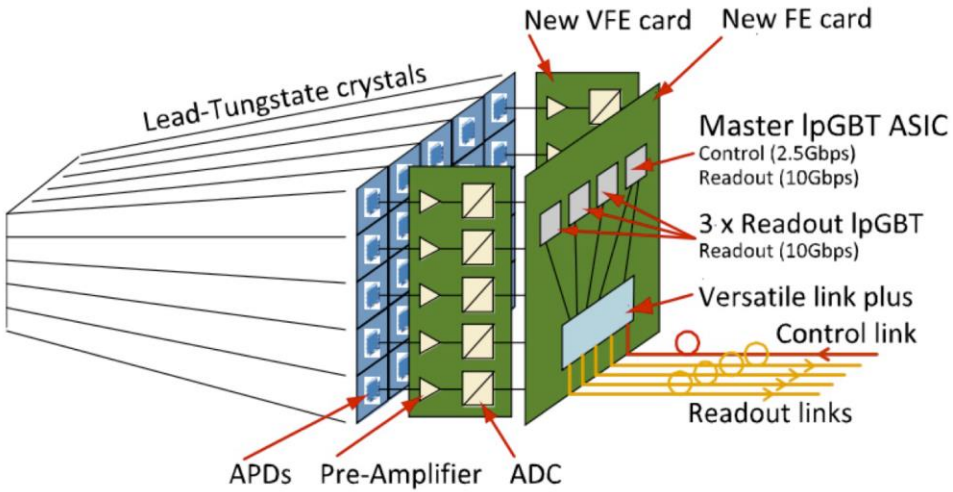
LHC Long-Shutdown 3: 2024-2026

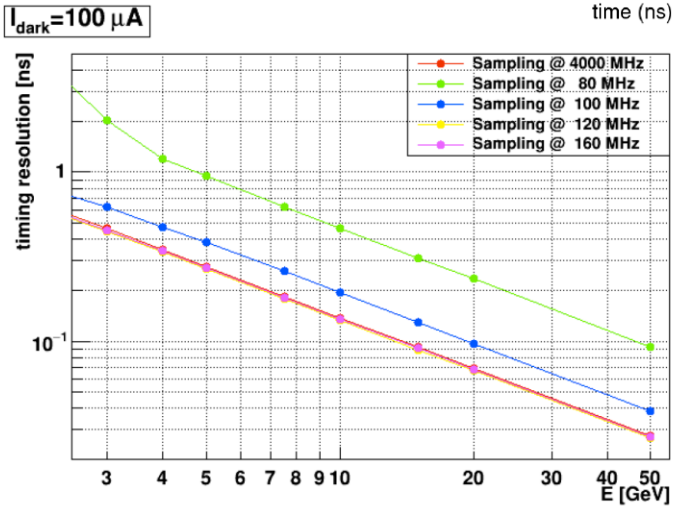
CMS Barrel ECAL Front-End

- APD light readout will remain, but new FE electronics
  - 80 MeV noise RMS; 50 MeV - 2 TeV dynamic range
    → 2 gains with two 12-bit ADCs per channel
  - 2‰ integral non-linearity
  - 30 ps electron time resolution @ 50 GeV and $\langle\mu\rangle$=200



- 12240 Very Front-End cards for 61200 channels





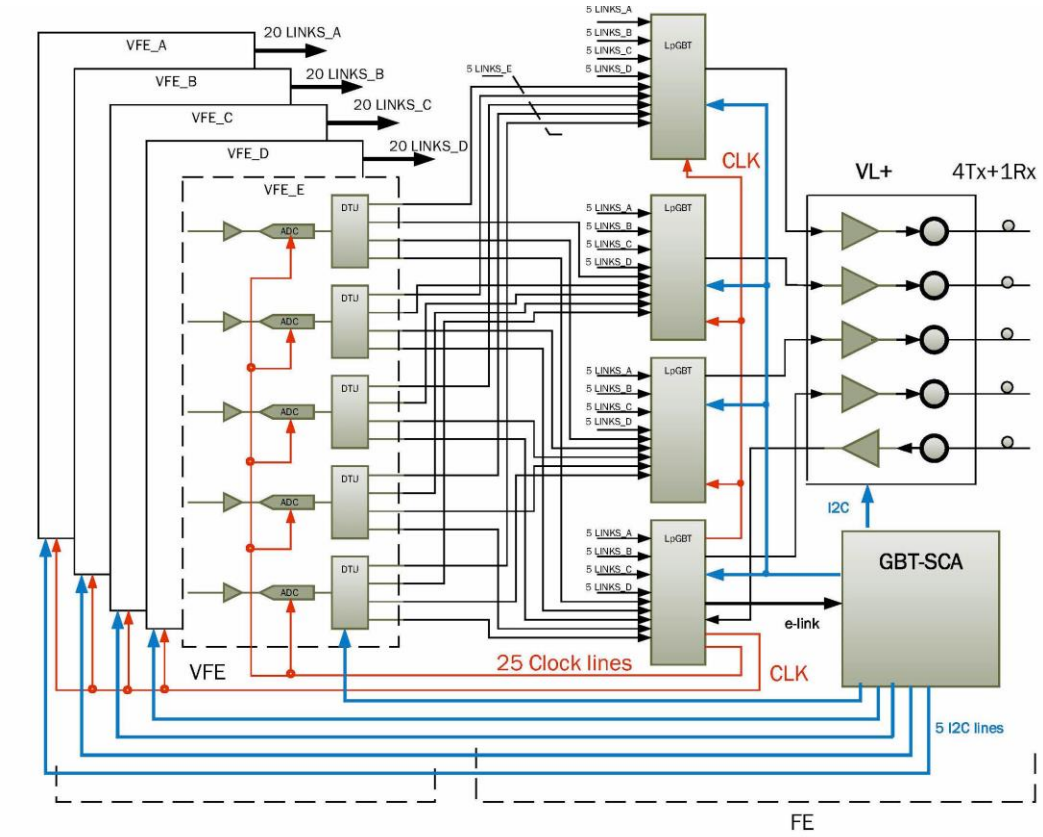
- Trans-impedance amplifier with low-pass in 130 nm TSMC:
  - about x3 improved timing resolution compared to CR-RC preamp-shaper (backup)

- ADC sampling rate 160 MHz optimal for time resolution and spike rejection
  - commercial ADC IP block integrated in dedicated ASIC in 65 nm TSMC

CMS Barrel ECAL Front-End

- 2448 Front-End cards transmit ADC data and distribute clock and control signals

- ADC data compression on statistical basis is being studied:
  - "long" data transfer for energies above ~6 GeV = 7 bit
  - only for a small fraction of events (10^{-4}-10^{-5})

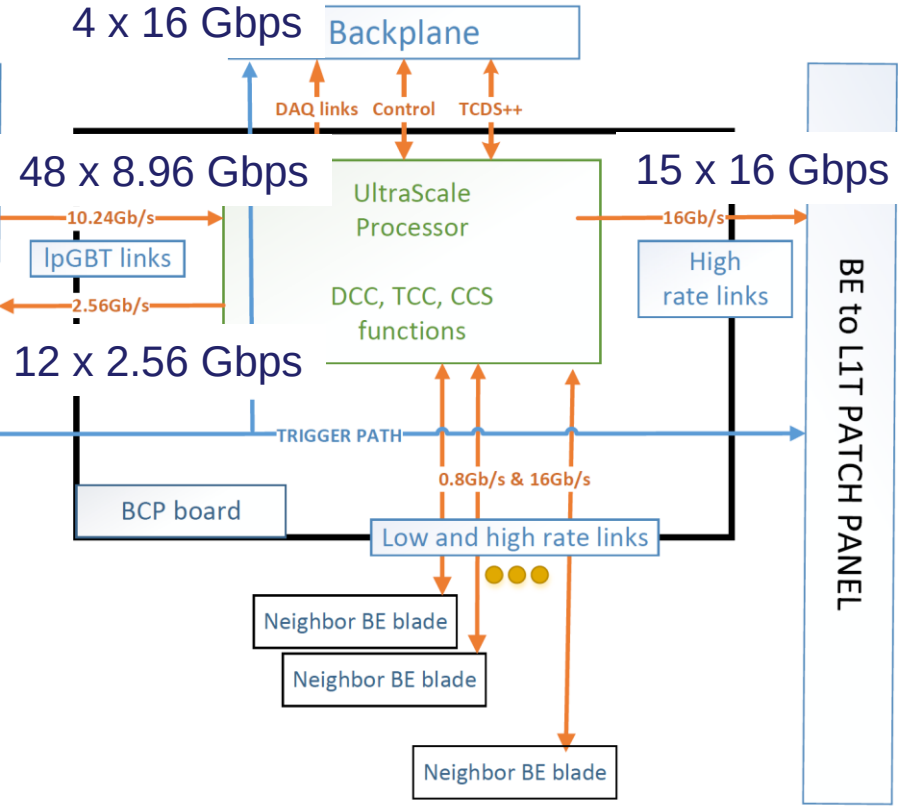


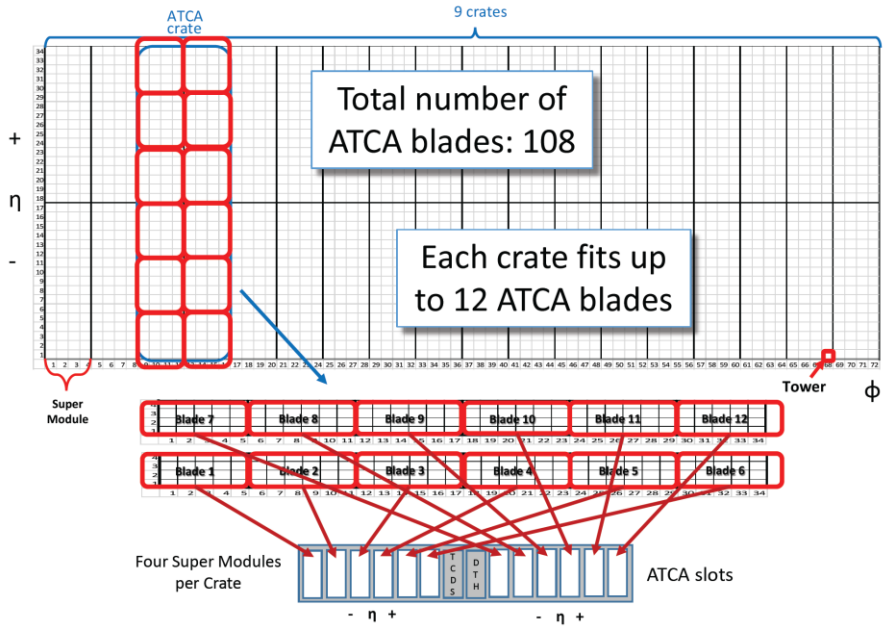
- Total data rate per FE card: 13 bit x 160 MHz x 25 = 52 Gbps
  → lossless data compression by factor 2 to fit into 4 x 8.96 Gbps = 4 lpGBT links

- Best compatible with 4 Tx + 1 Rx VL+ format

CMS Barrel ECAL Off-Detector

- Barrel Calorimeter Processor (BCP):
  - transverse energy calculation
  - trigger primitive preparation:
    - single crystal or cluster
  - anomalous pulse spike rejection
  - TTC distribution to/from FE



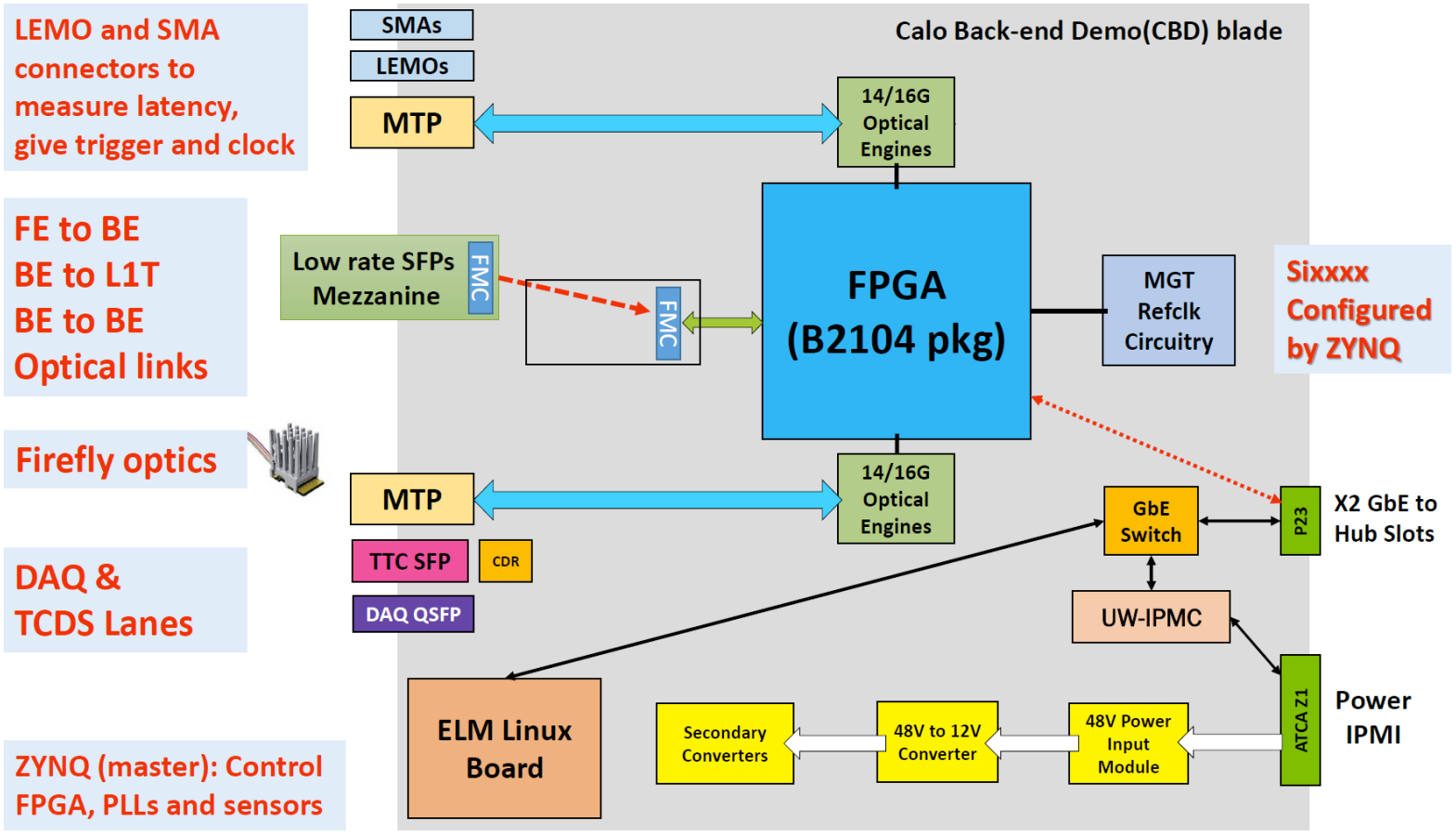


- 2 FPGAs per BCP
- 300 crystals per FPGA
- 15 x 16 Gbps for L1 trigger primitives (10 bit E_T, 1 bit spike, 5 bit time per crystal) → 3060 trigger links total

- 43 kb / event for crystal readout with 20 samples + 8 kb / event for trigger primitives
- total DAQ bandwidth 4 x 16 Gbps / FPGA

CMS ECAL Barrel Off-Detector

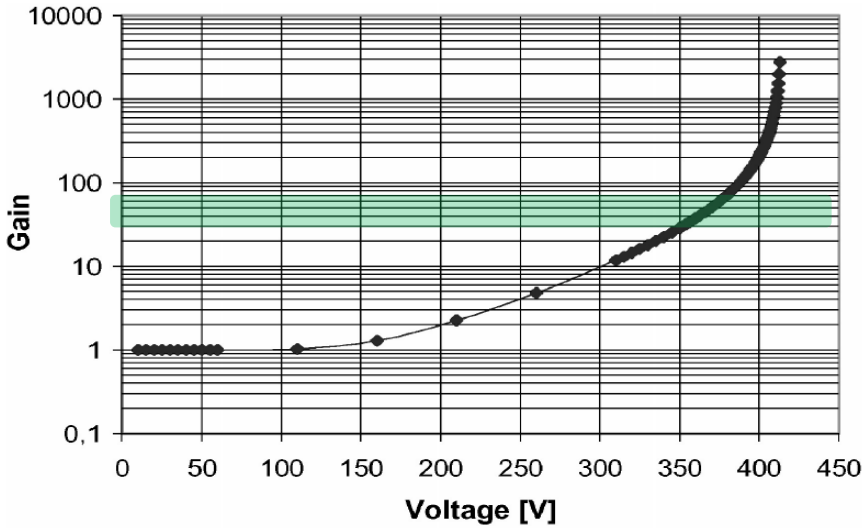
- BCP demonstrator:
  - ATCA blade with 2 Xilinx Ultrascale FPGAs and SAMTEC Firefly transceivers
  - 2 ZYNQ FPGA mezzanines for board control, ATCA system interface and Embedded Linux Mezzanine



CMS ECAL Barrel APD Power

- New HV system for APD to cope with radiation damage after 3000 fb^{-1}
  - increased dark current to 100 µA expected and possible shorts of APD pairs
  - increased bias voltage by +30 V necessary

Parameter	Legacy HV system	HL-LHC HV system
Output voltage range	0–500 V	0–600 V
Programmable setting step	1 mV	1 mV
External calibration	±20 mV	±20 mV
DC regulation at load	±20 mV	±20 mV
DC stability at load (over 90 days)	±70 mV	±70 mV
Low freq. noise at load (f < 100 KHz)	±20 mV	±20 mV
High freq. noise at load (f > 100 KHz)	±20 mV	±20 mV
Operating temperature at supply	15–40 °C	15–40 °C
Current limit	15 mA	20 mA
On and off ramp rate	2–50 V/s	2–50 V/s
Current measurement (from 1μA)	5%	5%



CMS Barrel HCAL

- 36 readout boxes x 252 channels = 9072 channels
- 36 x 32 optical links at 5 Gbps → 18 ATCA Barrel Calorimeter Processors (BCP)
  - 2 FPGAs per BCP prepare trigger primitives and readout data

Table 3. CMS Phase-2 detector projected data links and event size summary.

subdet	FE daq links	FE trigger links	sub-event size	BE leaf cards	BE crates	DAQ links	notes
PxTk	1000	0	1.6	100	12	48	
SiTk	1500	13500	0.5	300	33	132	(7)
ECAL	8000	2000	1.2	100	12	48	(8)
HCAL	1000	1000	0.2	100	12	48	(8)
HGCAL	8000	8000	1.2	160	18	72	
DT	0	3000	0.1	60	8	16	(9)
CSC	0	600	0.2	12	2	8	(9)
GEM	500	1000	0.05	30	12	12	
RPC	1000	1000	0.06	40	5	20	
Other	1000	1000	0.1	20	3	12	
Total	25612	27500	5.0	922	117	416	

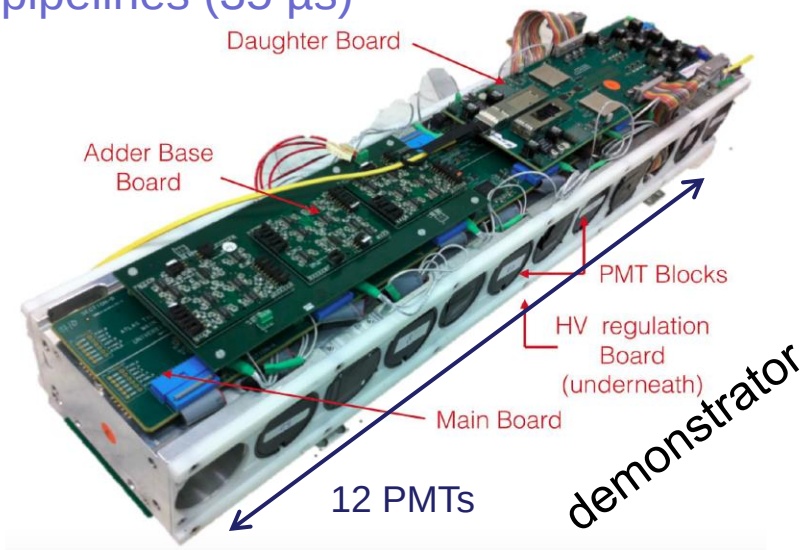
- What will happen with HB µTCA hardware?
  - Phase-I HB µTCA boards will be used in in ATCA adapter boards to equip the Forward HCAL (HF)

ATLAS Tile Calorimeter Upgrade

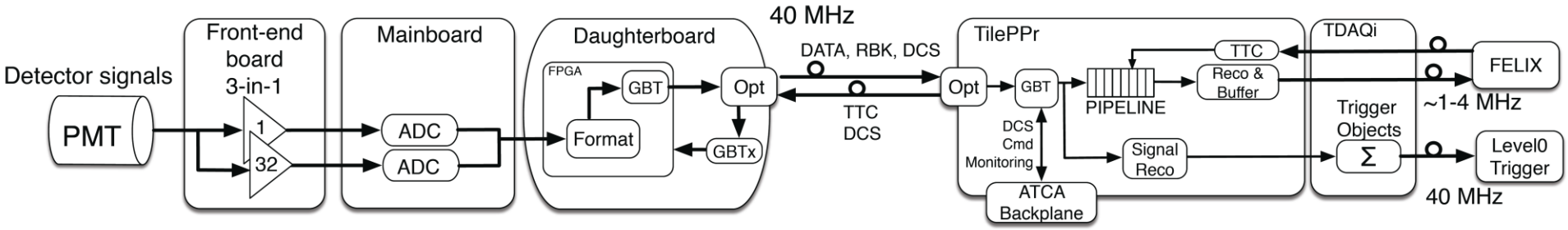
- Scintillator tiles will not be exchanged → upgrade of front-end and off-detector electronics to cope with
  - higher trigger rate (1-4 MHz), extended data pipelines (35 µs)
  - higher radiation levels

- New mini-drawer concept will allow better accessibility of electronics for maintenance

- Replacement of most radiation exposed PMTs
  - Hamamatsu R11187 more robust, higher quantum efficiency
  - 768 out of 9852 PMTs (8%) will be replaced

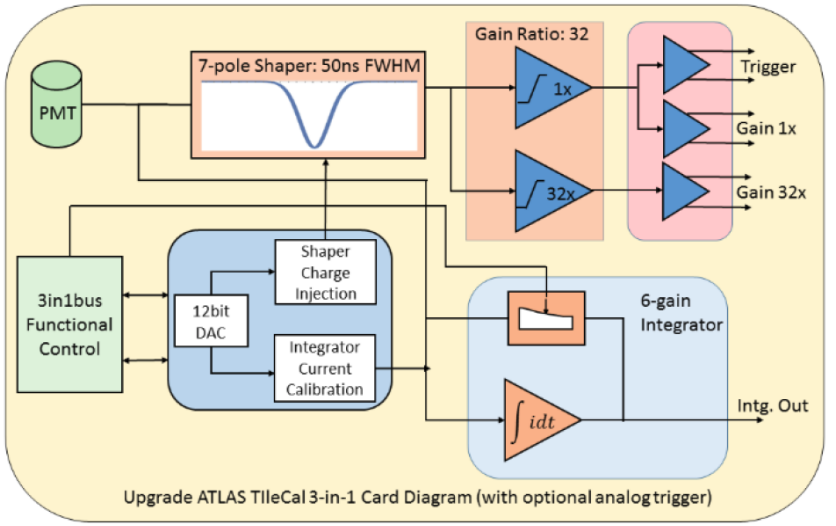


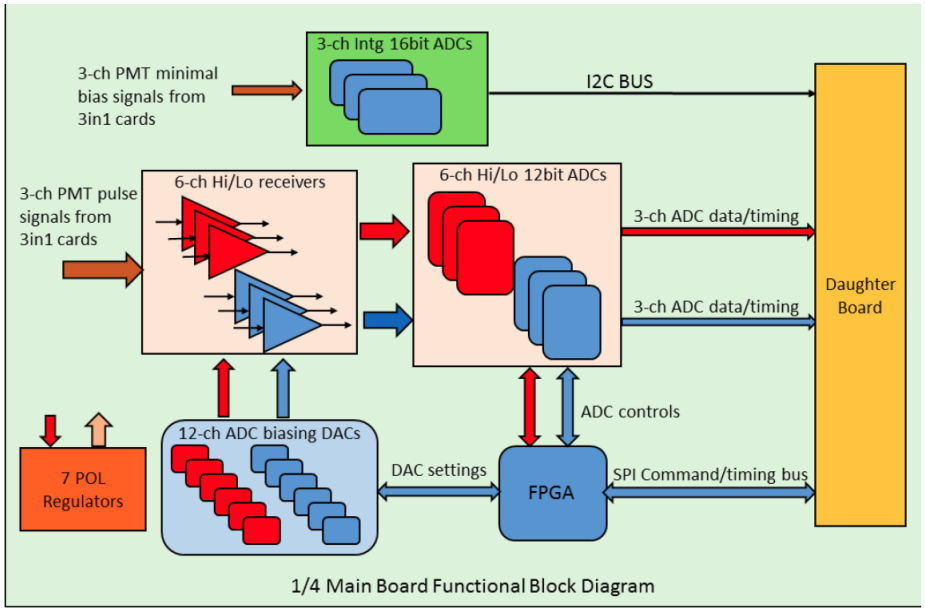
- Full calorimeter information will be read out at 40 MHz → full granularity trigger input

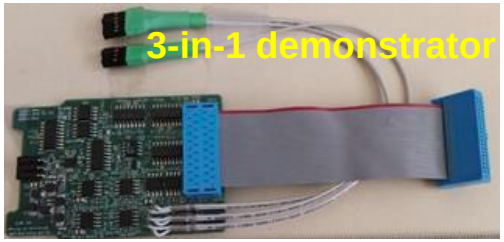


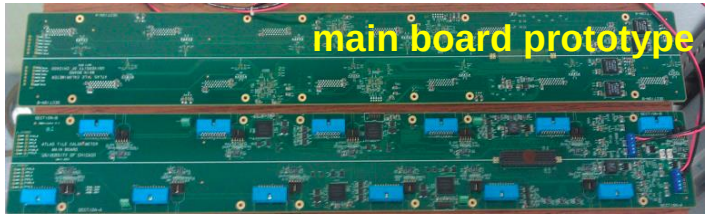
ATLAS TileCal: 3-in-1 Front-End

- Baseline: 3-in-1 front-end card on main board
- shaped and digitized PMT pulse for energy reconstruction:
  - 7-pole passive LC shaper
  - low-pass differential analog drivers
  - 2 gains for 17 bit dynamic range
- charge integration amplifier (10-21 ms) for Cs-source calibration and luminosity monitoring: digitized at 50 kHz with 16-bit ADC





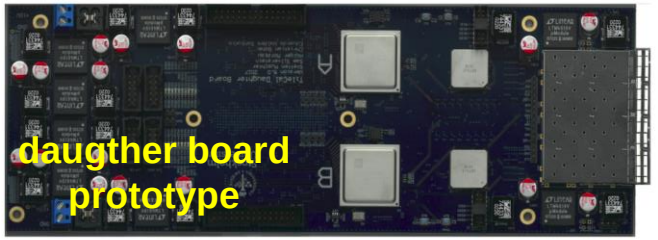


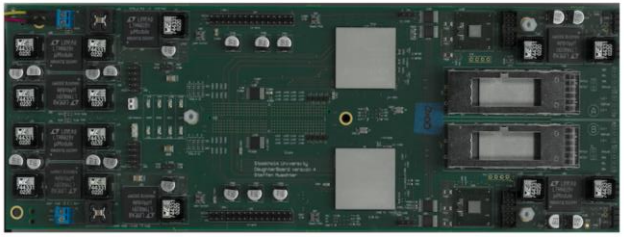


- Main board equipped with:
  - 12-bit COTS ADCs (LTC2264-12)
  - Altera Cyclone FPGA for control

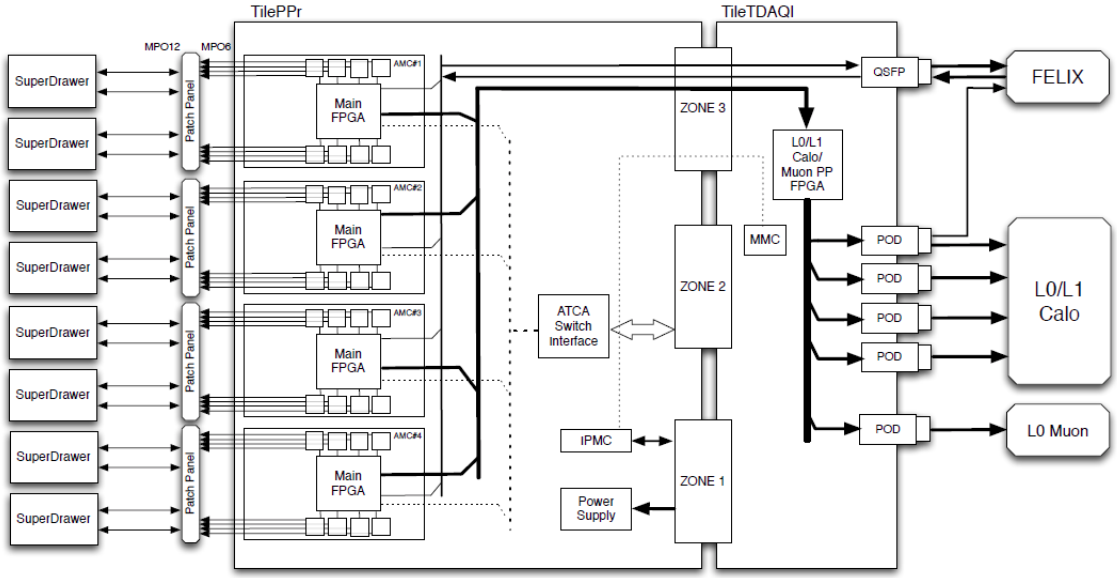
ATLAS TileCal: Serialization and Data Processing

- Daughterboards on front-end:
  - 2 Xilinx Kintex Ultrascale+ with triple redundant logic for serialisation
    - SEE tests to be done
    - tests with Kintex-7 show 1-2 non-recoverable errors per month at HL-LHC
  - 2 SFPs for optical transmission at 9.6 Gbps with Forward Error Correction
  - GBTx chip for clock and control



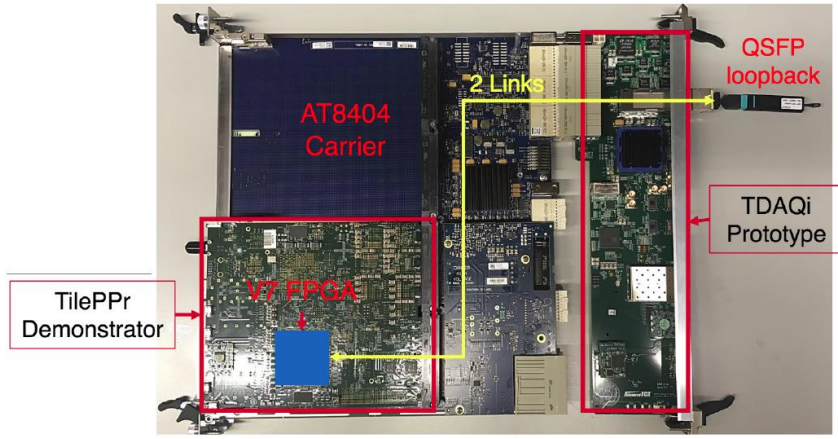


- Off-detector:
  - Tile Preprocessor (PPr)
  - Tile TDAQ interface (TDAQi)



ATLAS TilePPr and TileTDAQi

- 32 ATCA carrier blades each with 4 Compact Processor Modules (CPM)
- 4096 up-links at 9.6 Gbps and 2048 down-links at 4.8 Gbps
- CPM Advanced Mezzanine Card:
  - 32 input links / FPGA = 8 mini drawers
  - digital filter and energy reconstruction
    - 12 DSPs / channel
  - data buffering until L0/L1 accept
    - >2 Mbit memory
  - candidate FGPA Xilinx Kintex Ultrascale

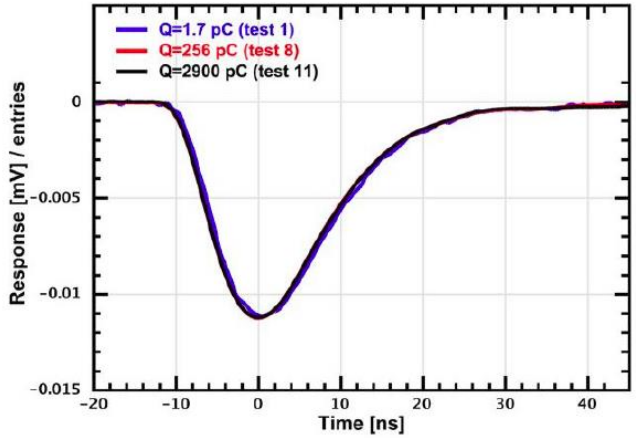


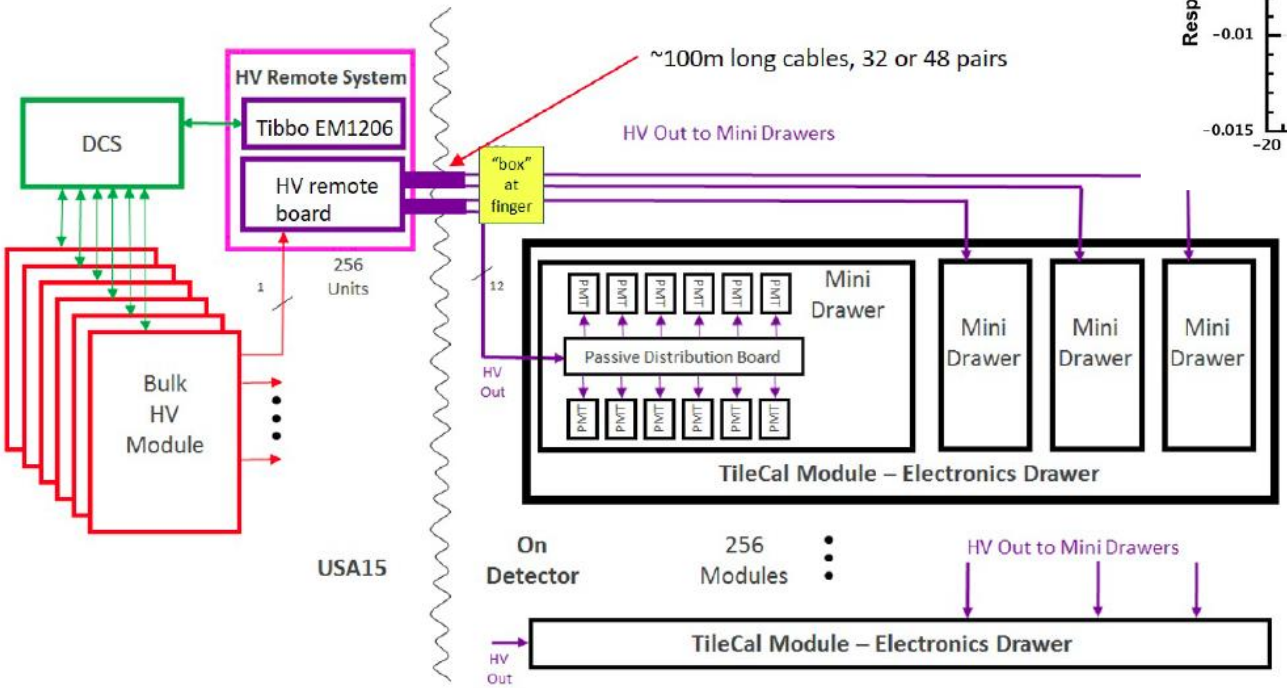
- TDAQi Rear Transition Module:
  - preparation of digital trigger sums → trigger Feature EXtractor (FEX) modules
  - full granularity data after noise threshold (>2σ) → Global Event trigger processors
  - D-layer cells for muon trigger reconstruction

	Receiver	Granularity (η x φ)	Number objects per PPr	Resolution	Link bandwidth	Available bits per link and BC	Bits per link used (data)	Objects per link	Link count
CALO	eFEX	0.1 x 0.1	192 TTs	13 bits	11.2 Gb/s	224	208	16	12
	jFEX	0.1 x 0.1	192 TTs	13 bits	11.2 Gb/s	224	208	16	12
	gFEX	0.2 x 0.2	16 TTs	13 bits	11.2 Gb/s	224	208	16	1
	Global		48 cells	15 bits	14.4 Gb/s	288	184	8	6
MUON	RPC	D-cells	40 cells	15 bits	11.2 Gb/s	224	210	14	3
	TGC	D-cells	36 cells	15 bits	11.2 Gb/s	224	180	12	3

ATLAS TileCal: PMT HV

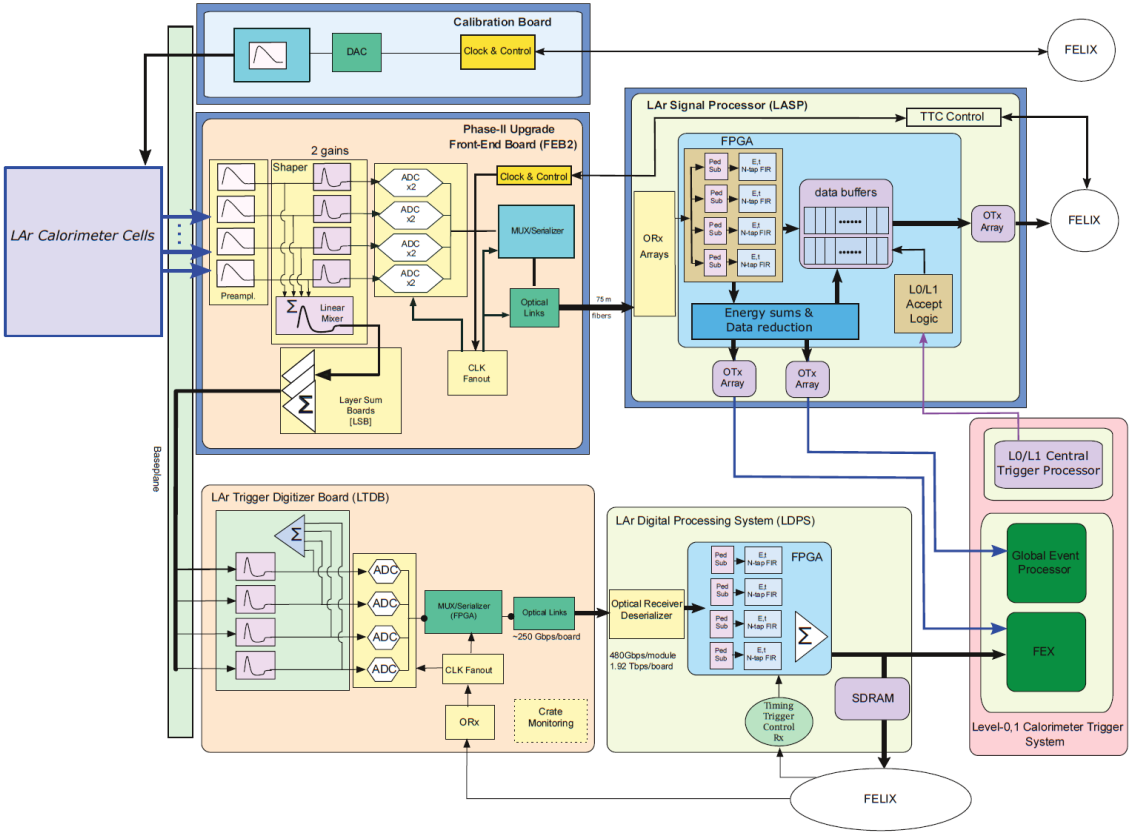
- HV regulators moved to radiation-free environment, each PMT connected individually (100 m cable)
- active HV dividers, improved grounding scheme
- low HV ripple and noise (few mV RMS), stable HV





ATLAS LAr Calorimeter Electronics Upgrade

- Send all data off detector at 40 MHz → flexibility of the trigger system
  - accept rate 1-4 MHz, 35 µs pipelines
  - full granularity calorimeter information available to trigger
- Preserve noise performance as today: non-linearity 2 ‰, detectable MIP signal
- Keep electroweak physics in same gain range (H,Z,W,...):
  - 2-gain readout and 14-bit ADC for 16-17 bit dynamic range



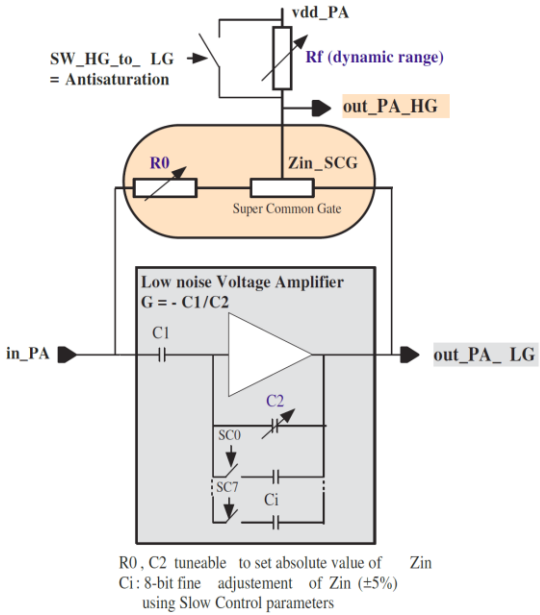
- 1524 new Front-end boards (1 FEB2 / 128 channels)
- 372 LAr Signal Processors (LASP)
- 130 electronic Calibration Boards
- New FE powering

- Phase-I supercell readout remains

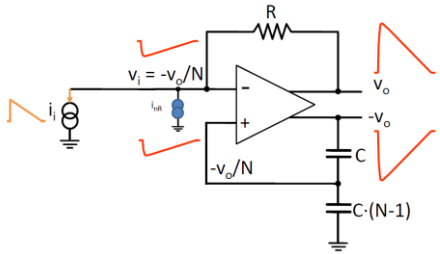
ATLAS LAr Calorimeter: Front-end

- Two preamplifier/shaper developments:
  - super common gate preamp in 130 nm TSMC
  - fully differential preamp/shaper in 65 nm
  - → both have tunable input impedance and low noise

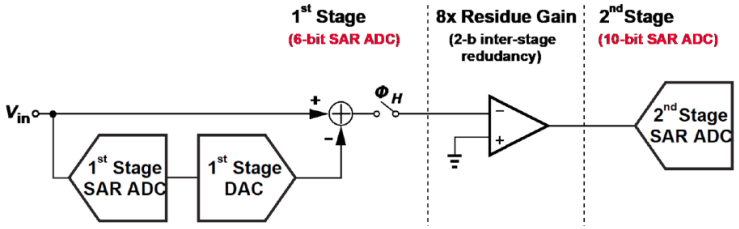
→ combine strengths of the two designs into new 130 nm chip

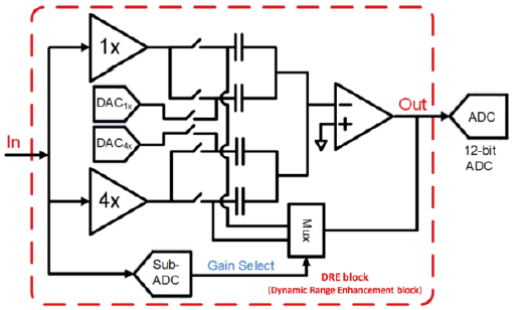


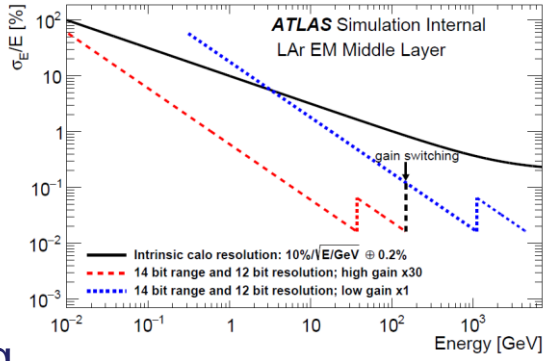
- CR-(RC)^2 shaping is still optimal at high pile-up



- Two ADC designs:
  - 12-bit SAR ADCs combined with Dynamic Range Enhancer (DRE) → 14-bit ADC







  - commercial 12-bit ADC IP block (CMS) with oversampling and digital filter → 14-bit ADC

- 22 lpGBT Tx links per FEB2 for data transmission → 33528 fibers
- 2 lpGBT Tx/Rx link pairs per FEB2 for individual clock and control → 6096 fibers

ATLAS LAr Calorimeter: Off-Detector

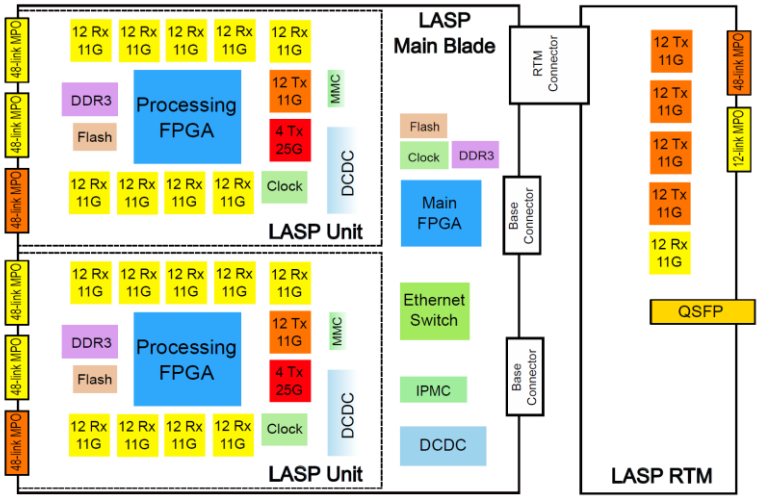
- Baseline links per FPGA:
  - 88 lpGBT input links to process 512 cells
  - 2-3 DAQ links, up to 27 links for trigger FEX
  - 4 links for Global Event trigger @ 25 Gbps

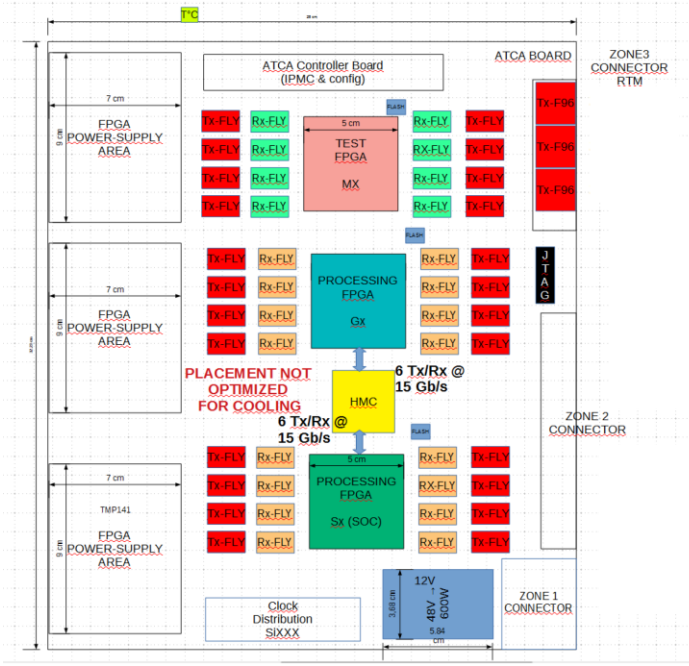
- Main tasks:
  - digital signal filtering and energy+time measurement with active pile-up correction
  - preparation of trigger primitives: energy sums and energy-ordered cell energies
  - real-time baseline correction - if needed

→ 36 DSPs/channel and 151 Mbit of memory / FPGA

- Ongoing R&D on full-size ATCA blades
  - evaluate Altera/Intel Stratix 10 SX / MX: integrated processor or large high-bandwidth memory
  - Samtec Firefly transceivers
  - cooling is a challenge

- TTC distribution to FEB2 → evaluate solution as separate TTC blade (less powerful FPGAs needed)



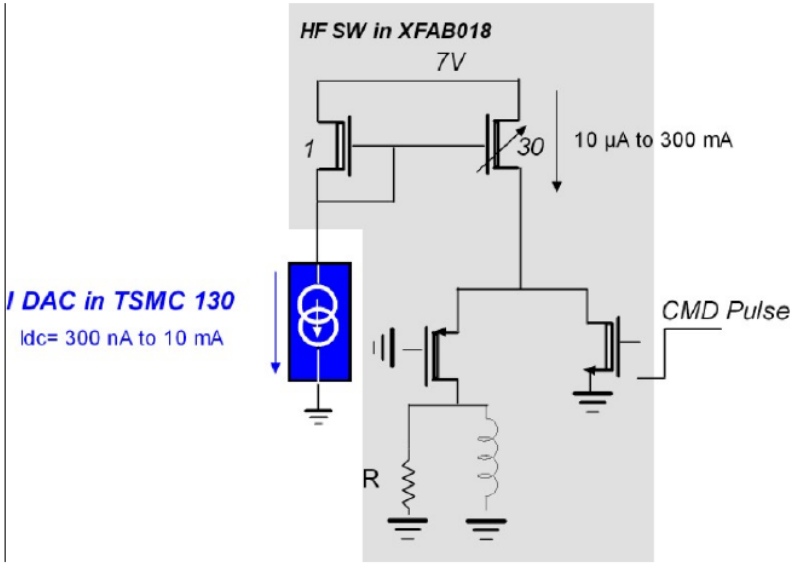


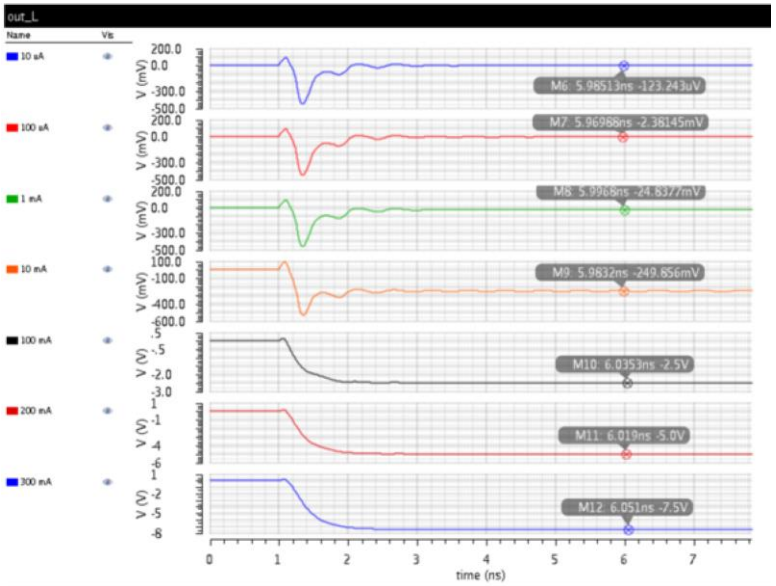
LASP Testboard

ATLAS LAr Calorimeter: Calibration Board

- Pulses are injected at the level of the LAr calorimeter electrodes
- To cover signal currents up to 10 mA, a 7.5 V calibration pulse needs to be injected → HV-CMOS technology (X-FAB XT018)

- Baseline: 16-bit DAC in 130 nm TSMC and current mirror to HV-CMOS HF switch
- Like to have ideal exponential pulse shape at all amplitudes → find balance between ringing and parasitic signals





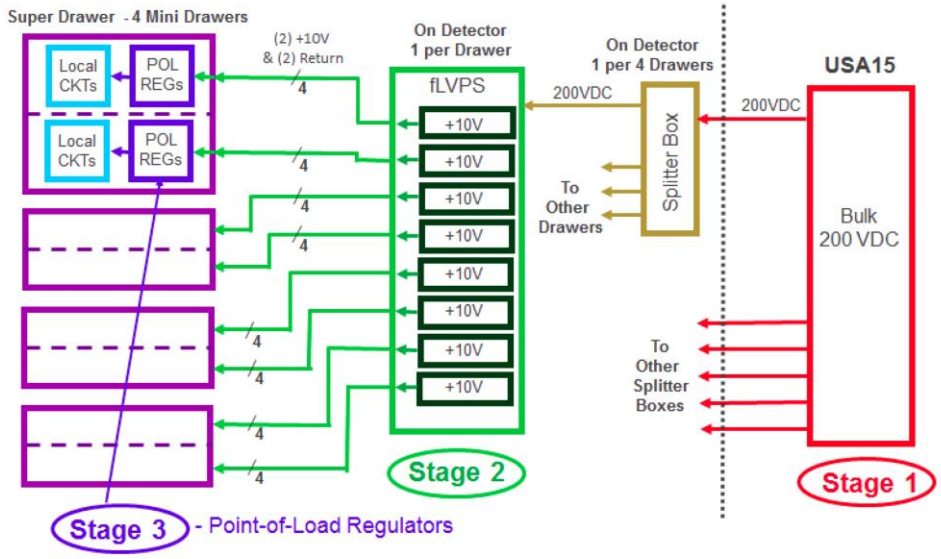
- Switch and DAC test chips have been submitted and first results expected soon
- Radiation tests are in preparation

Low-Voltage Power Supplies

- All new front-end electronics rely on a similar powering concept
- Radiation and magnetic field tolerance is required for on-detector power devices

- Main ACDC converters for 200 V - 400 V
  - CMS EB: Maraton PS 400 V
  - ATLAS: 200 V (Tile) and 280 V (or similar, LAr)
- LVPS from 200V-400V to 12 V or 24 V or 48 V or 10 V
  - most DCDC converter developments in collaboration with industry (CAEN, Wiener)
  - located in better accessible area → long(er) power cables → noise? small diameter
  - redundancy:
    - 2 or 3 modules including 1 spare to be turned on remotely/automatically
    - power bricks running in parallel
- on front-end 2.5 V - 7.5 V local voltage
  - PoL converter and linear regulators

example: ATLAS Tile LV power scheme



Summary and Outlook

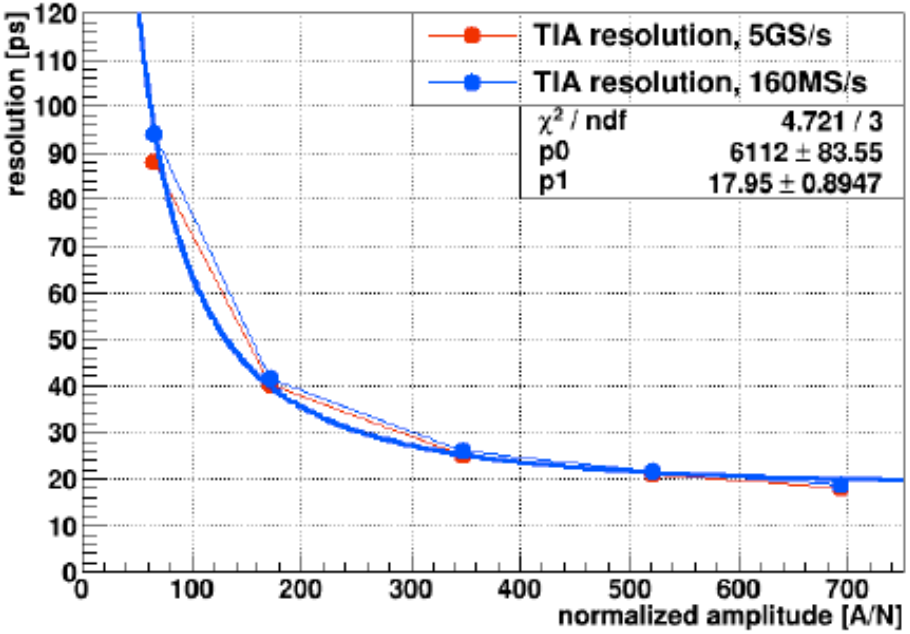
- All main calorimeters will be read out at 40 MHz motivated by new trigger systems
  - CMS ECAL includes precision time measurement
- Different front-end electronics because of: different preamp/shaper solutions, different optimal sampling rate, different radiation requirements
- Common hardware will be used for data transmission and detector control:
  - lpGBT, GBT, VL+
  - ELMB++
- Possible common solutions for LV powering:
  - PoL regulators, LVPS, ACDC main converters
- Would be nice to have:
  - radiation tolerant optical links beyond 10 Gbps → fewer FE fibers, better match to payload, more demanding FPGA requirements in data processing and buffering
- More ACES contributions on calorimeter electronics:
  - Preamplifier/Shapers and ADC for Calorimeters: Philippe Schwemmling Wednesday 15h30
  - Power Requirements and Developments for Calorimeters: Sergei Lusin Thursday 9h30
  - Thursday noon/afternoon: all on ATCA boards and infrastructure

More Information

Radiation Tolerance

	TID (kGy)	NIEL (n_{eq}/cm^2)	SEE (h/cm^2)
ATLAS LAr	2.3	4.9×10^{13}	7.7×10^{12}
CMS EB	10		$\sim 10^{13}$
ATLAS Tile	0.2	6×10^{12}	1.5×10^{12}

CMS TIA performance



- discrete-component trans-impedance amplifier

Q is the number of electrons

APD ($\epsilon \approx 0.1$)

F is the excess noise factor

M the gain of the APD

$$\sigma_Q = \sqrt{\frac{\Delta t \times I_{\text{leak}}}{q_e}[\epsilon + MF(1-\epsilon)]}.$$

σ_Q~ sqrt(leakage current x integration time)

CMS TIA performance

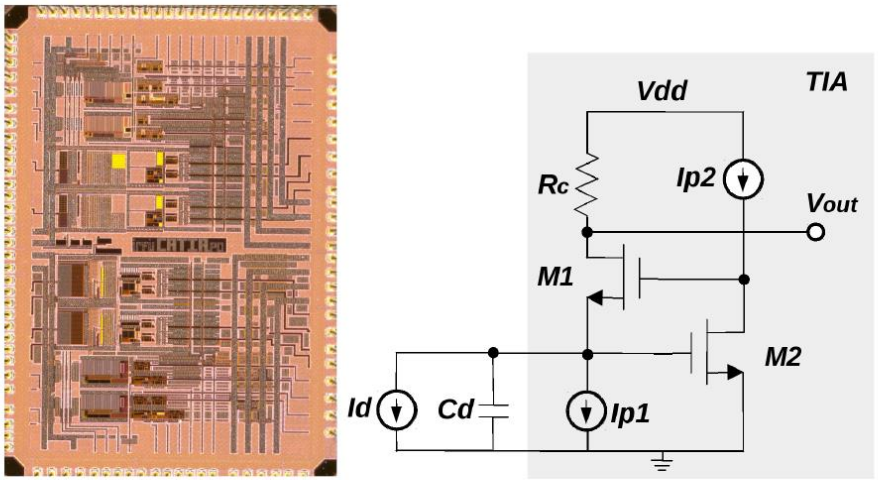
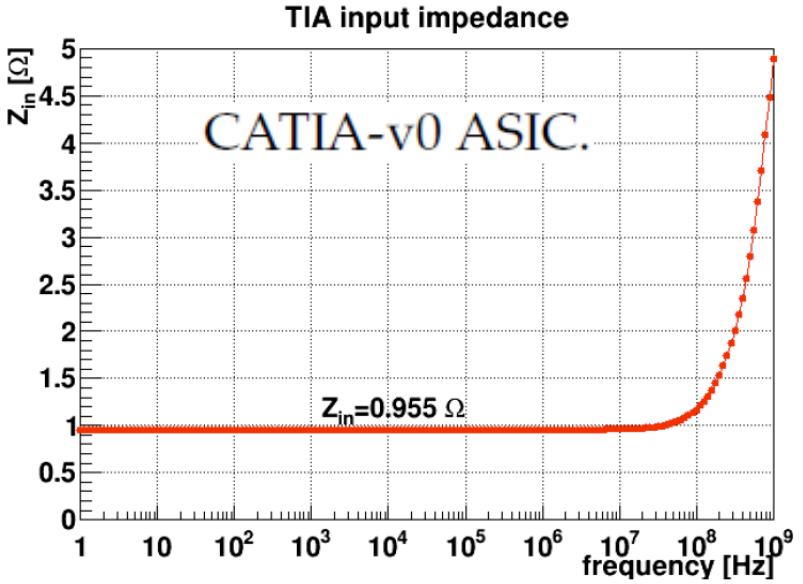
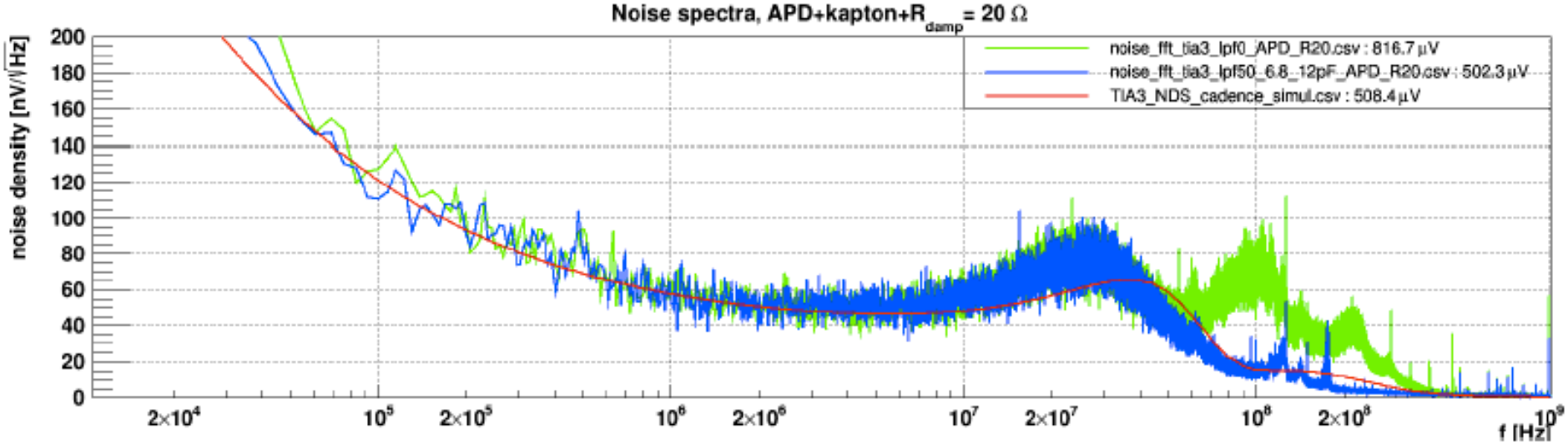
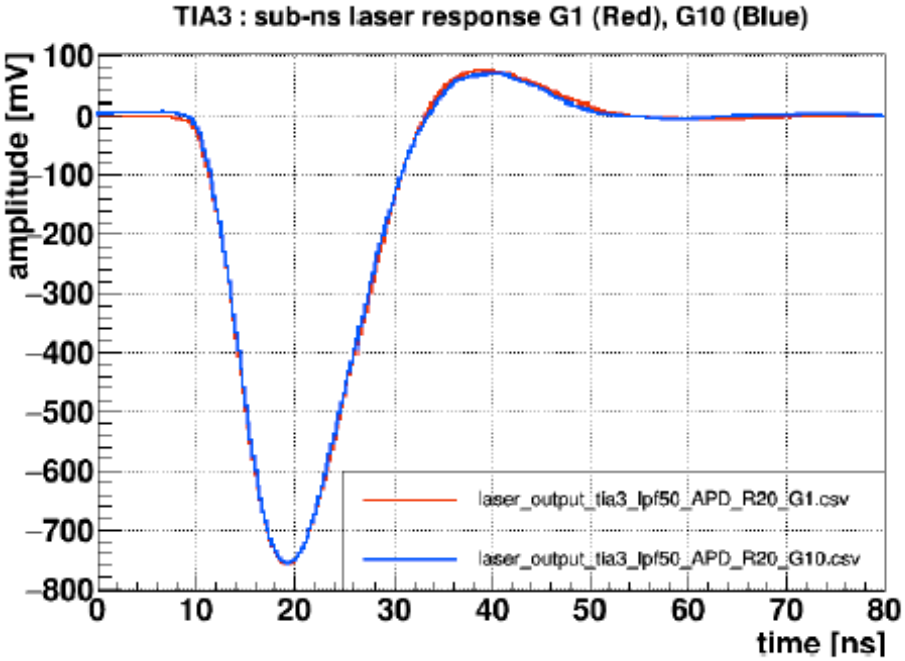


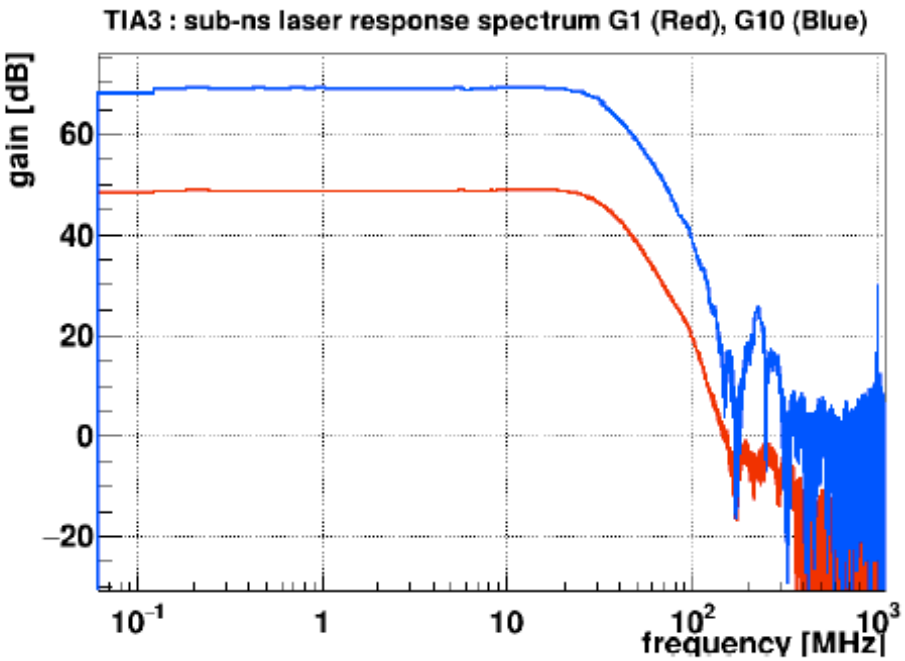
Figure 3.9: Microphotograph of the CATIA ASIC (left), and schematic view of the TIA architecture (right). See text for explanations.



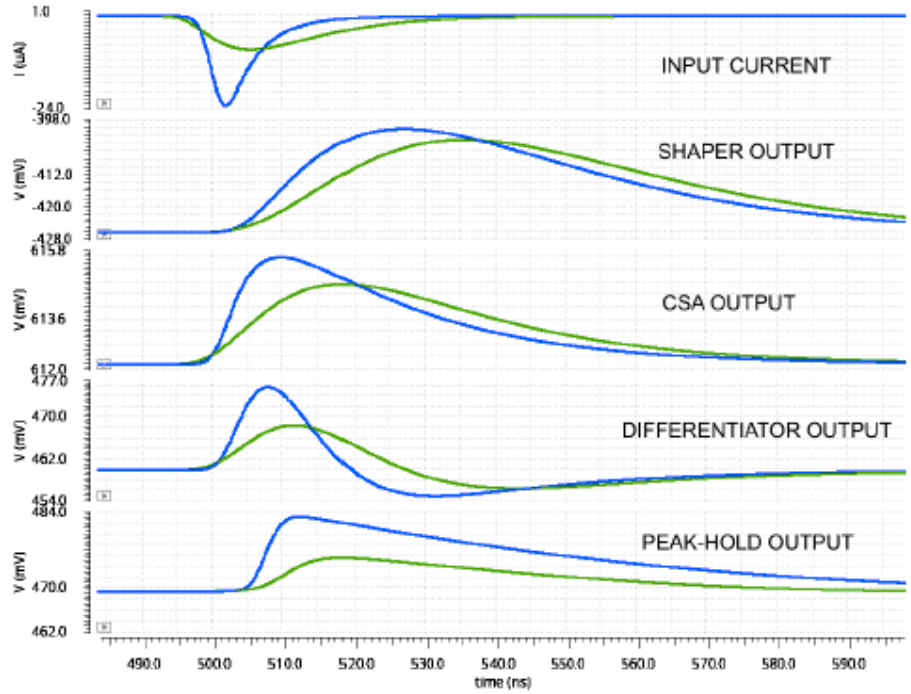


CMS TIA performance





CMS Charge Sensitive Amplifier (CSA) performance



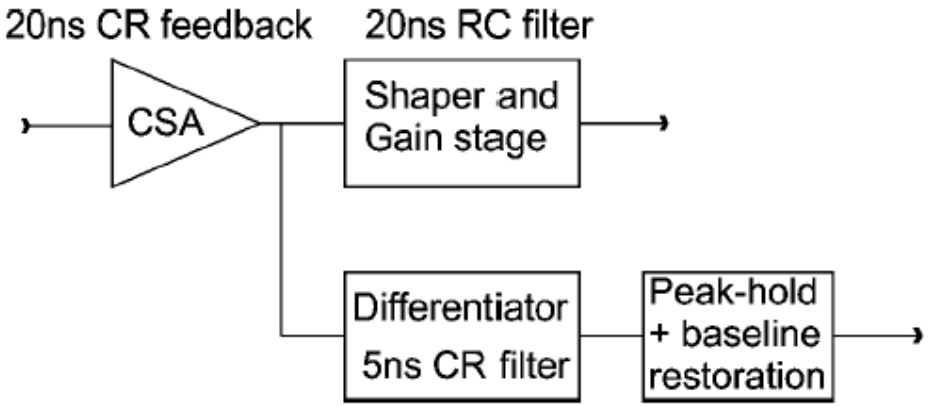
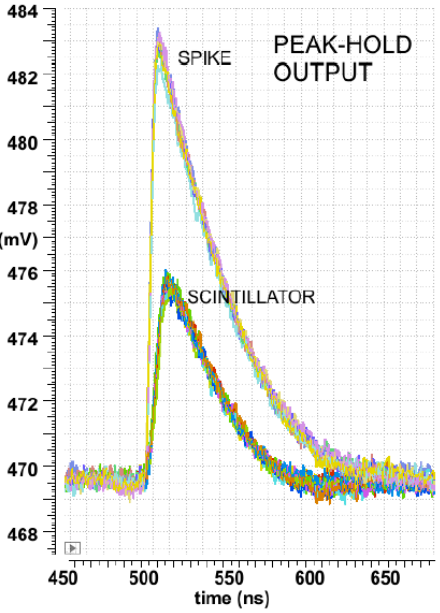
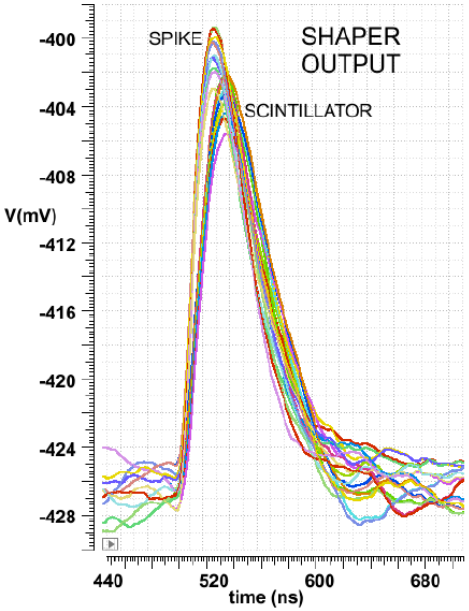


Figure 3.13: Left: MGPA++ simulation. Spike pulses are in blue, and scintillation pulses are in green. Right : MGPA++ preamplifier, shaper, and differentiator arrangement.

CMS CSA performance





- on-chip spike detection not robust enough in all amplitude ranges
- off-detector spike identification prefered

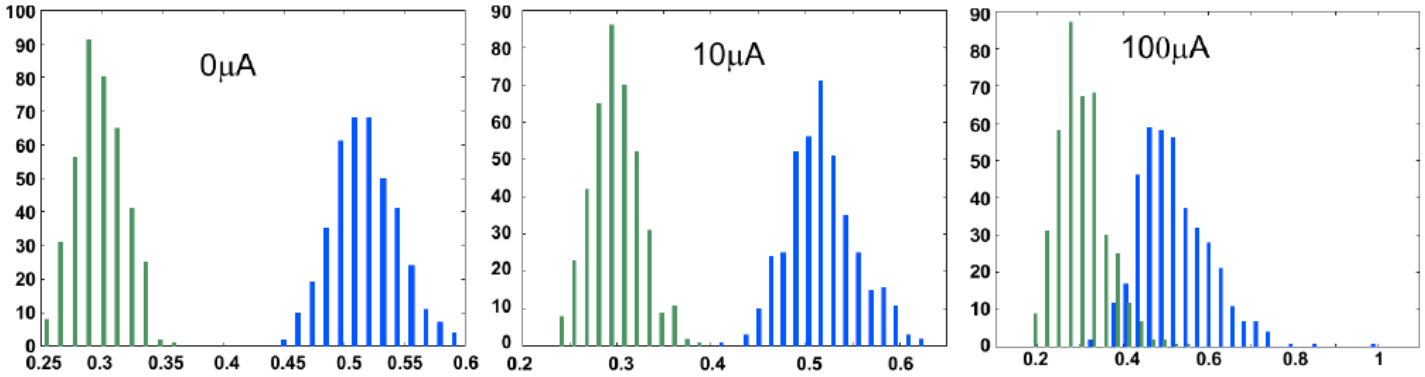


Figure 3.15: Peak-hold/shaper ratios for spikes and scintillation pulses at 2 GeV, for 0, 10, 100 μA detector leakage currents.

CMS CSA performance

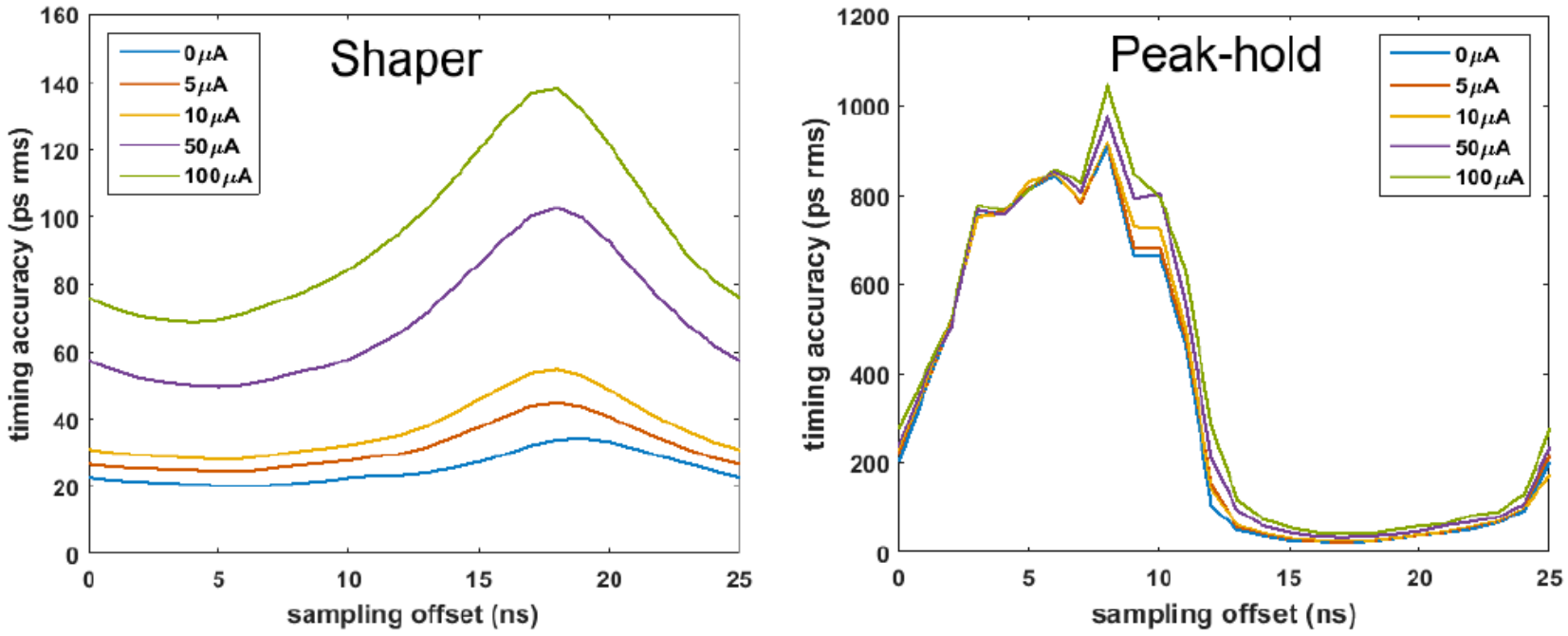


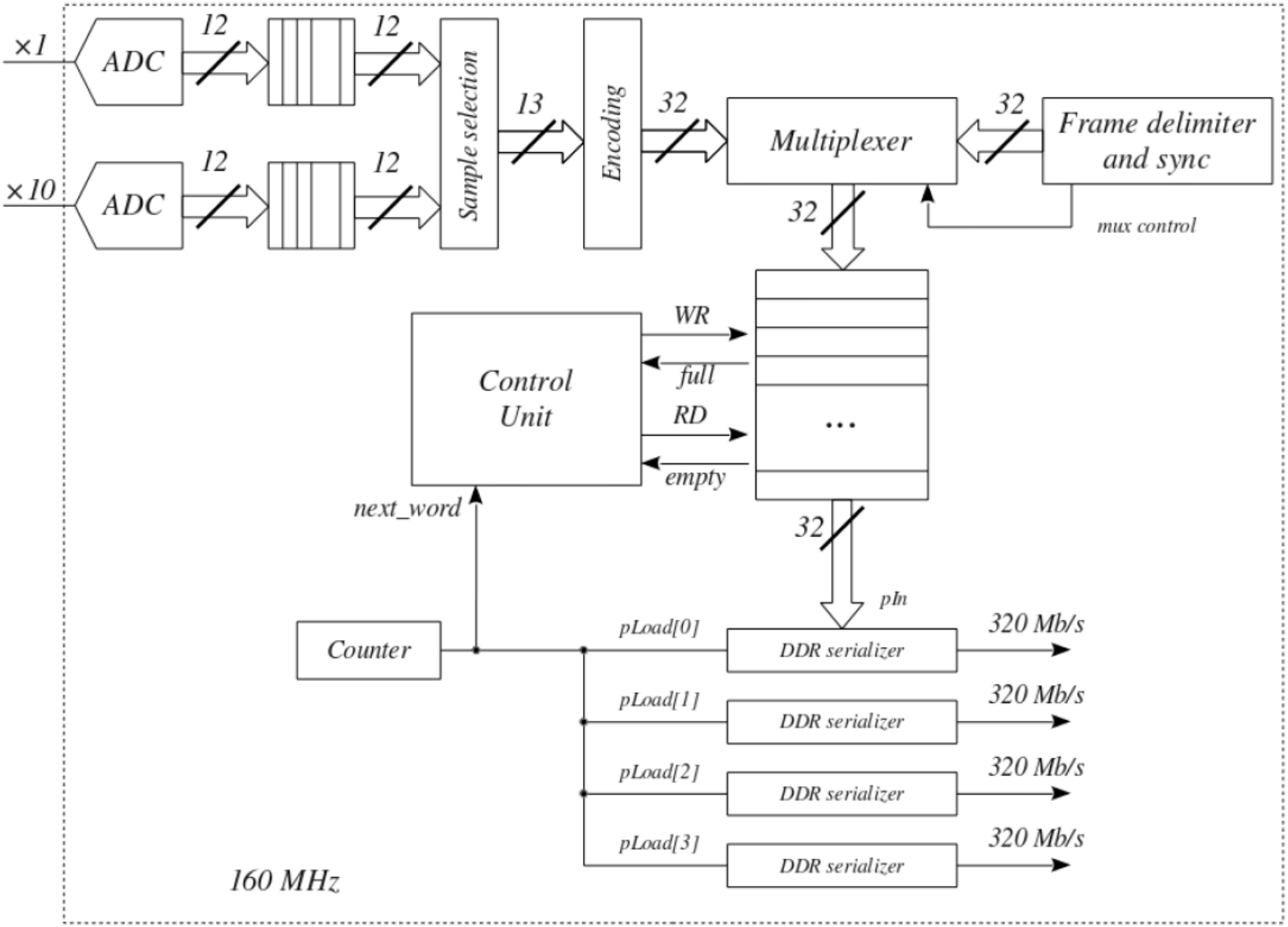
Figure 3.16: Timing accuracy for the shaper (left) and the peak-hold (right) circuits, for detector leakage currents from 0 to 100 μA.

CMS FE: ADC Requirements

Table 3.2: ADC requirements.

Specification	min	typ	max	unit
Sampling frequency	160			MS/s
Resolution	12			bit
Supply voltage	1.08	1.2	1.32	V
Differential input range	±500			mV
Analogue input bandwidth	70	80		MHz
Slew rate	100			V/μs
Sampling clock jitter		2	5	ps
Power consumption		25	30	mW
Temperature range	−20	8	85	°C
INL		1	1.5	LSB
DNL		0.5	0.9	LSB
ENOB	10.2			bit
SNDR	63			dB
Latency		10		Clock cycles
Calibration time		100		μs
Technology	CMOS 65 nm			
Radiation tolerance (TID)	100			kGy
SEU cross section	15 (tbc)			MeV cm^2/mg

CMS FE: Gain Selection, Encoding, Multiplexing



- probability for energy value with >6 bit is 2 x 10^{-4}: baseline bandwith of 2 Gbps/channel can be reduced to 1 Gbps + few Mbps for signal energies

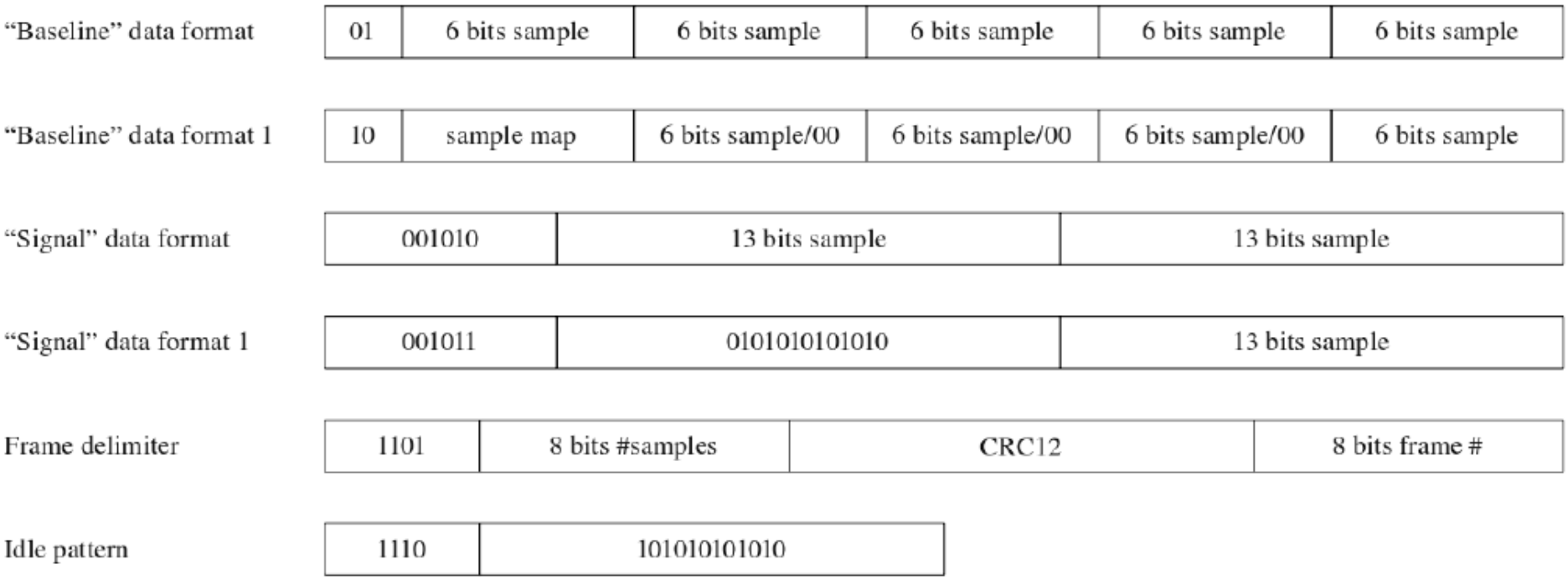


Figure 3.18: Proposed data format.

- L1 trigger primitives: either 16-bit data per crystal or per 5x5 tower

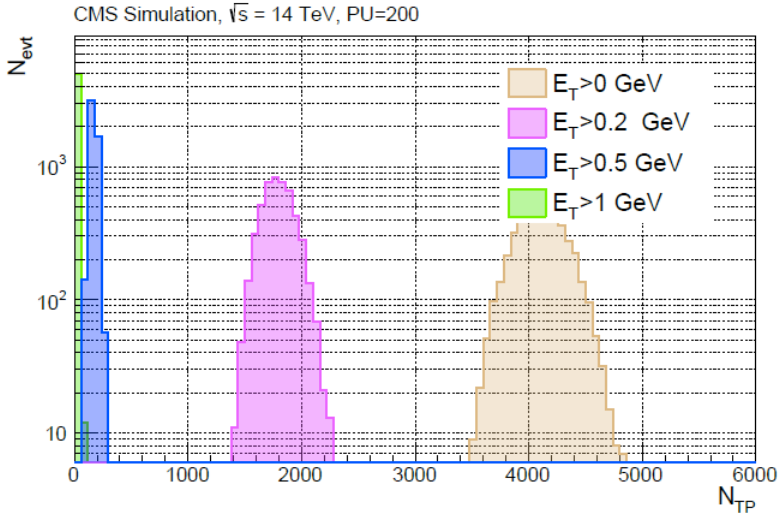


Figure 3.29: Distribution of the number of single crystal trigger primitives expected per event for several crystal E_T thresholds and a pileup level of 200 events.

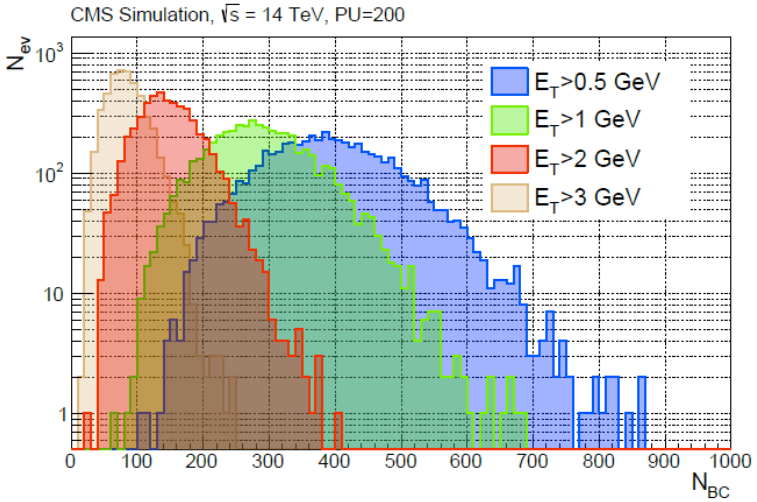


Figure 3.30: Distribution of the number of cluster trigger primitives expected per event for several cluster E_T thresholds and a pileup level of 200 events

CMS ECAL Barrel Calibration

- Energy and timing calibration and inter-calibration needed: new laser system and PiN diode light control system
- Light readout with GSample/s MATACQ chip