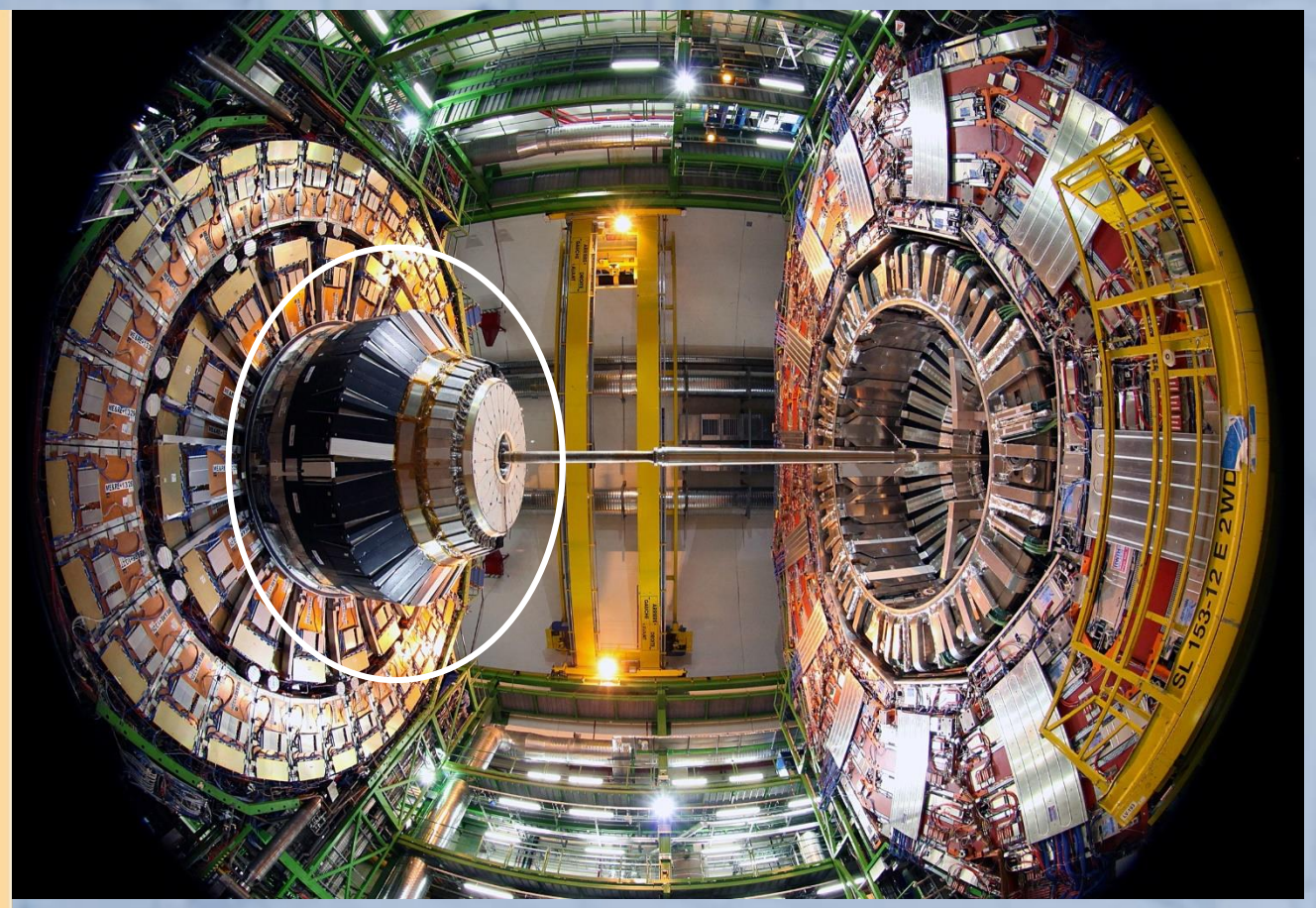
High Granularity Calorimeter (HGC) Readout

Apr 25 2018

Paul Rubinov

Shown by Jim Virdee Apr18 2018

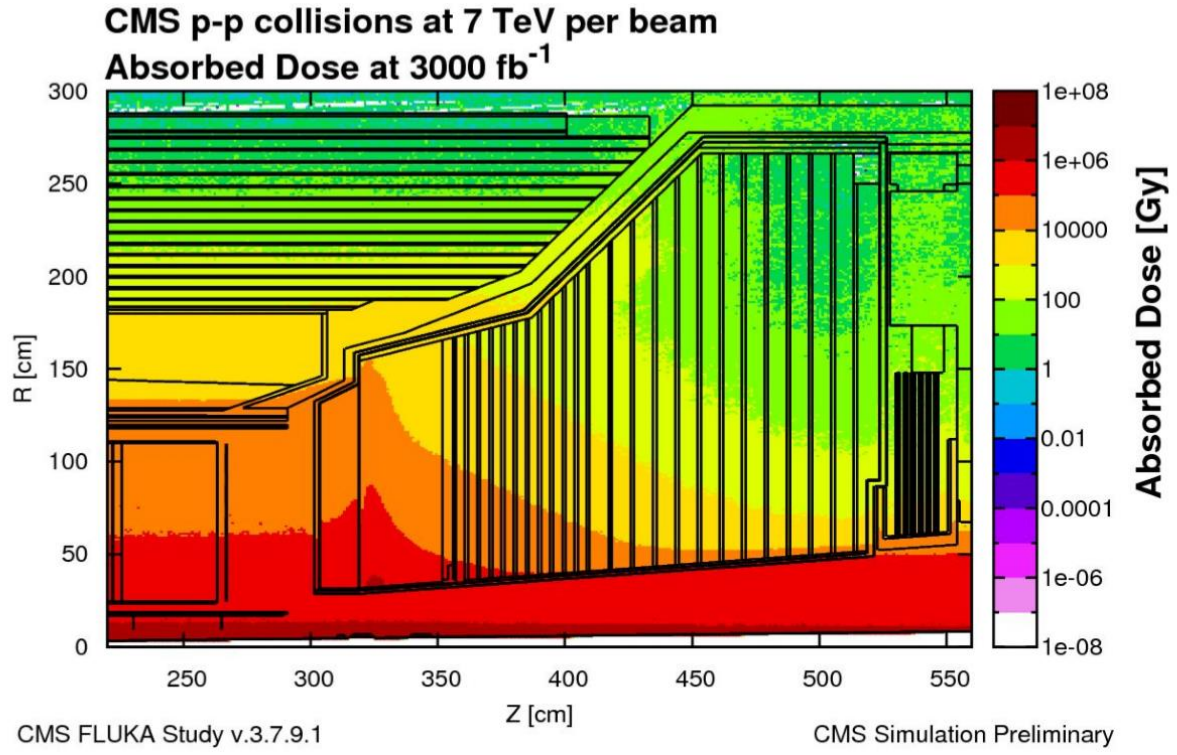


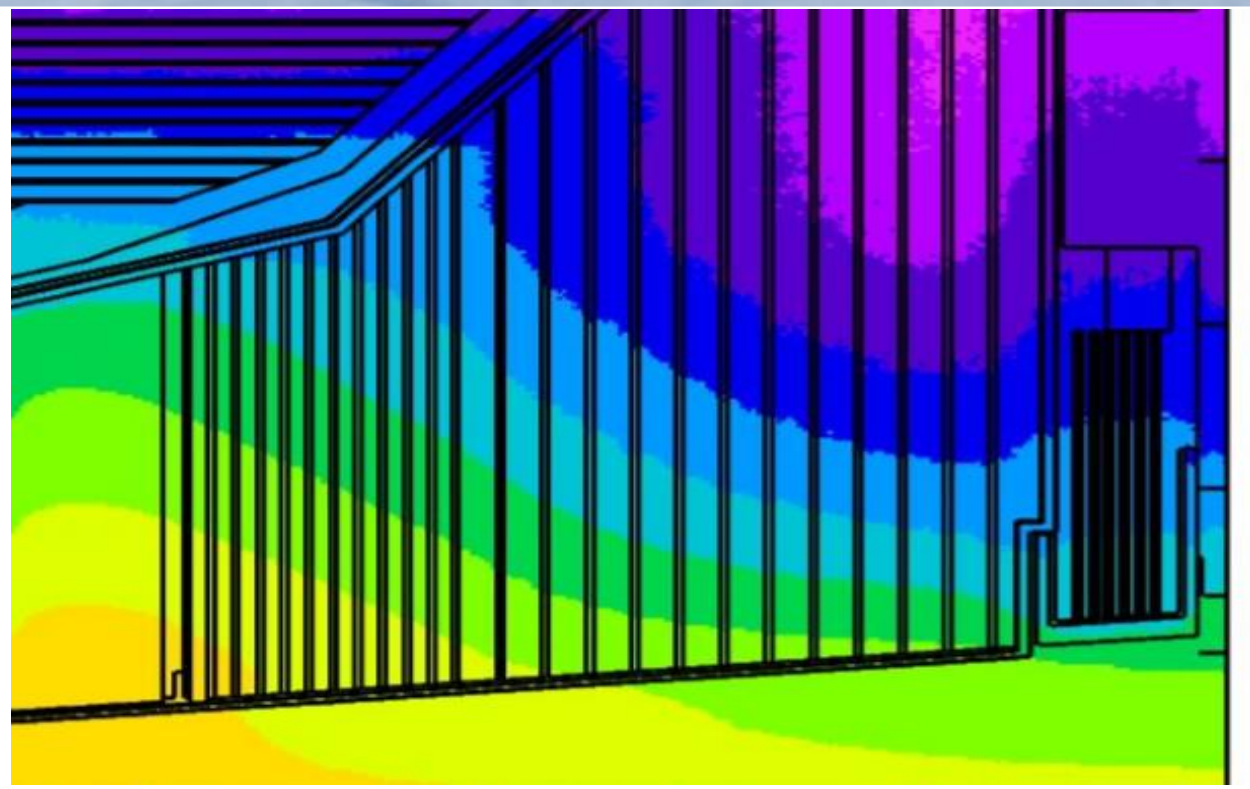
Review outcome:

"…the proposed design of the high granularity endcap calorimeter for the CMS upgrade is challenging but is expected to satisfy requirements of the harsh HLLHC running conditions. Continuing R&D and simulation studies are needed to verify and optimize the design choices. "

https://cds.cern.ch/record/2293646?ln=en

Physics Driven Basic choices:

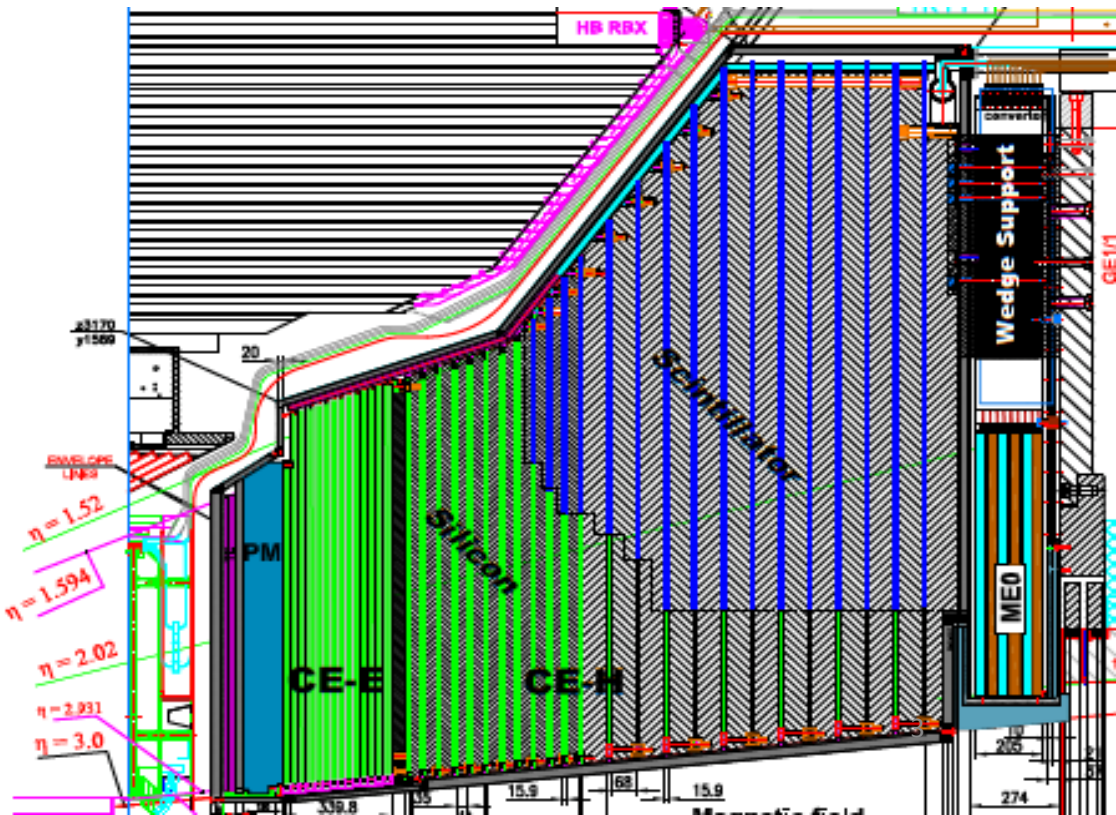




Highest (total dose) 10^{16} neq/cm^2 and around 200 MRad
→ Silicon sensors where dose >3kGy and > 10^{13} n/cm^2
→ Scintillator w SiPM readout < 3kGy and < 10^{13} n/cm^2

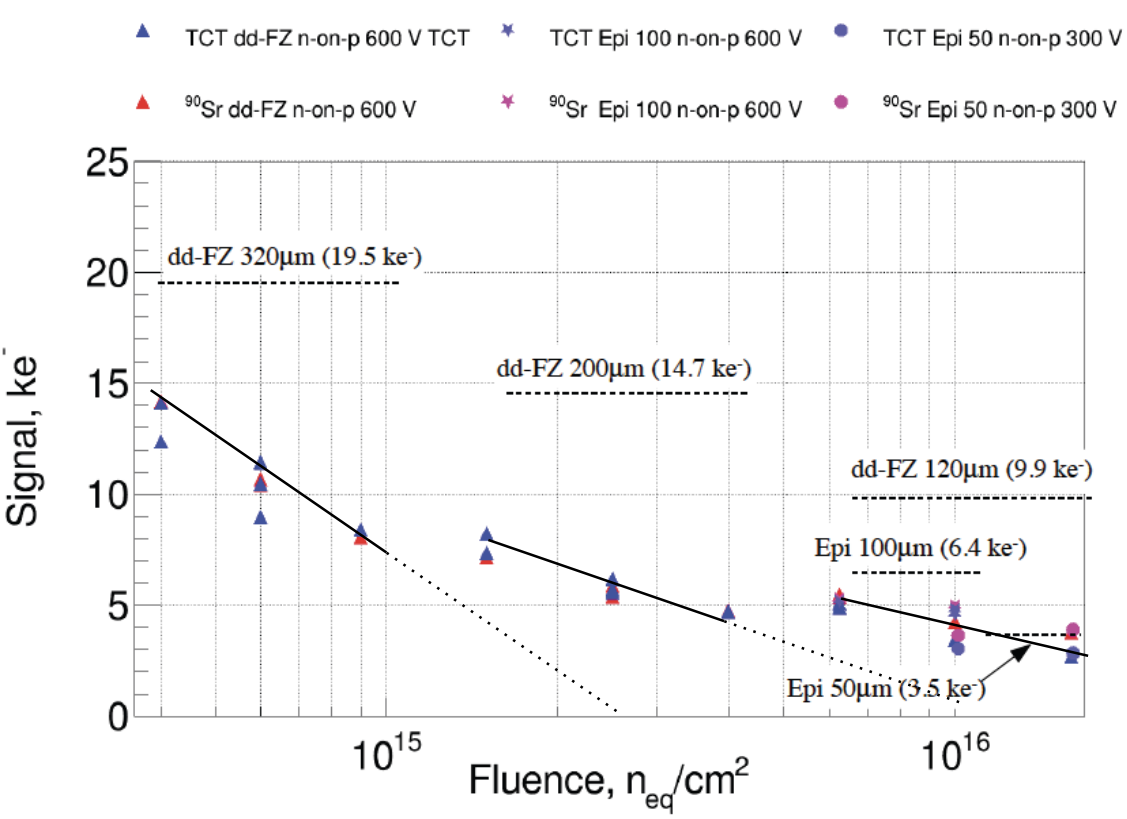
3 types of cassettes:
Very fine grained in the CE-E section every ~1 X_0 in 28 layers
double sided with lead absorber
Single sided Si only in the CE-H layer 1-8
Single sided Si+Scint in the CE-H layer 9-24
for total ~10l
52 layers in all!

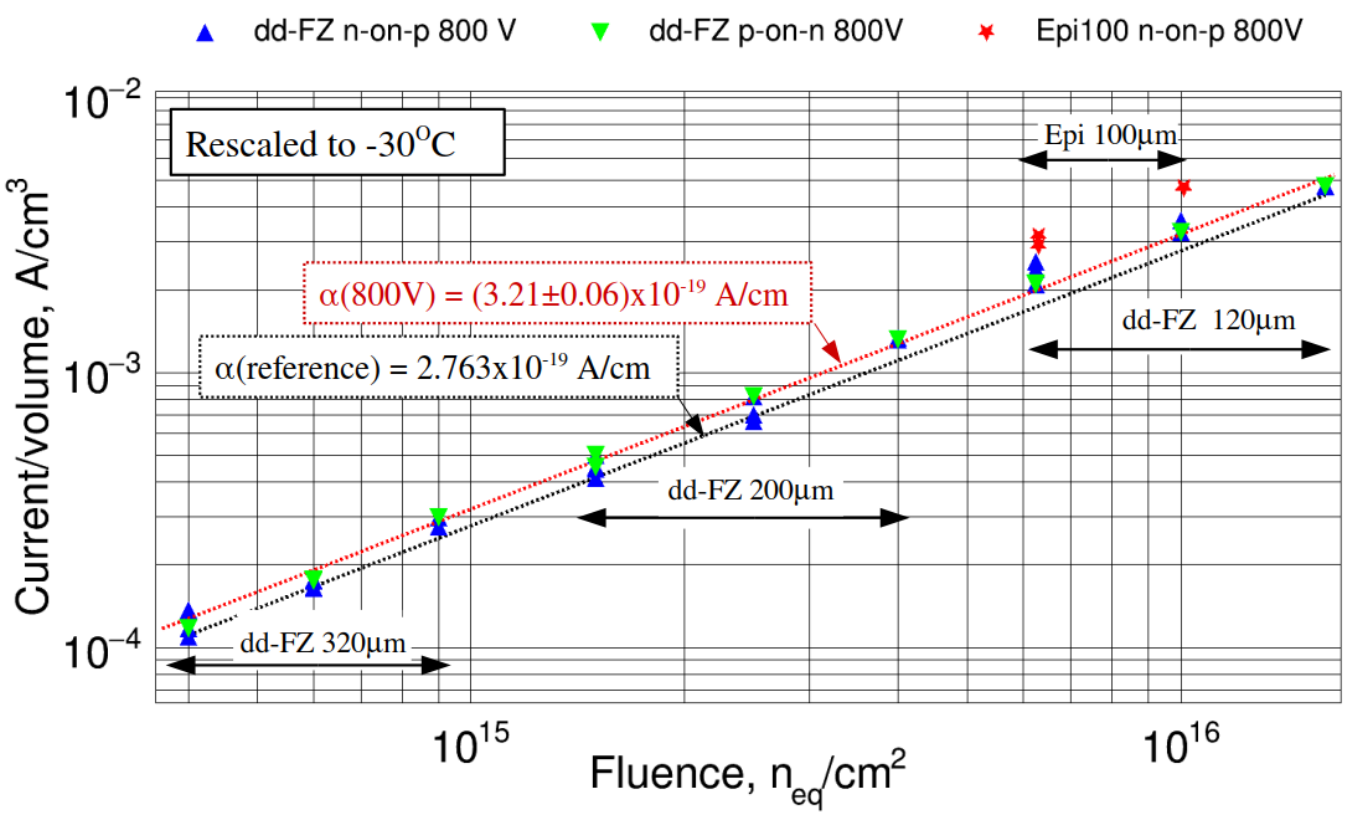
η range ~1.5 to 3



Physics Driven Choices (cont)

- Radiation is driving choice of Si
  - Cool as much as possible (-30C) to minimize leakage current
  - Still have ~10uA/cm^2 for 320um Si → need thinner Si for larger fluence regions





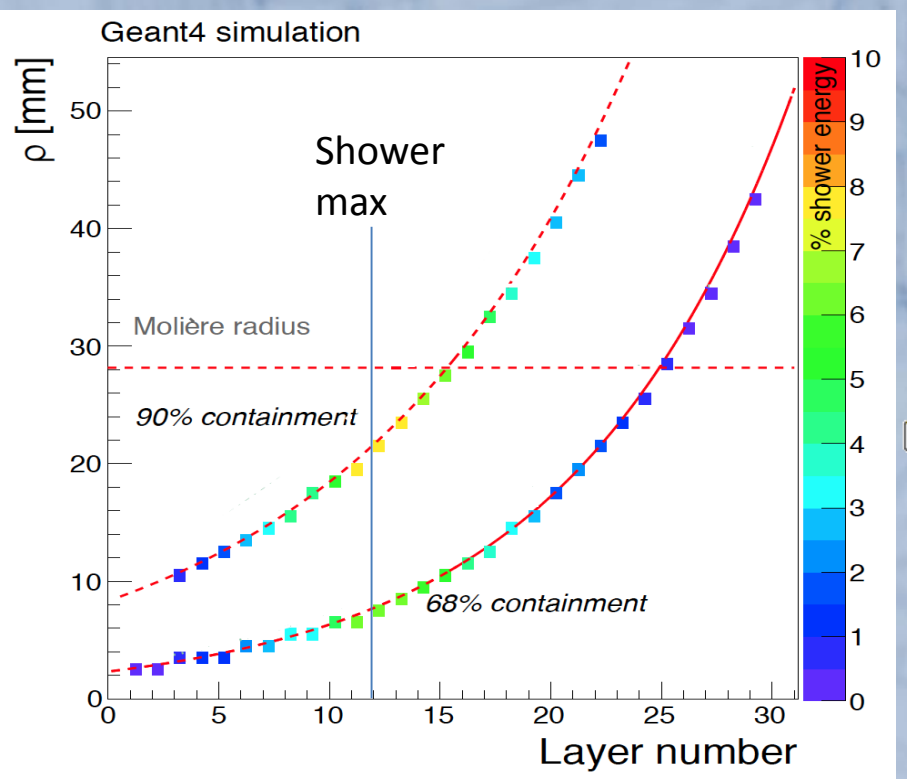
Leakage current, capacitance proportional to area,
MIP signal NOT proportional to area

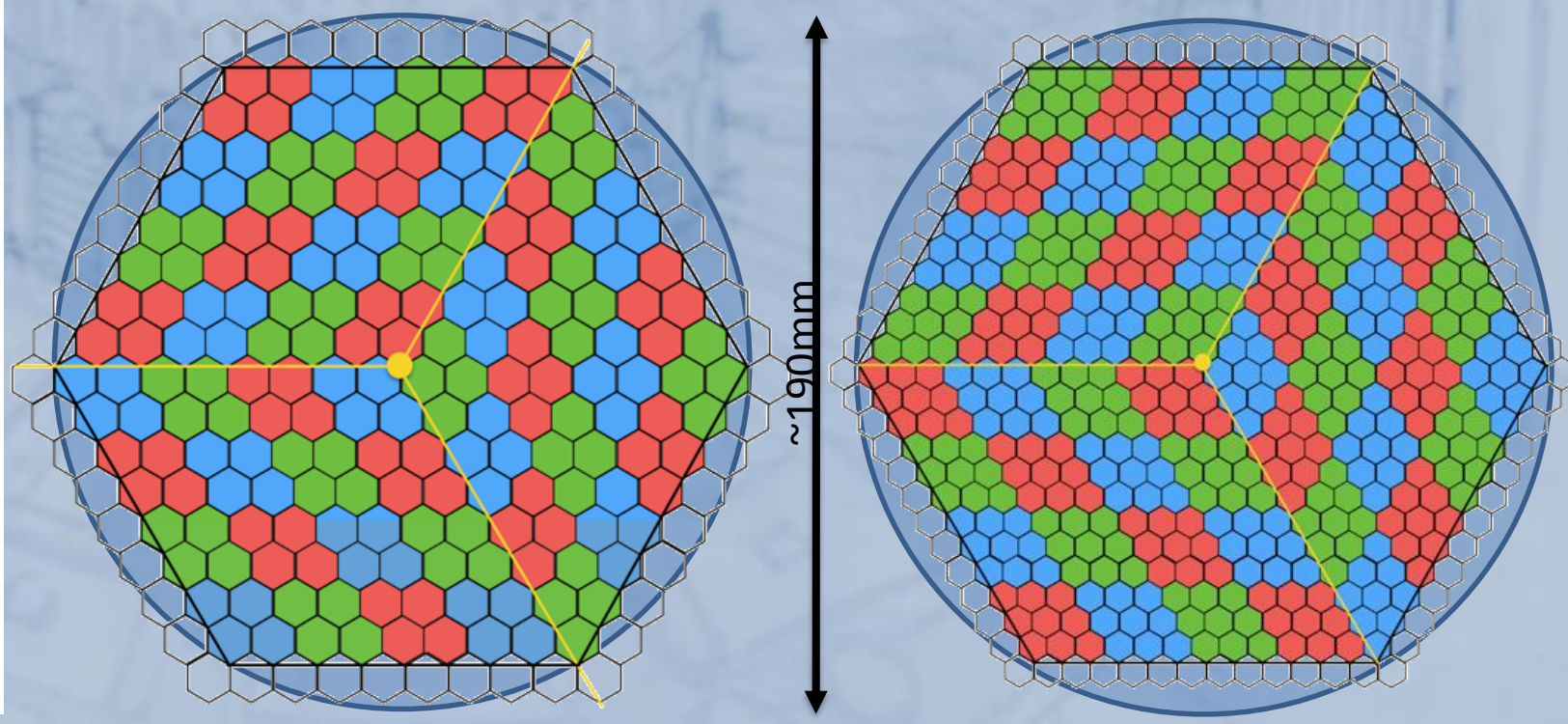
Constant term less than 1% REQUIES the we be able to measure MIPs
Keep FE noise <2ke to see MIP in 100um Si!

Physics Driven Choices (cont)

- Radiation is driving choice of Si
- Size of the detector / cell size → channel count
- Must be kept at -30C → Cooling power ~110KW /end cap → ~20 mW/ch for all electronics
- Leakage current, capacitance proportional to area, MIP signal NOT proportional to area

CELLS CAN NOT BE >> 1cm² for 300um/200um, 0.5 cm² for 100um





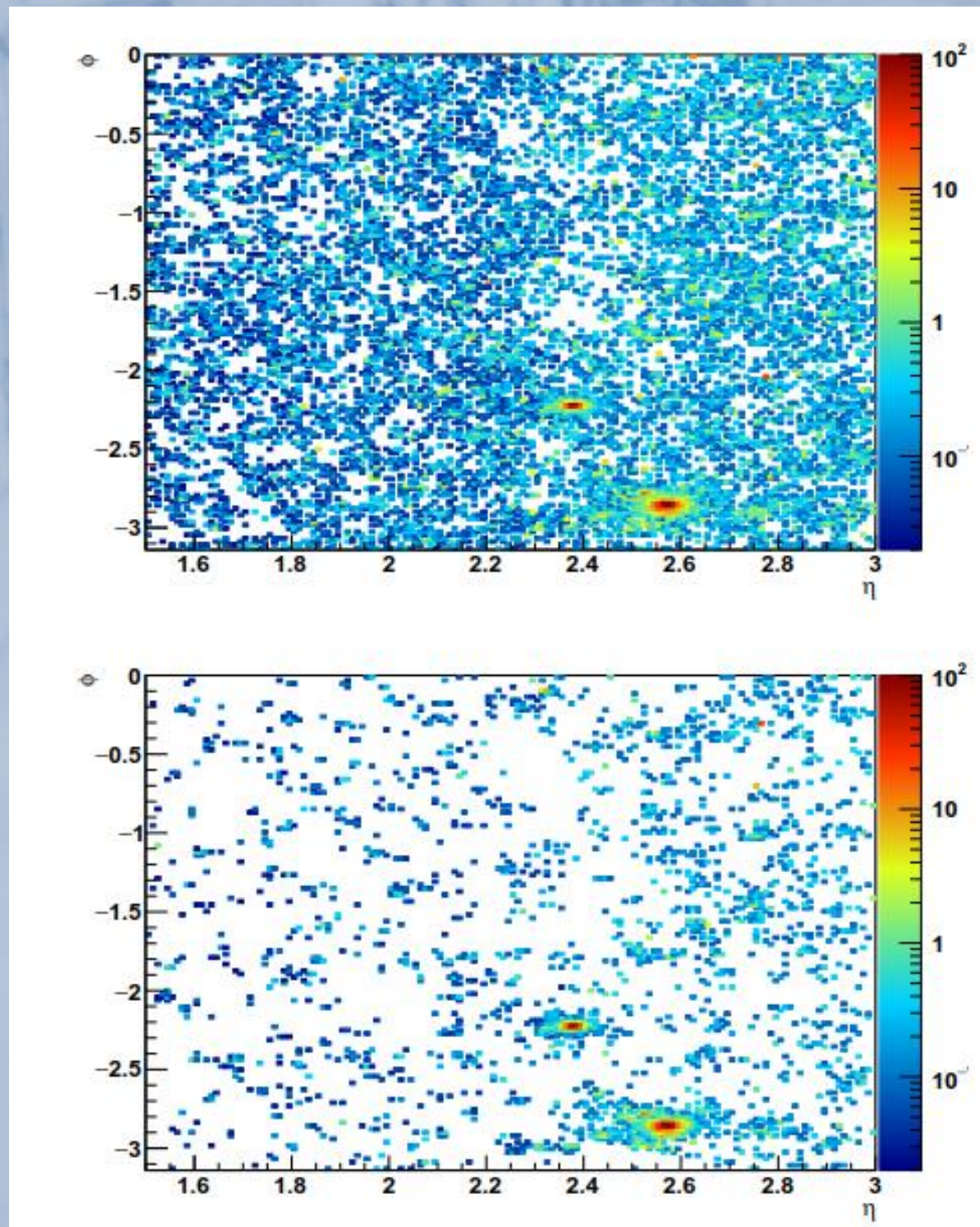
EM showers are not much bigger than 1cm too!

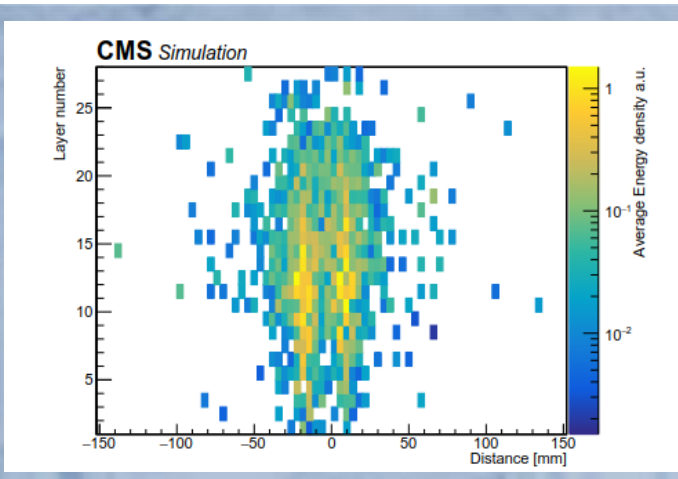
~50pF for all cells

200mm wafers patterned with 192 cells (200/300um) or 432 cells
Cell size is quantized – driven by wafer size

But we always knew want small cells and fine segmentation

In the very busy environment, we have fine 4D segmentation: x, y, z, t





2x 80GeV E Photons 3cm apart

H→ γ γ with all hits above 12fC projected to the front face of calorimeter (VBF + γ)

Same after removal of hits with $|\Delta t|>90$ps

CMS HGCAL: a 52-layer sampling calorimeter with unprecedented number of readout channels

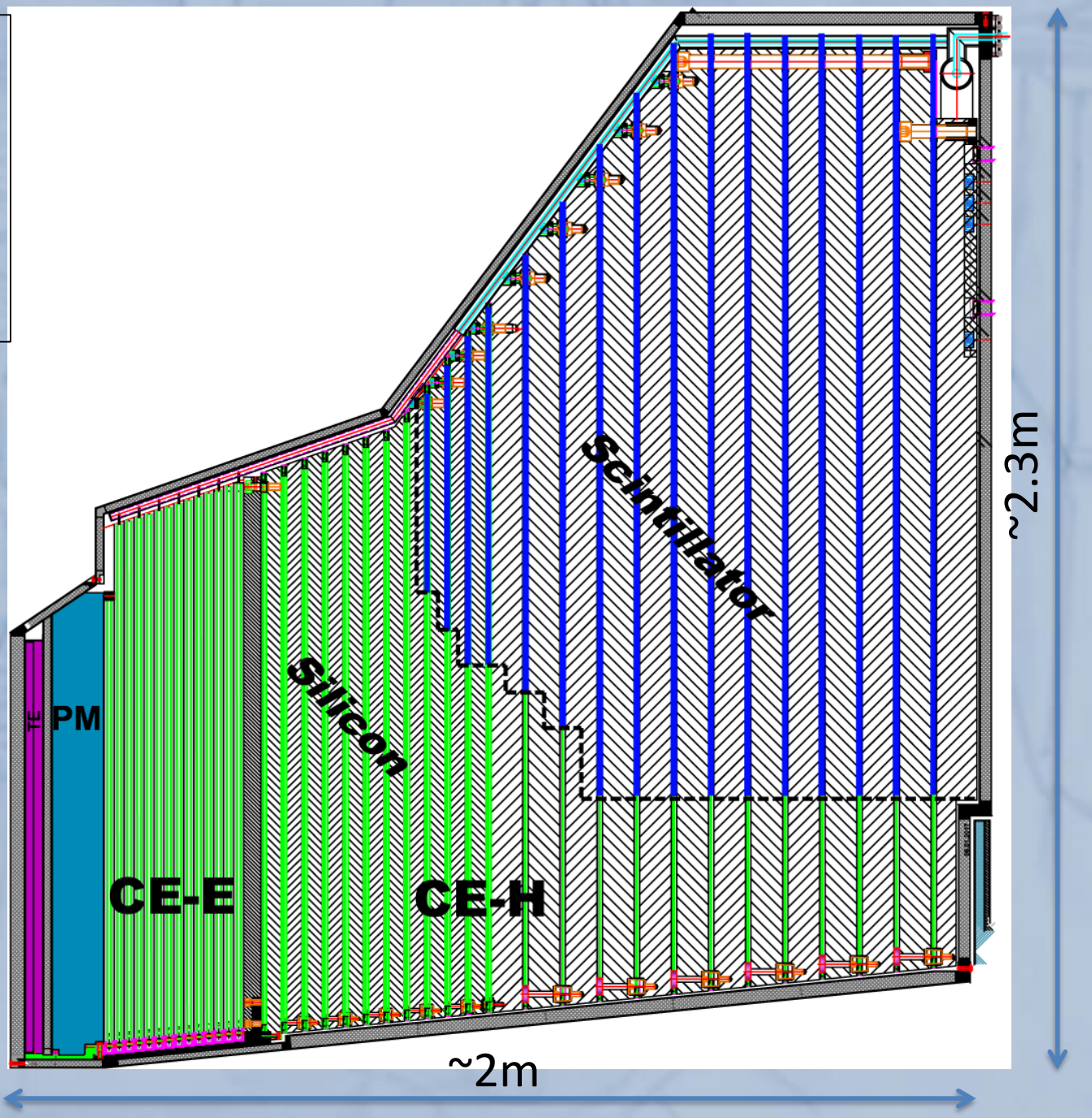
Active Elements:

- Hexagonal modules based on Si sensors in CE-E and high-radiation regions of CE-H
- Scintillating tiles with SiPM readout in low-radiation regions of CE-H

Key Parameters:

- **~600m²** of silicon sensors
- **~500m²** of scintillators
- 6M Si channels, 0.5 or 1.1 cm² cell size
  - Data readout from all layers
  - Trigger readout from alternate layers in CE-E and all layers in CE-H
- ~27000 Si modules (sensor wafers)

Cooling is a fundamental limitation: 110kW per endcap



Electromagnetic calorimeter (C**E-E**): **Si**, Cu/CuW/Pb absorbers, 28 layers (26 X_0)

Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 24 layers, (10λ_I)

HGC Electronics: Physics driven requirements

- Noise : ~0.3fC, 2ke$^-$

  Inter-calibration require isolated cell

  < 1% constant term requires 3% precision → MUST BE ABLE TO MEASURE MIP

- Shaping: ~20ns, ~50ps timing
- Dynamic range: 0 → 10pC (!) … it is a calorimeter
  16 bit dynamic range for EVERY cell

- Very low power
  ~10mW/ch for HGROC anal
  ~5mW/ch for HGROC dig
  ~5mW/ch for everything else

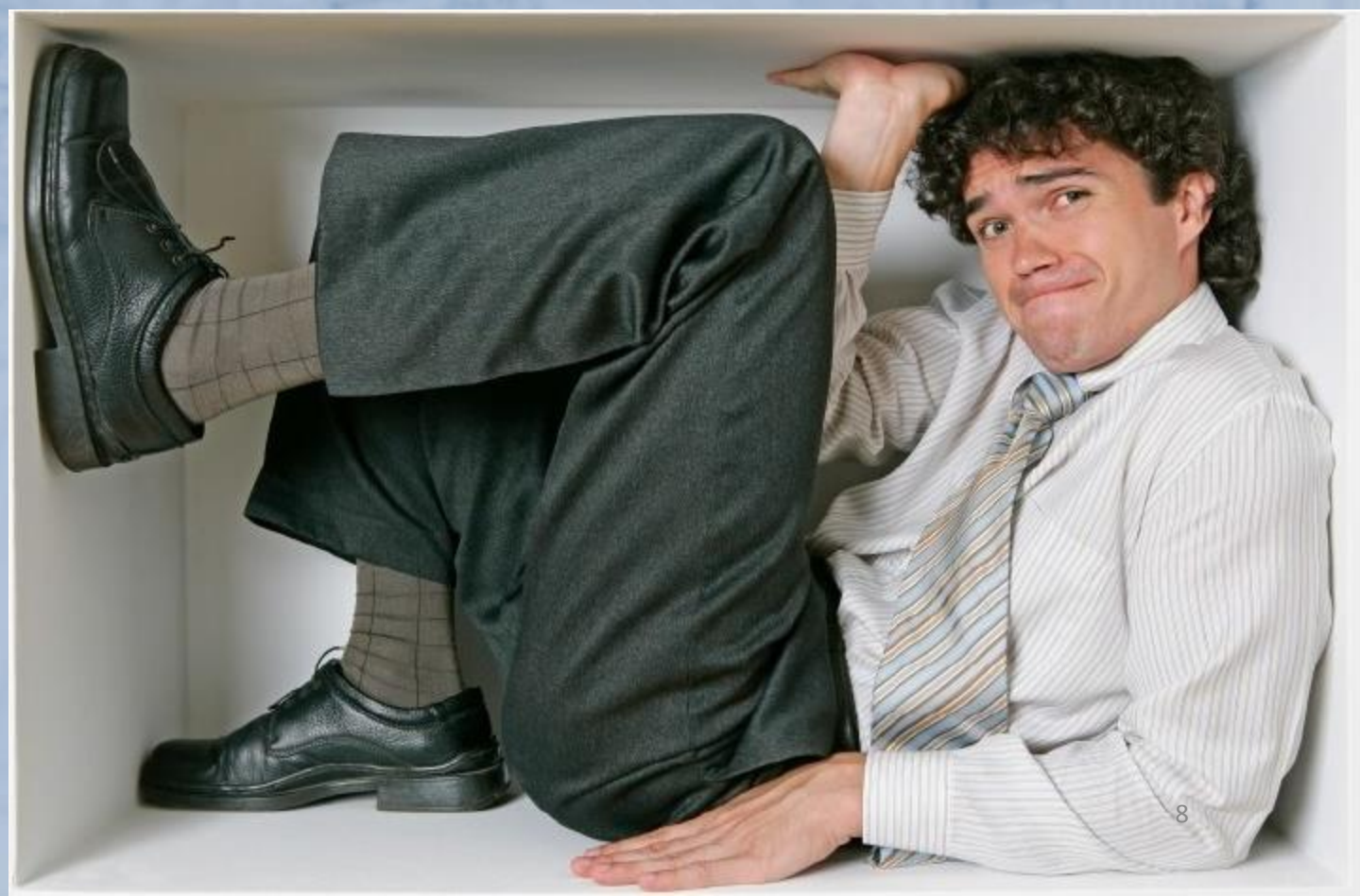
  120kW cooling / 6M chan =20mW/ch

Multi-gain:

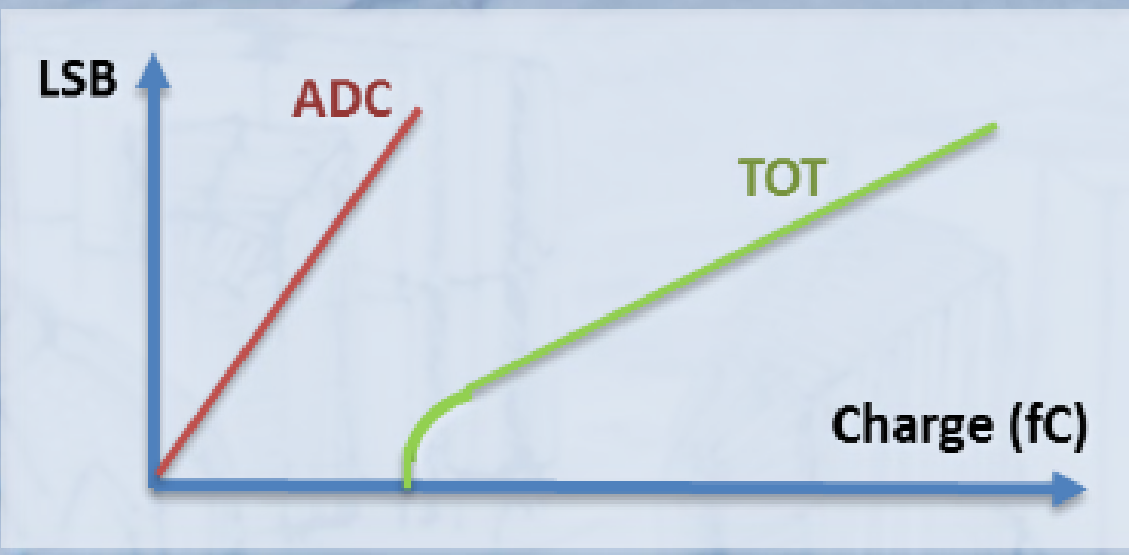
- Carefully considered

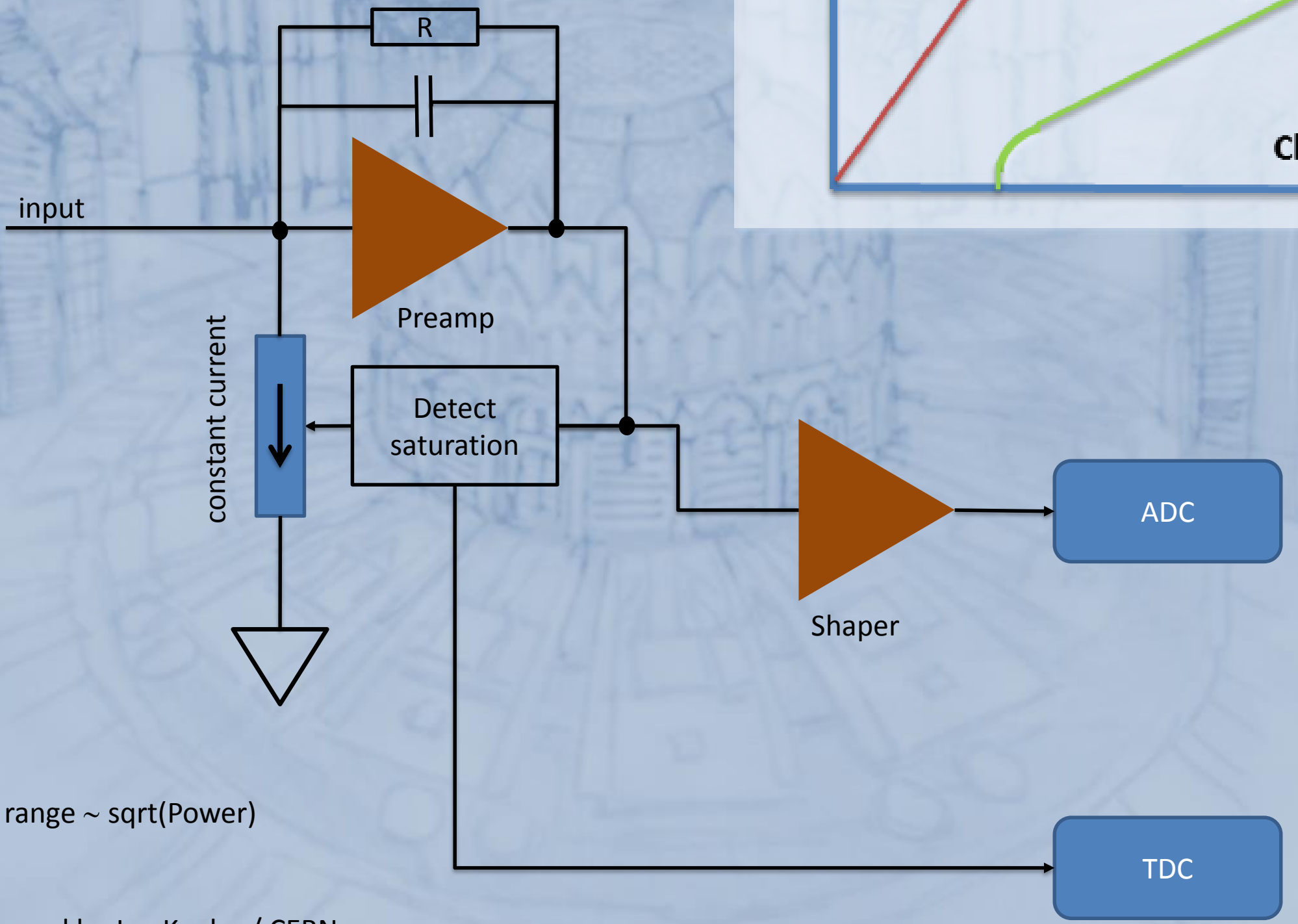
- Final decision:

  Time Over Threshold



Analog basic idea: ADC for part of range (about 1%)

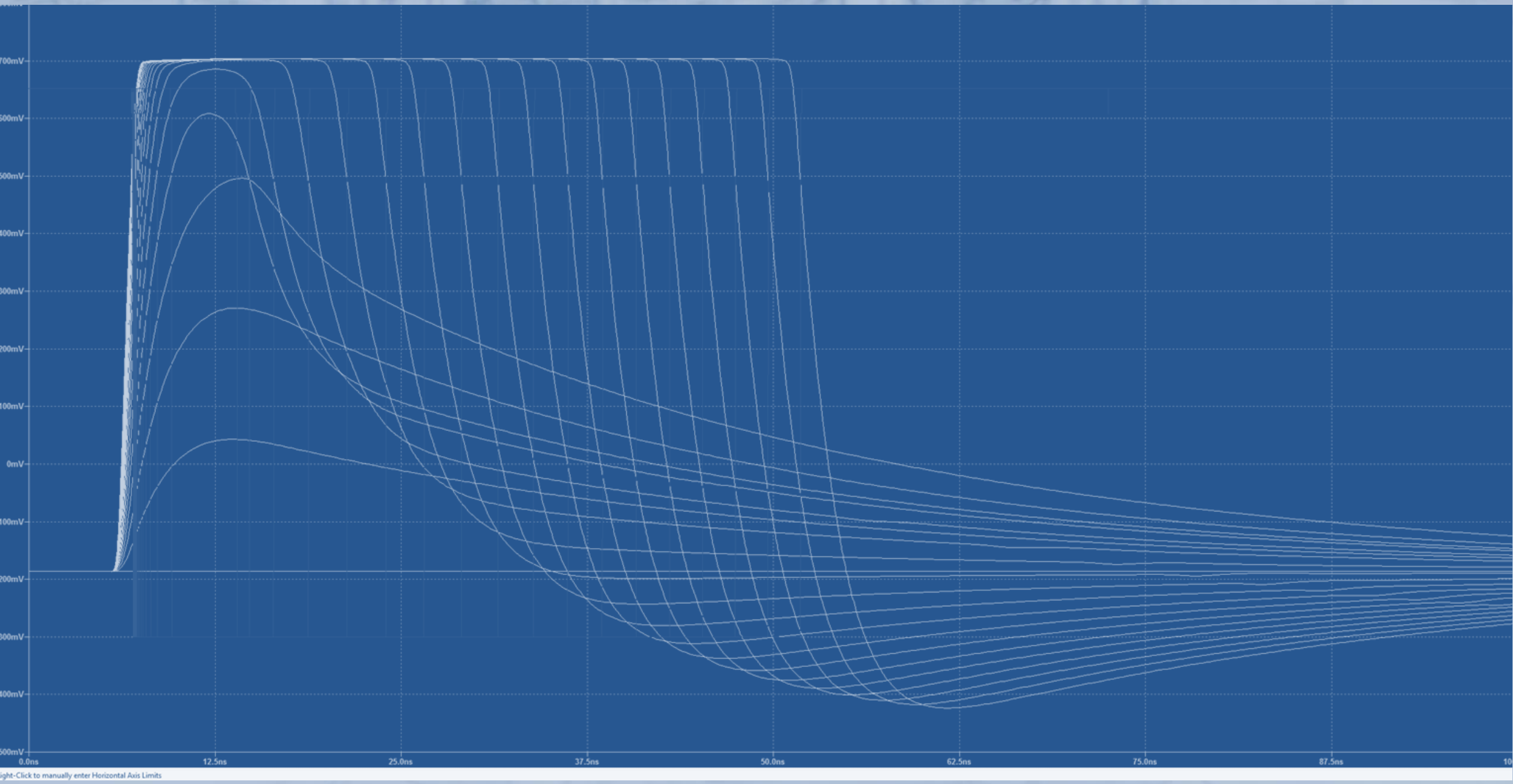




Dynamic range ~ sqrt(Power)

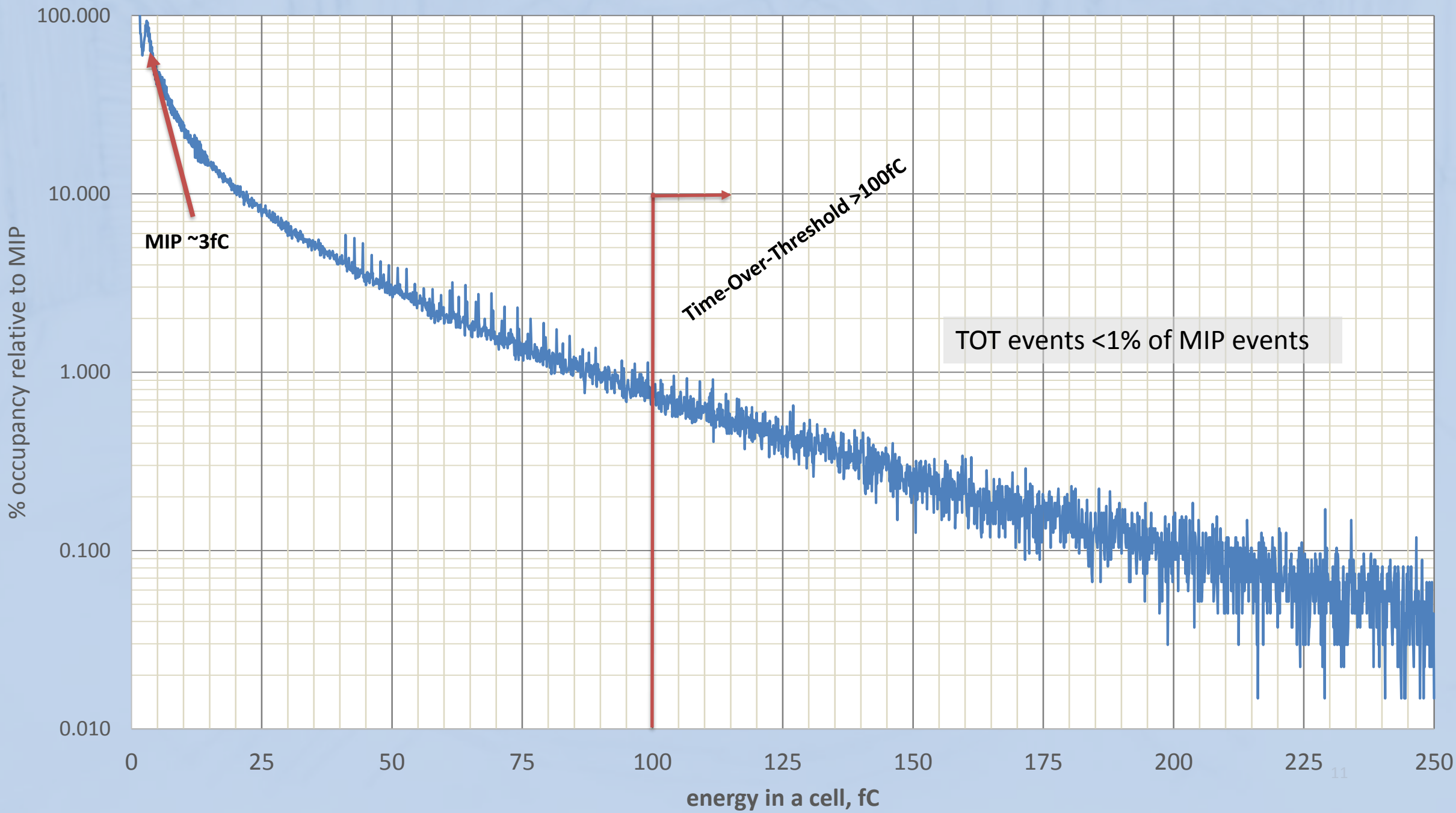
Idea proposed by Jan Kaplon/ CERN

Dynamic range improves as sqrt(Power), but not for TOT



T-O-T

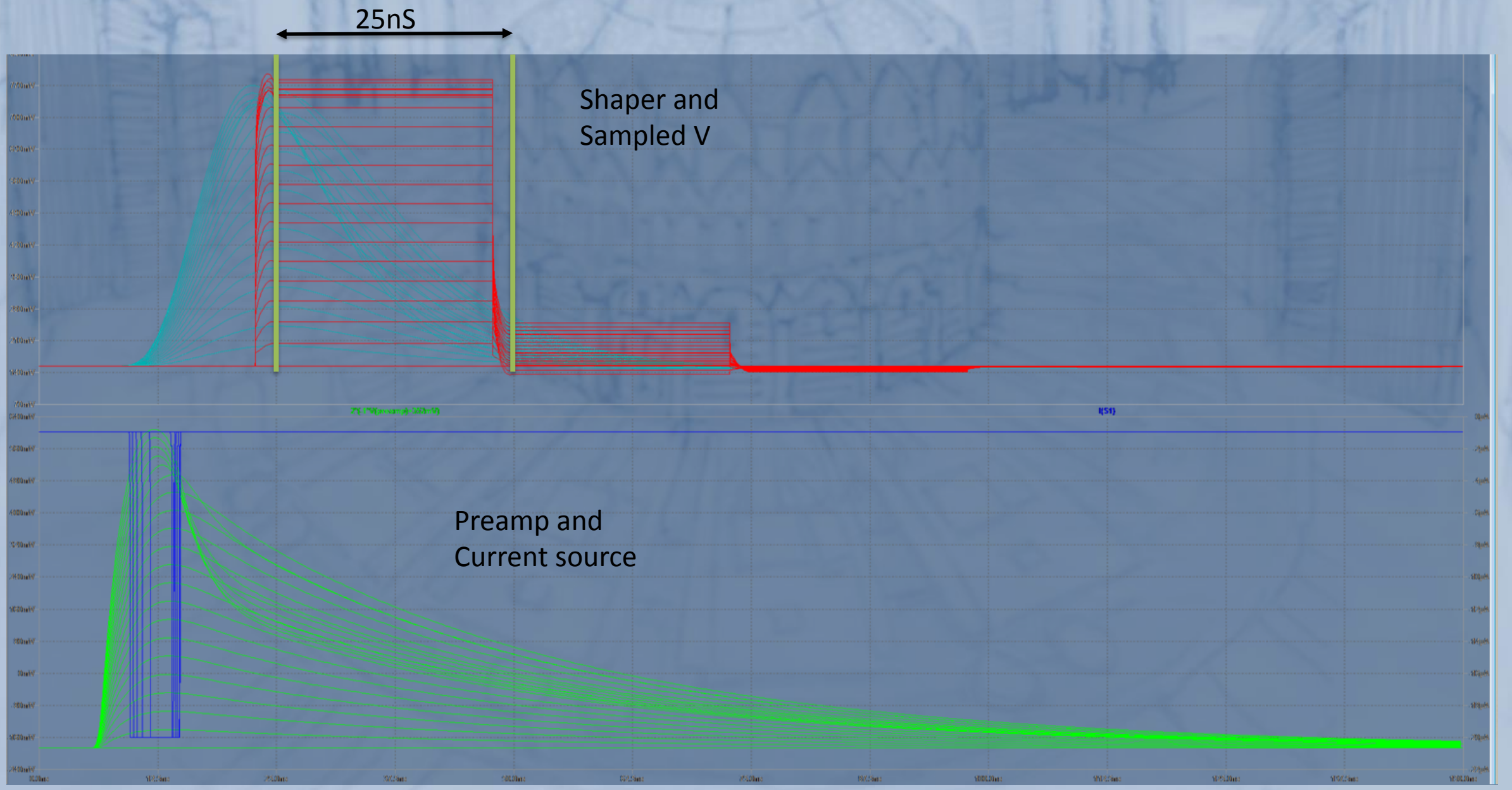
Large energy deposition is INTERESTING but RARE
Time-Over-Threshold trades TIME for



Turning on the current source can cause strange effects…

"…democracy is the worst form of Government except for all those other forms… "

At first glance, TOT gives you "free" TOA
In fact separate discriminators, separate TDCs



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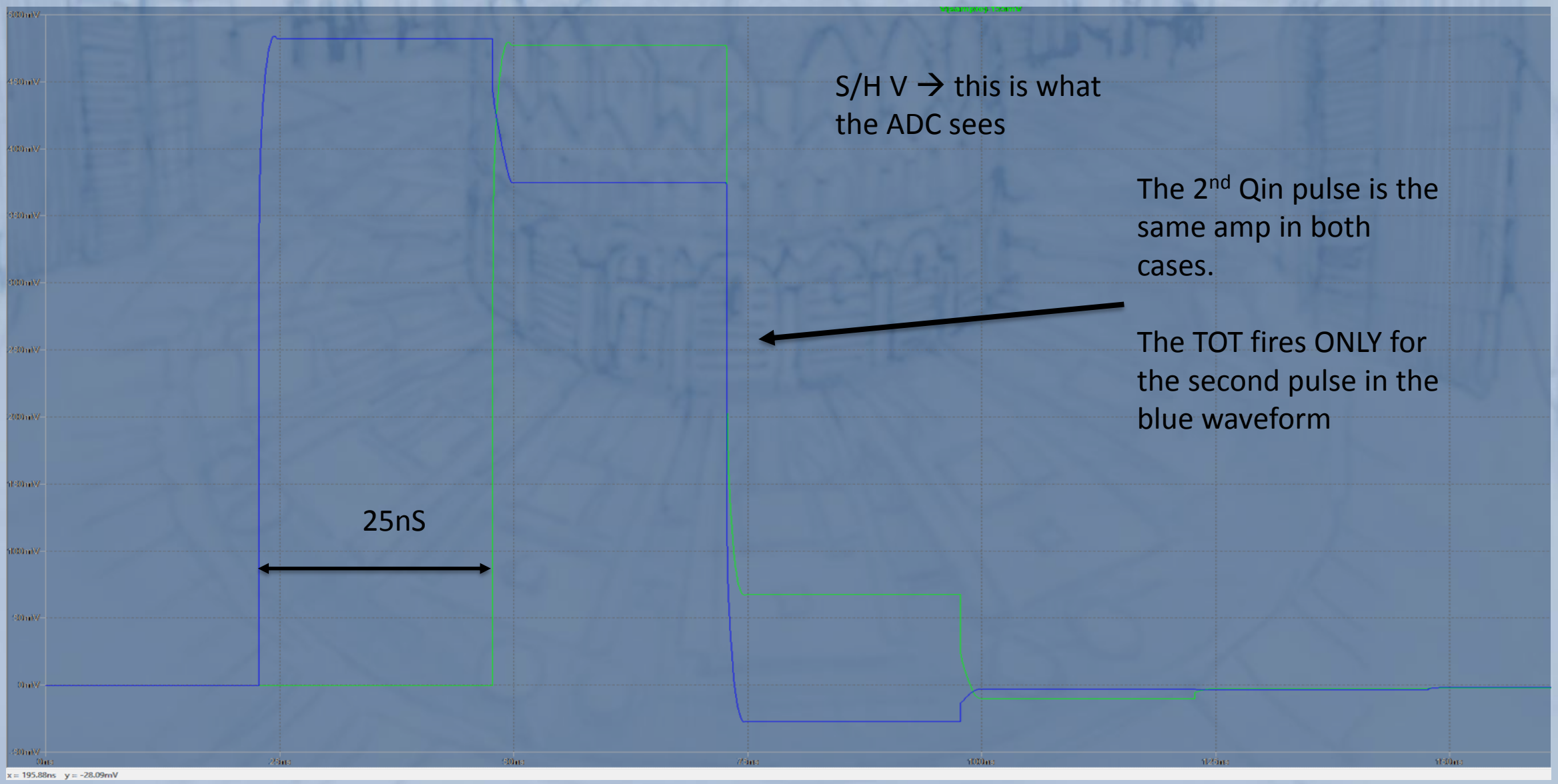


Final HGROC architecture:

HGROC: Targeting 130nm TSMC

- 64ch (for 192 cell sensors)
  72ch (for 432 cell sensors)
  + 2 extra small cells to help w MIP
  + 4 cells to help with common mode

- Dual polarity (needed for scint)

- ADC (10 bit @ 40 Mhz)
  0-100fC

- TOT (12 bit)
  100fc → 10pC (<1% occ)

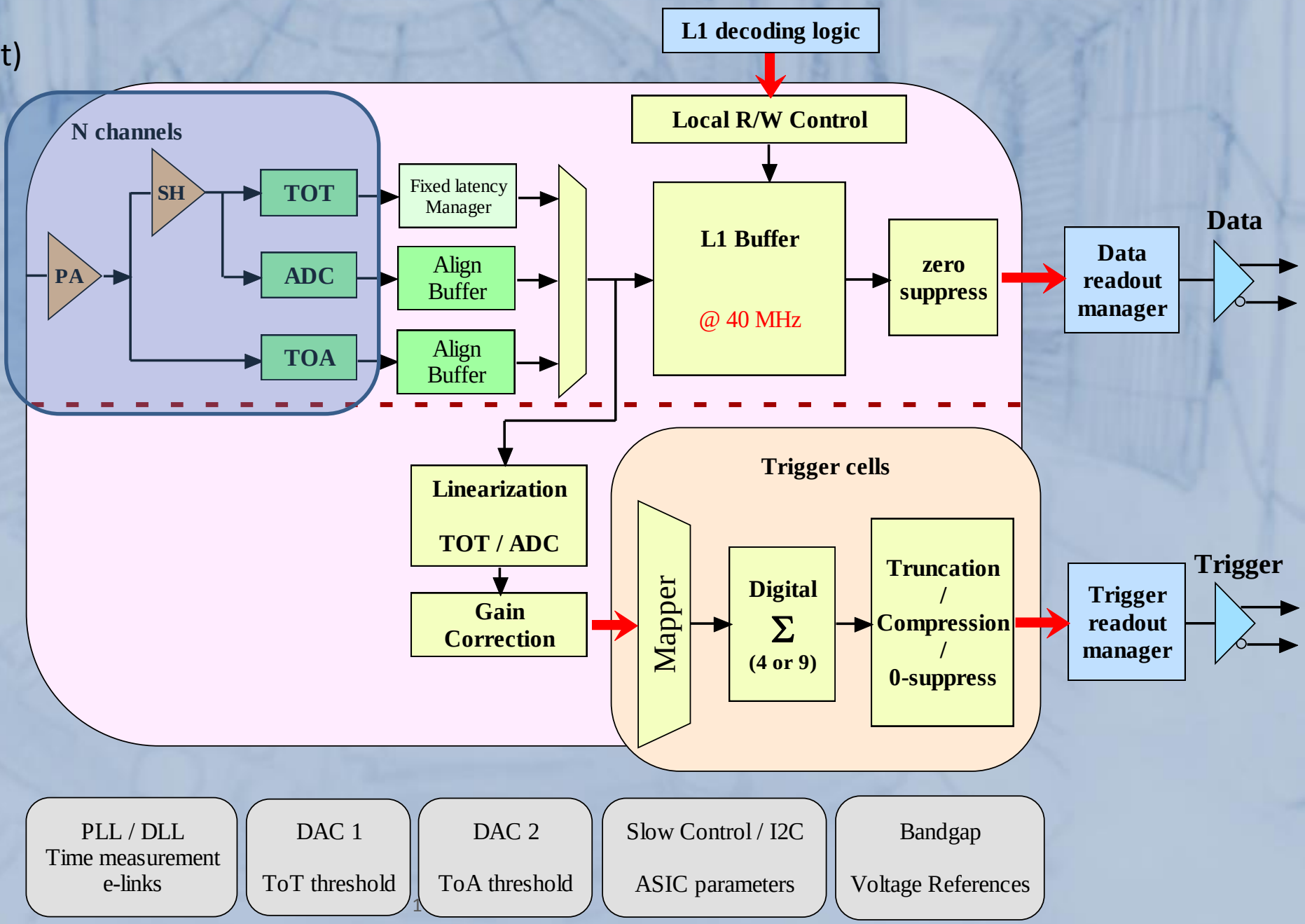
- TOA (10 bit)
  ~50ps for Qin > 10fC

- Linearized and summed trigger output every xing logarithmic, ~3% resolution
  5gbps / HGCROC

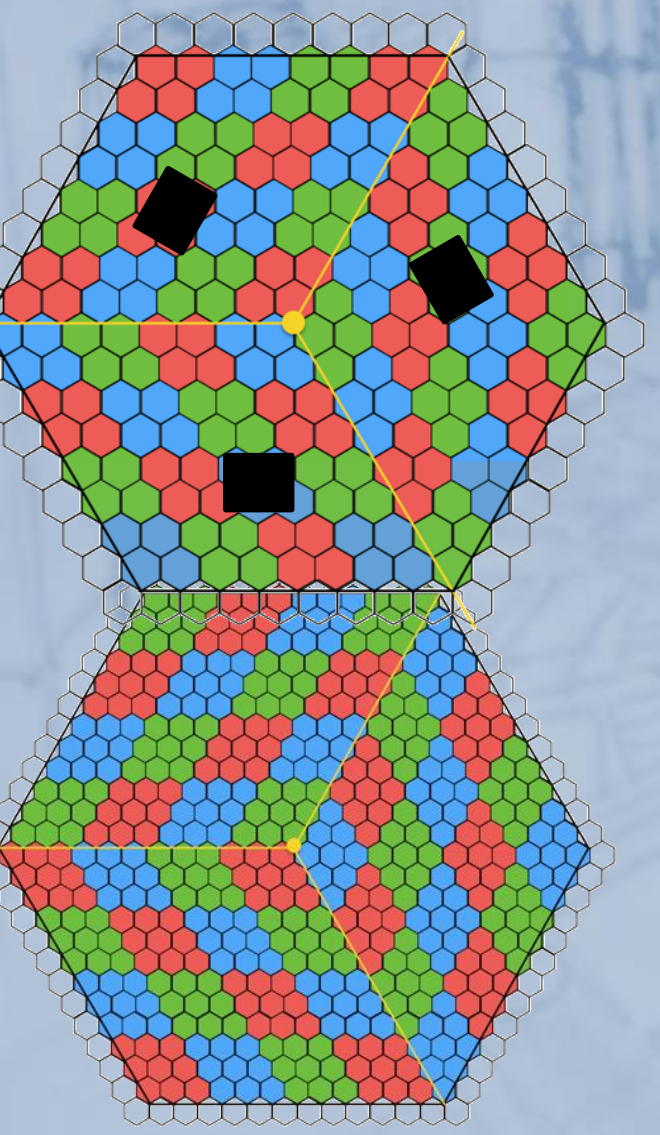
- DAQ readout on L1 accept
  up to 1MHz readout
  full resolution ADC/TOT, TOA
  zero suppressed ~1/3 MIP
  512 xing buffer

- 320MHZ TTC link

- I2C control for all parameters

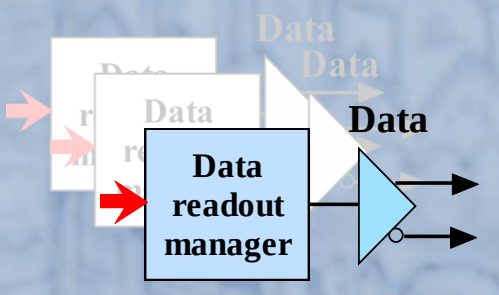


Final Readout architecture: two paths

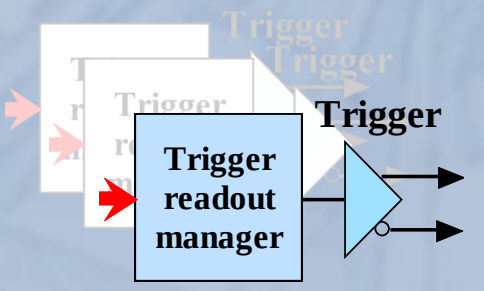


Cells are summed by 4 (for 192) or 9 (432) into Trigger Cells → FP (4+4) format
Trigger data must flow every xing (40MHz) – good resolution, good segmentation
(every other layer in the CE-E, every layer in the CE-H)

Individual cells are readout with full resolution and TOA on L1 accept
Full resolution, full segmentation



HGROC DAQ path
All cells/ all info above 0.5MIP
Only on L1 accept (1 MHz)
1 elink / HGROC at 1.28gbps
3 (6) elinks/sensor (1 per chip)

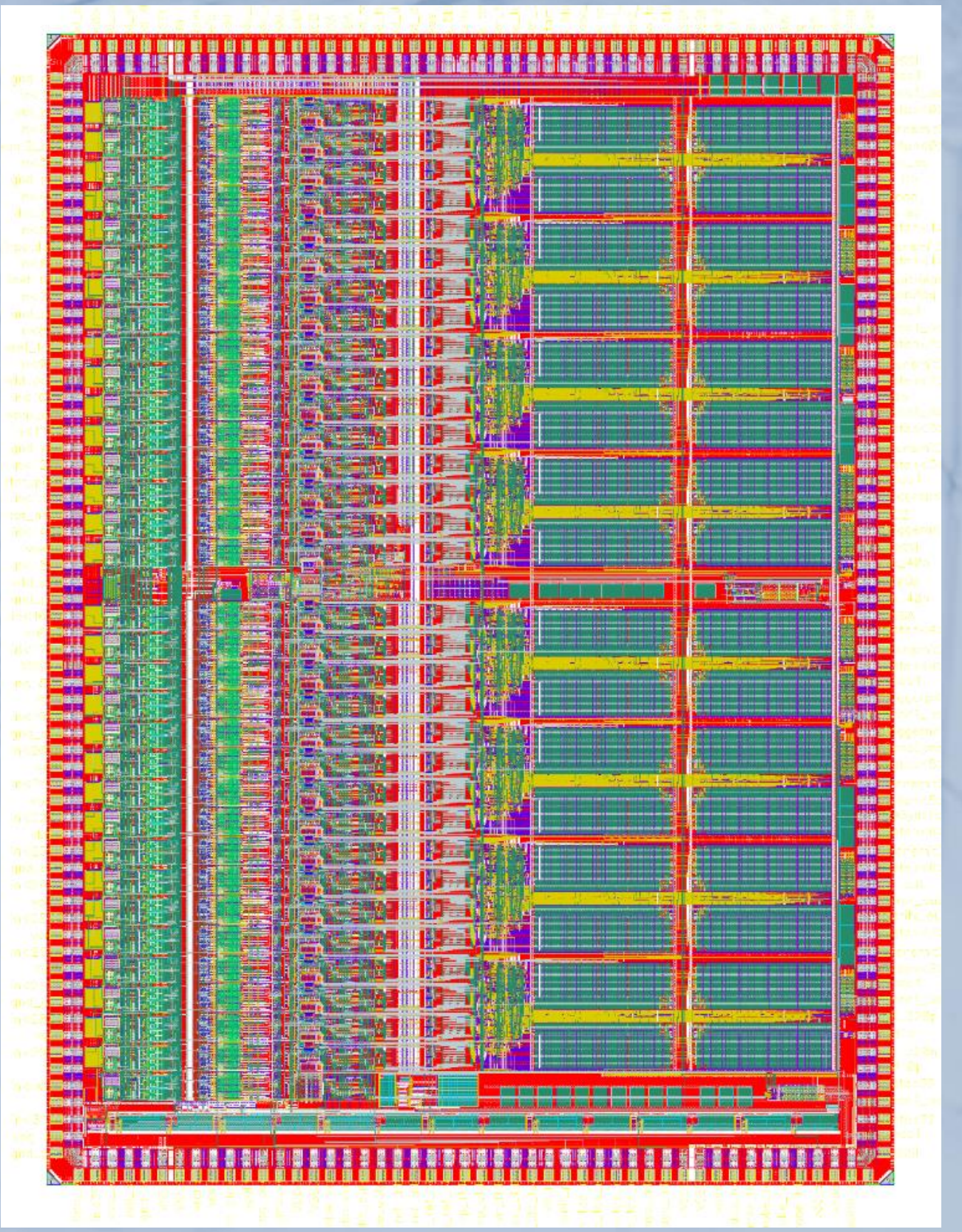


HGROC trig path
48TC/ sensor module (3 or 6 FE)
8bits FP for every TC, every 25ns
4 elinks / HGROC at 1.28gbps
12 elinks/sensor at 1.28gbps

HGROCv1 → in hand, being tested

- 7x5 mm²
- 224 pads
- 32 ch + 1 SWGPA (ch33)
- 8 blocs of 4 ch + digital
- Analog on top
- Bias, DLLs, CKs in the middle
- DACs, REFs at the bottom
- Analog and digital probes
- Bias accessible on pads
- Several bias tunable by DAC
- Slow control separated

- Substrate noise coupling reduction
  - Two separated Deep-Nwell underneath analog and mixed channel
  - High resistive substrate between analog, mixed and digital parts



Analog and Mixed channel: HGCROC v1 (130nm TSMC)

Input DAC: leakage compensation over +/- 10µA to 300nA accuracy (30 mV preamp output DC shift)

Cf = 0,1 0,2 0,4 0,8 fF

Cf_comp = 0,1 0,2 fF

Rf = 25k, 100k, 1M

itot: 6bits global setting, 80µA max, 40µA default

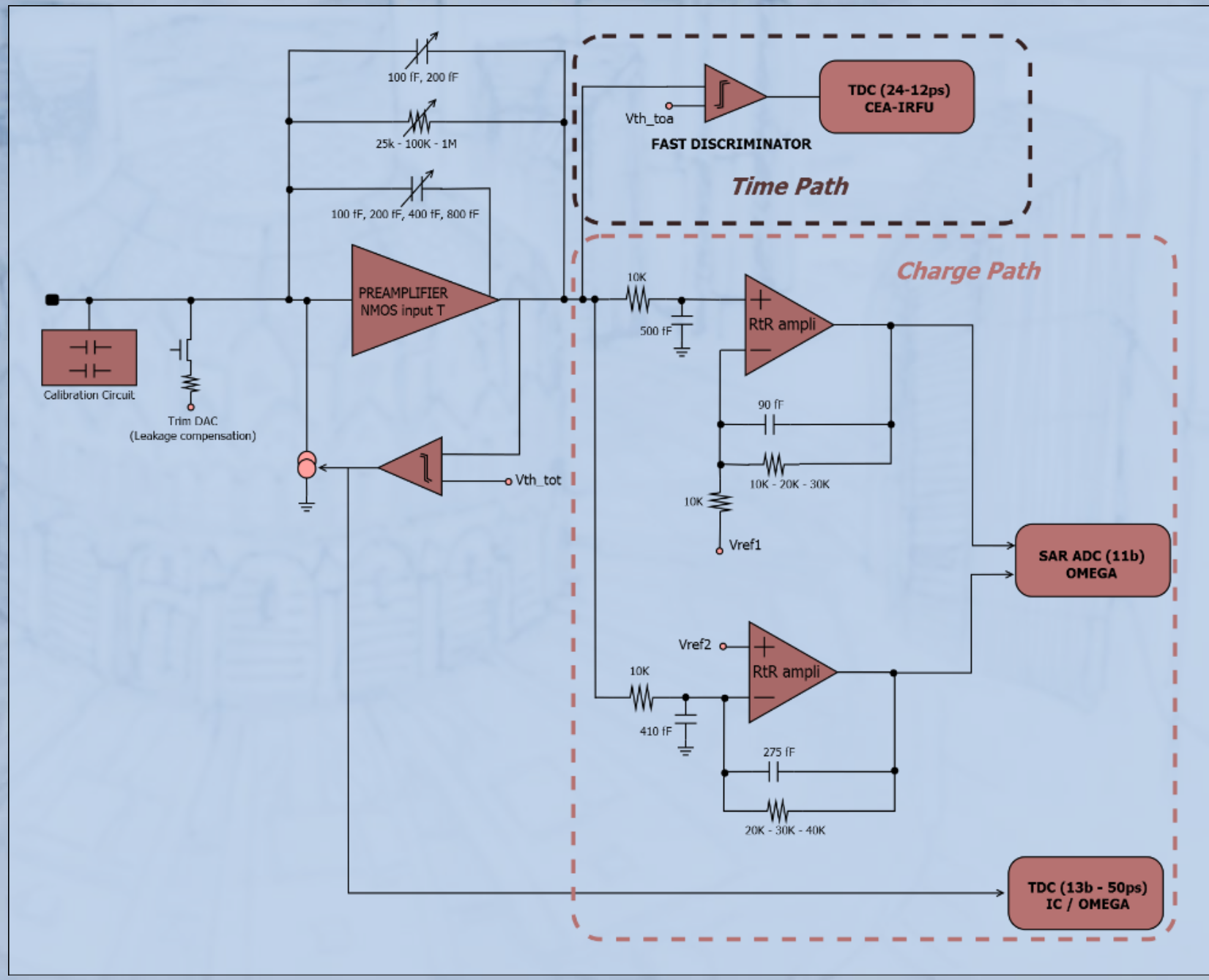
Vth_tot: 100mV – 1,2V dynamic range, 7bits global (0;1,2V;9mV), 5bits local (20mV;0,625mV)

Single-to-differential shapers, 20-30ns peaking time; gain 2, 3, 4

Vref1: 0–700mV, 7bits global

Vref2: 0–700mV, 7 bits global, 5bits ch

Vth_toa: 0–700mV, 7bits global, 5bits ch



~4.5mW Preamp/Shaper/Discr
+ ~same for ADC/TDCx2

Power dissipation @ 1,5V supply

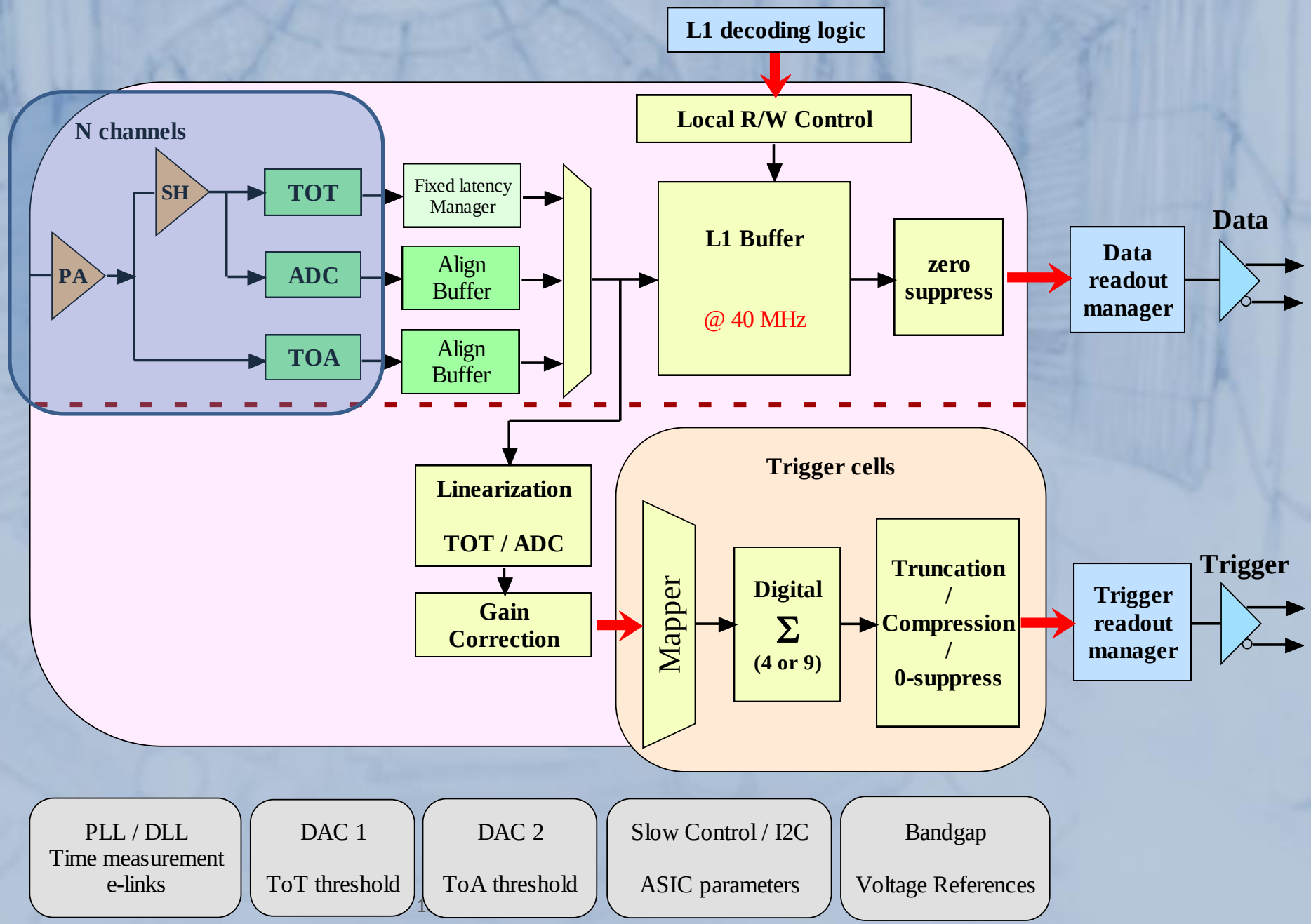
- Vdda (preamp): 1,6mA
- Vdd (tot): 160µA
- Vdd(shaper, toa): 1,1mA

HGROCv1 – first proto

now testing

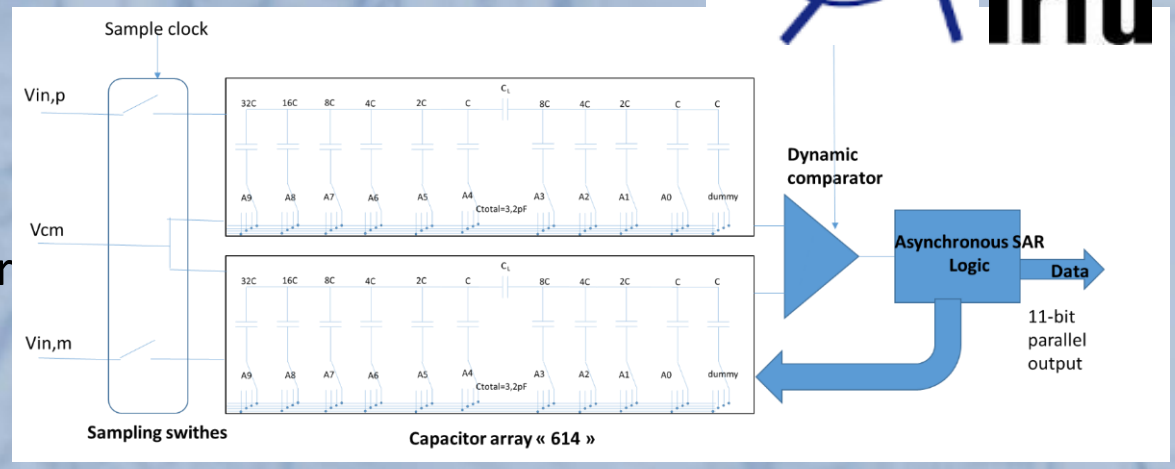
HGROCv1: implemented in 130nm

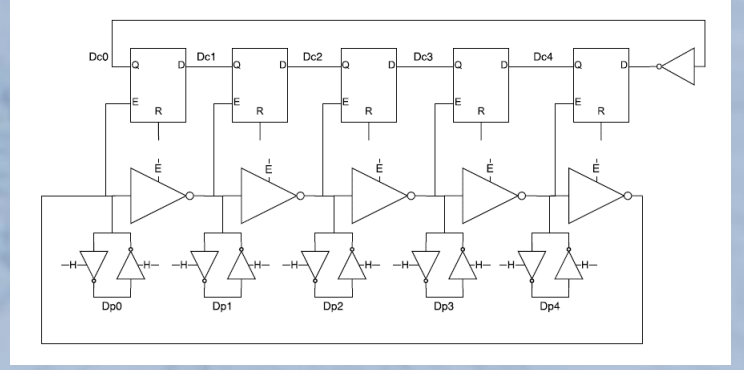
- Preamp gain adjustable 4bit
- New shaper without SK
  - In a next version, with SK and tunable shaping time and gain
- Decay time given by R_{f_pa}
  - 25K
  - 100K
- New TOT architecture
  - Gain adjustable by SC
  - Undershoot ➔ dead time
  - In a next version, find a way to remove/reduce it (dynamic reset)
- New TOA fast discriminator
  - In a next version, higher preamp bias current and fast output to improve the time measurement
- Local 5bit DAC to adjust the Vrefs and the thresholds
- Local input current DAC to compensate the leakage
- Internal calibration circuit
  - Low range up to 600 fC
  - High range up to 12 pC

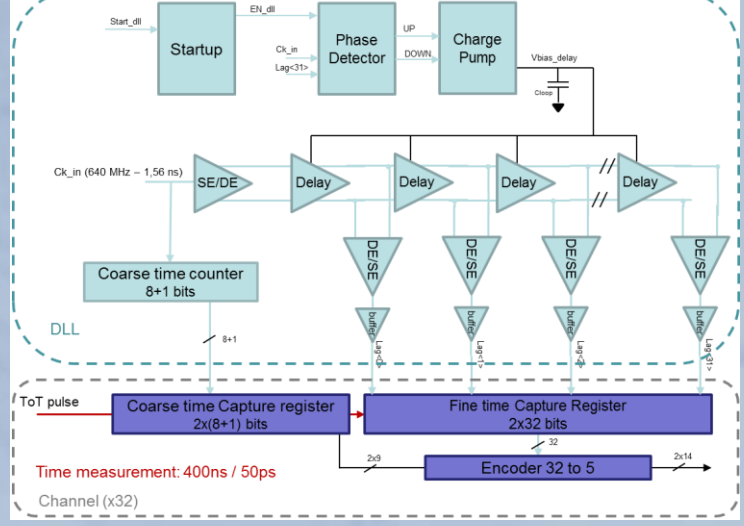


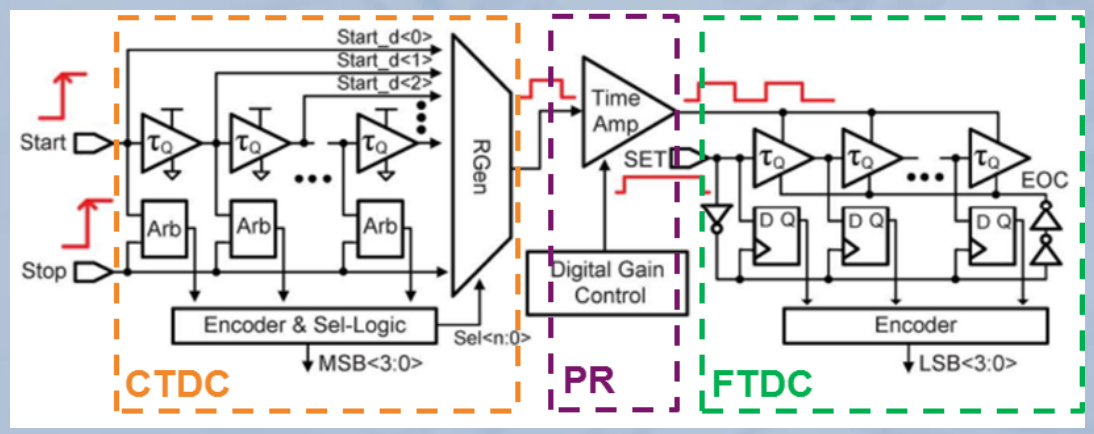
New mixed-signal circuits

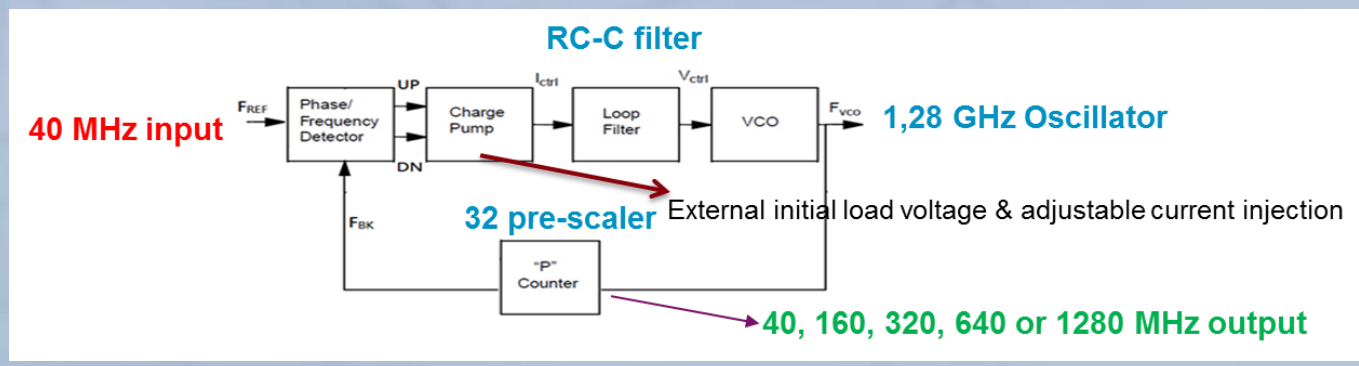
- ADC SAR
  - Inspired from Krakow design, 11 bit
- 2 TDCs for TOT
  - IC design, 50ps/200ns, based on a ring oscillator
  - OMEGA design, 50ps/400ns, based on a global DLL r
- TDC for TOA
  - CEA-IRFU design
  - 10/11 bit
- PLL
  - CEA-IRFU design
  - 40MHz input clock
  - 1,28GHz running frequency





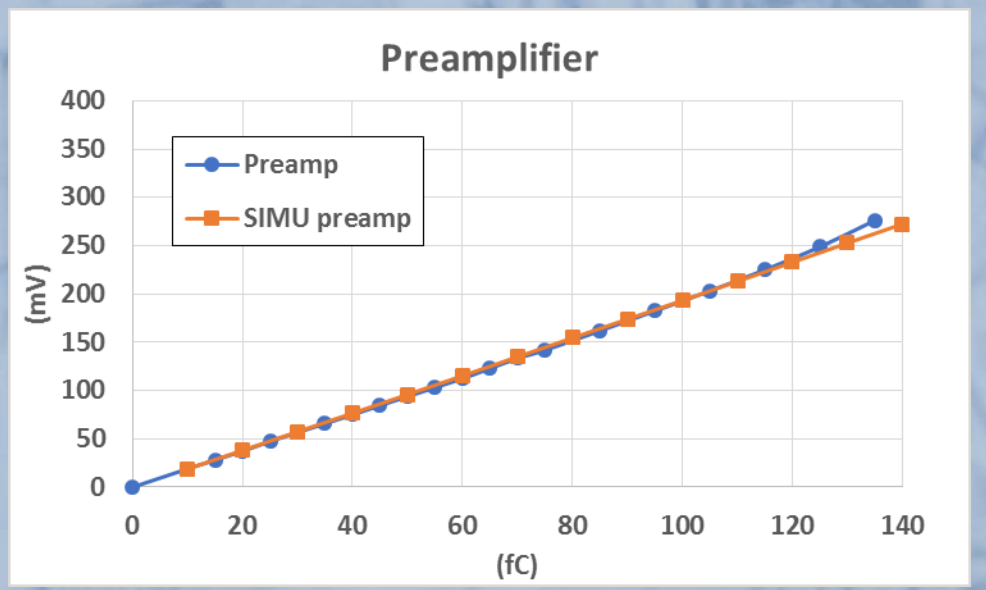


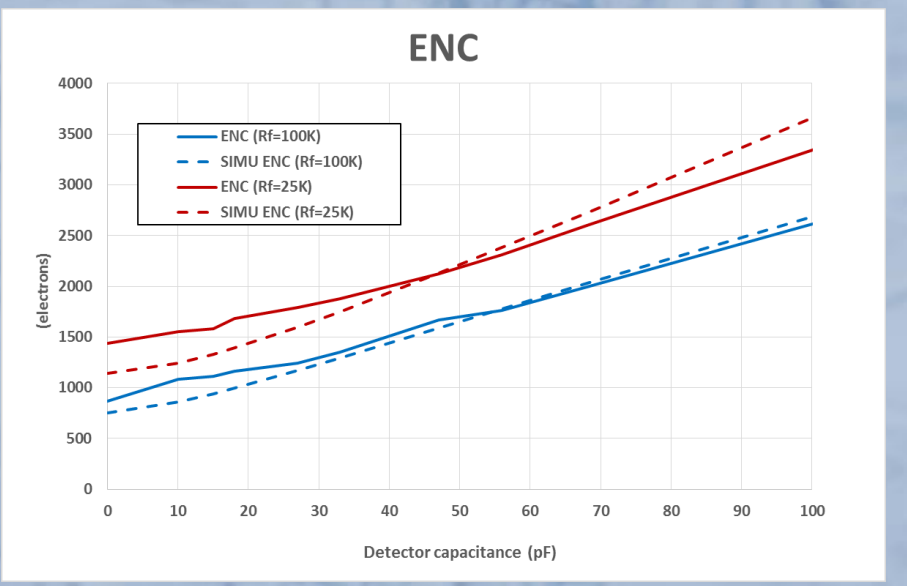


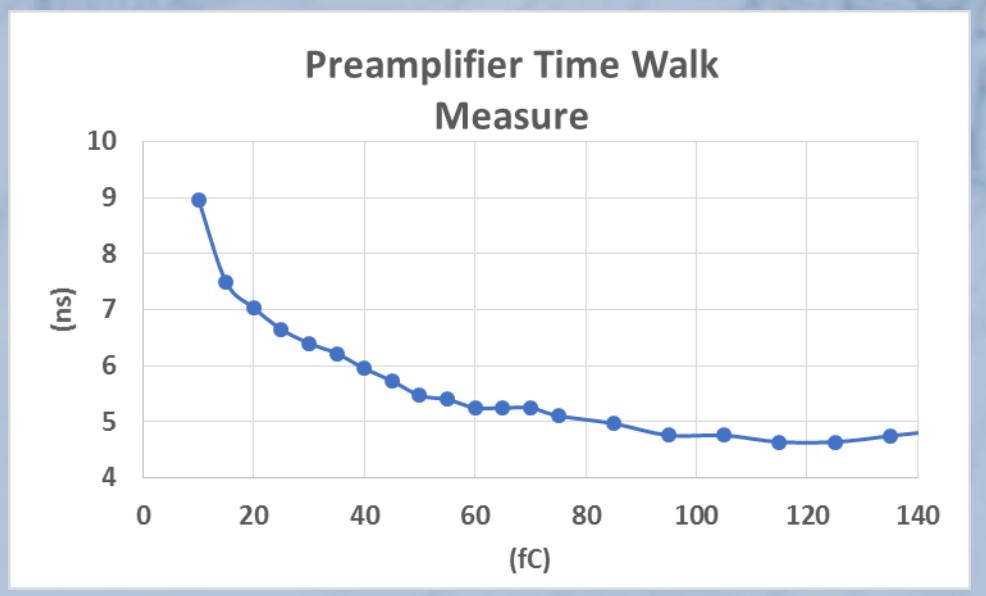


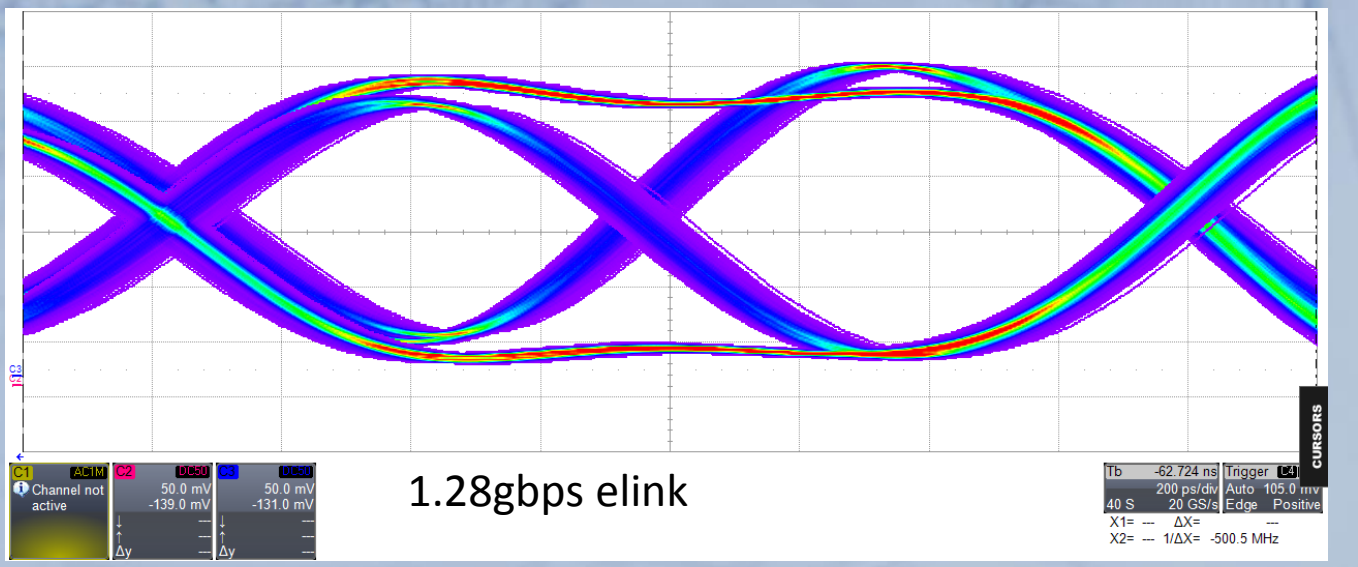
Testing now under way

- Some things look pretty good





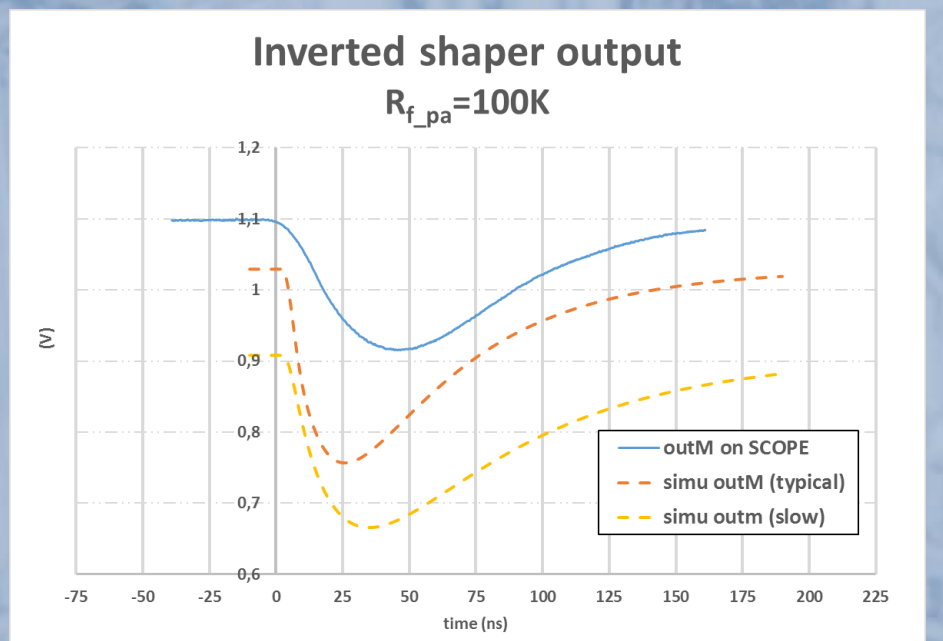


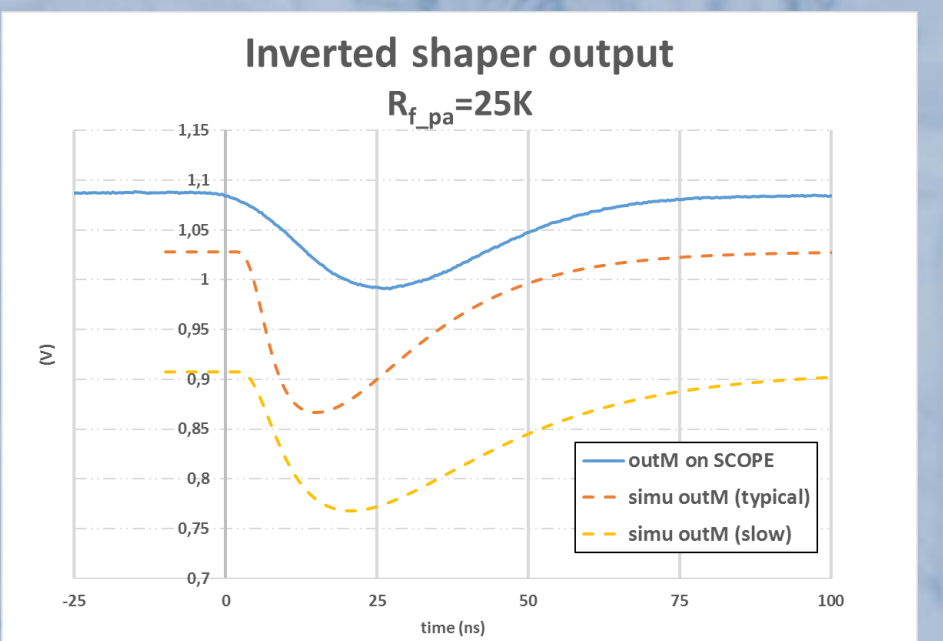


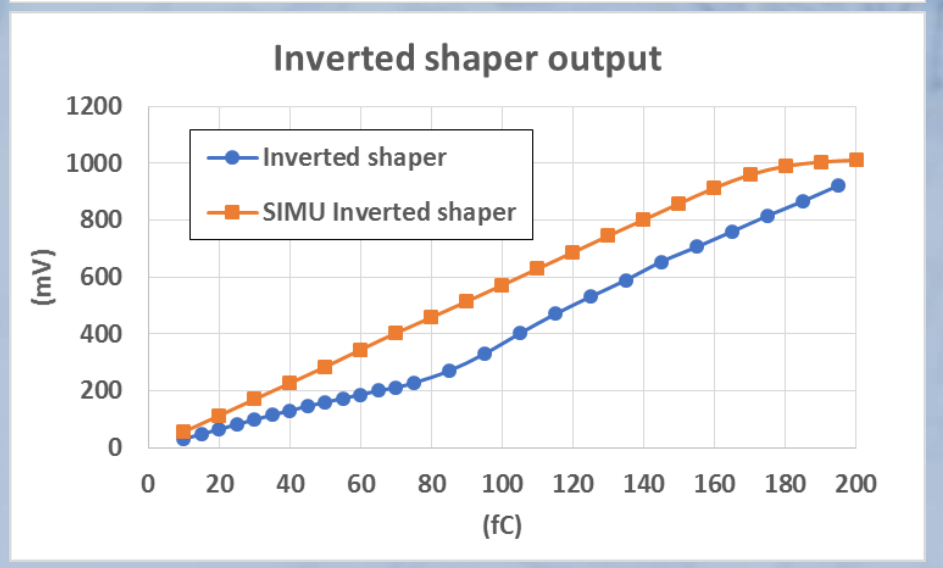
1.28gbps elink

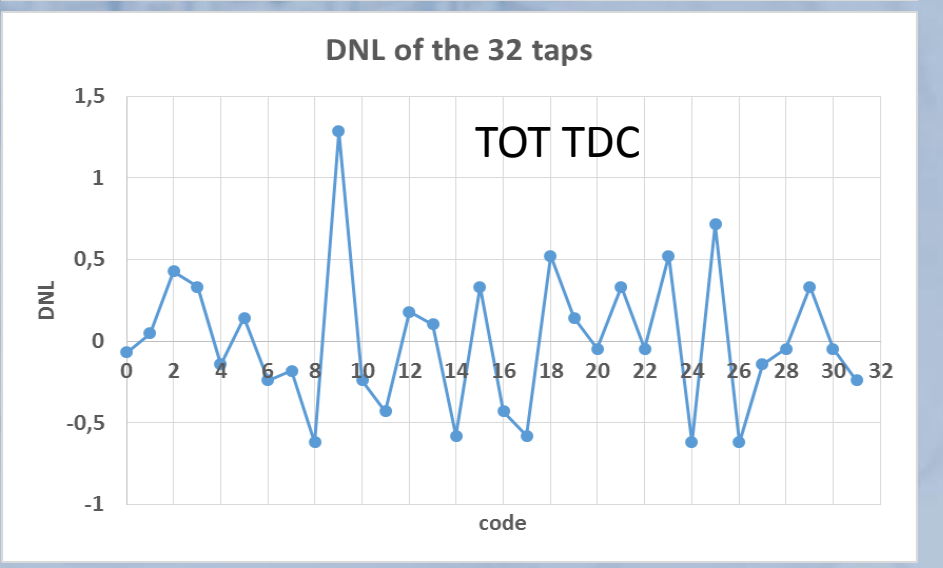
Testing now under way

- Some not as expected

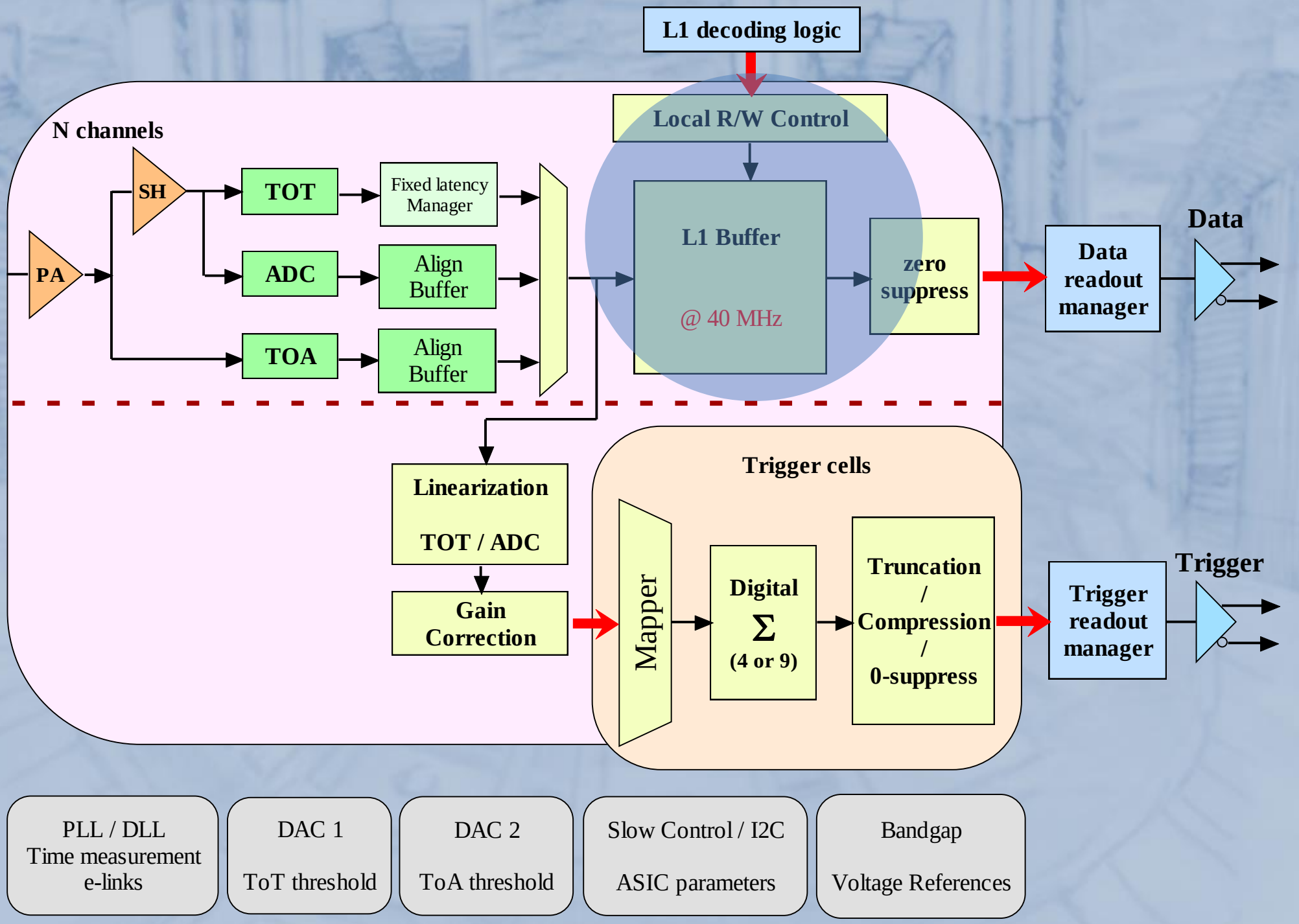






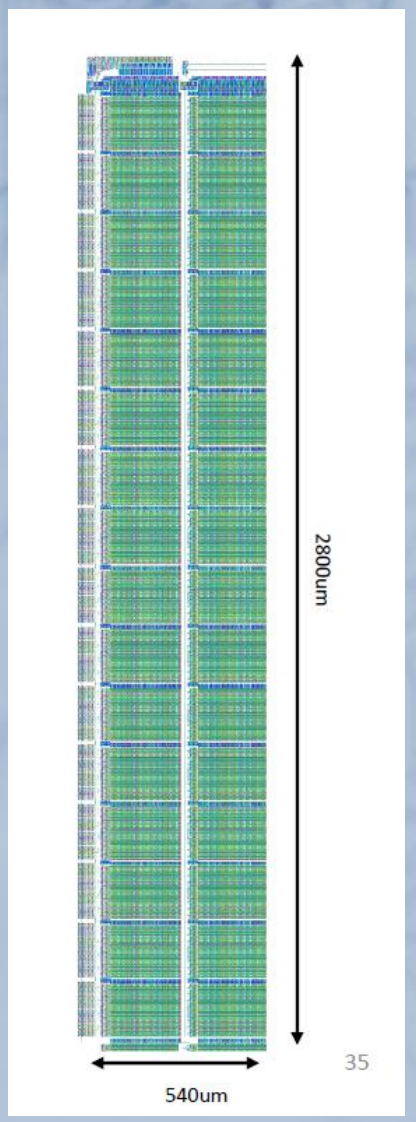


Digital example: L1 buffer



Digital part development (130nm) (not in HGROCv1)

- L1 buffer requires memory that is 32 wide by 512 deep for each chanel
- SRAM is “easy” with standard library



SRAM: 256 x 512, write at 40Mhz, read at 1.5Mhz
Area= ~1.5mm^2, Power=~22mW= 3mW/ch (?!)

CERN group [G. Bombardi, A. Marchioro, T. Vergine] design dynamic memory (20uS retention at 50C minimum)

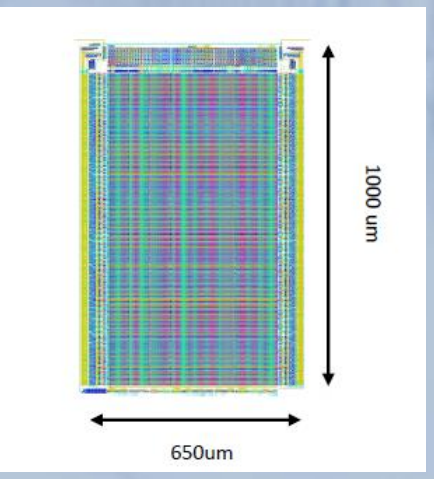
Power = < 0.4mW/ch (not 3!) , Area= 0.65 mm^2

Zero Suppression logic also requires careful attention

The total power allocated to the digital part of HGCROC is 5mW/ch

SRAM

DRAM



Two paths continued

HGROC trig path
48TC/ sensor module (3 or 6 FE)
8bits FP for every TC, every 25ns
4 elinks/HGROC at 1.28gbps
12 elinks/sensor at 1.28gbps

HGROC DAQ path
All cells/ all info above 0.5MIP
Only on L1 accept (1 MHz)
3 (6) elinks/sensor (1 per chip)

Trig eLink Concentrator (TrigEcon) (65nm digital ASIC)

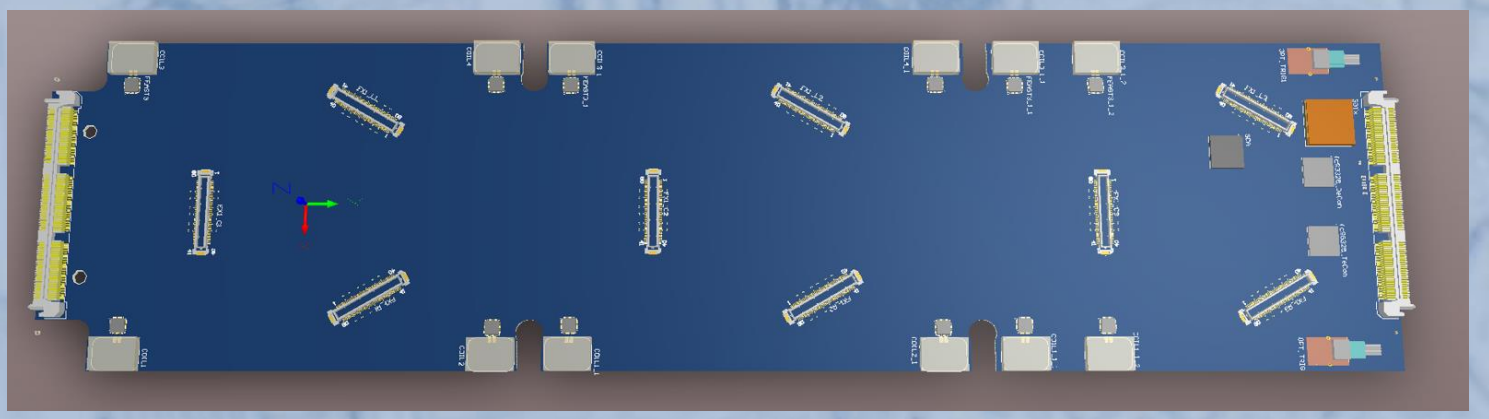
DAQ eLink Concentrator (DaqEcon) (65nm digital ASIC)

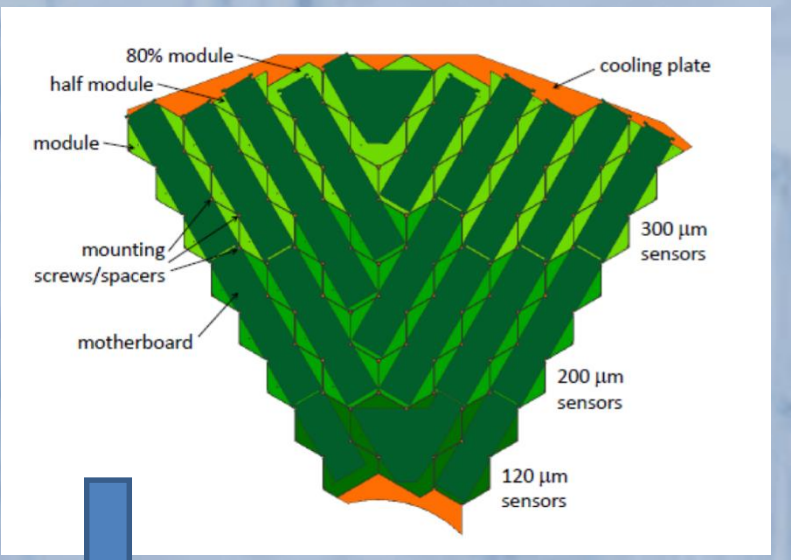
lpGBT

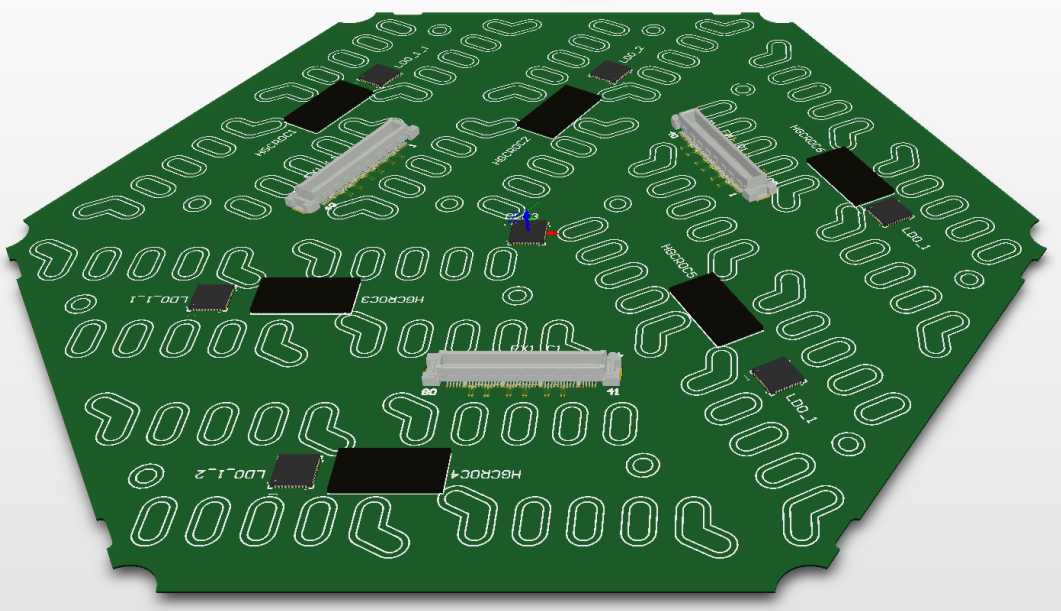
VL+
4TX
1RX

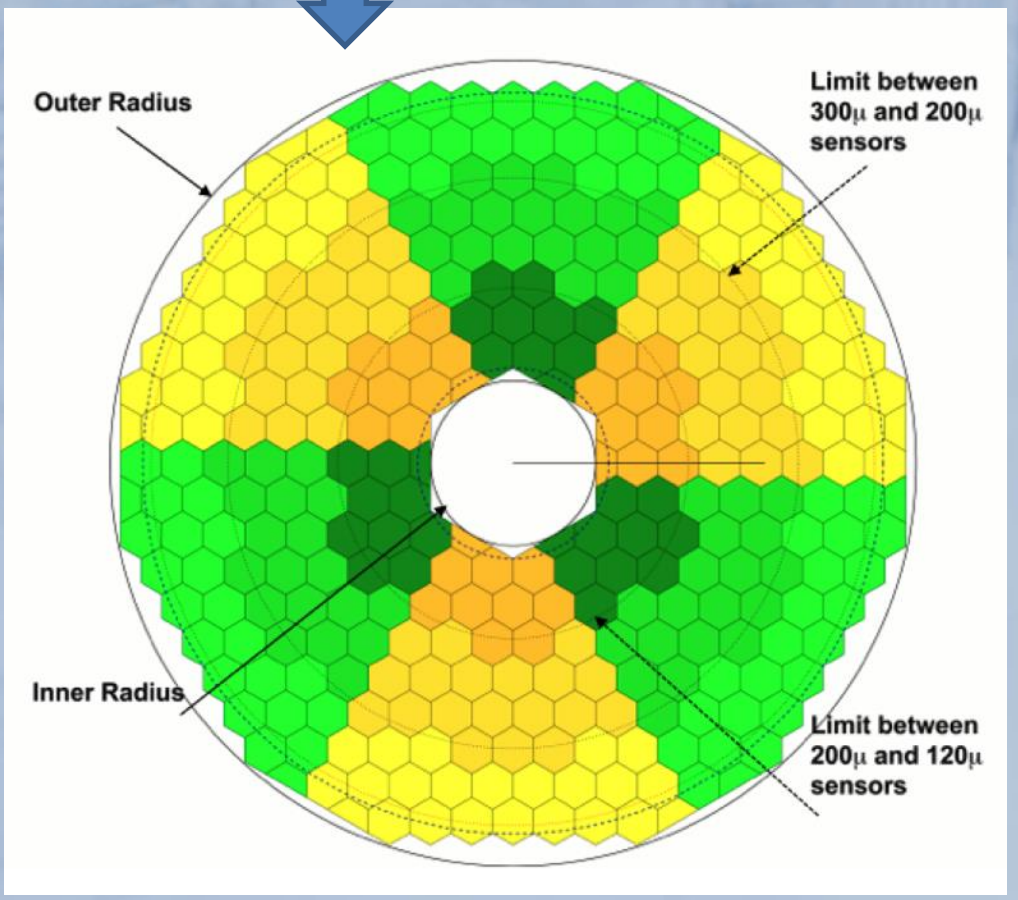
Panel (Motherboard) typically connected to 3 sensor modules

Next steps: Moving data out of the sensor, prototype eCons,



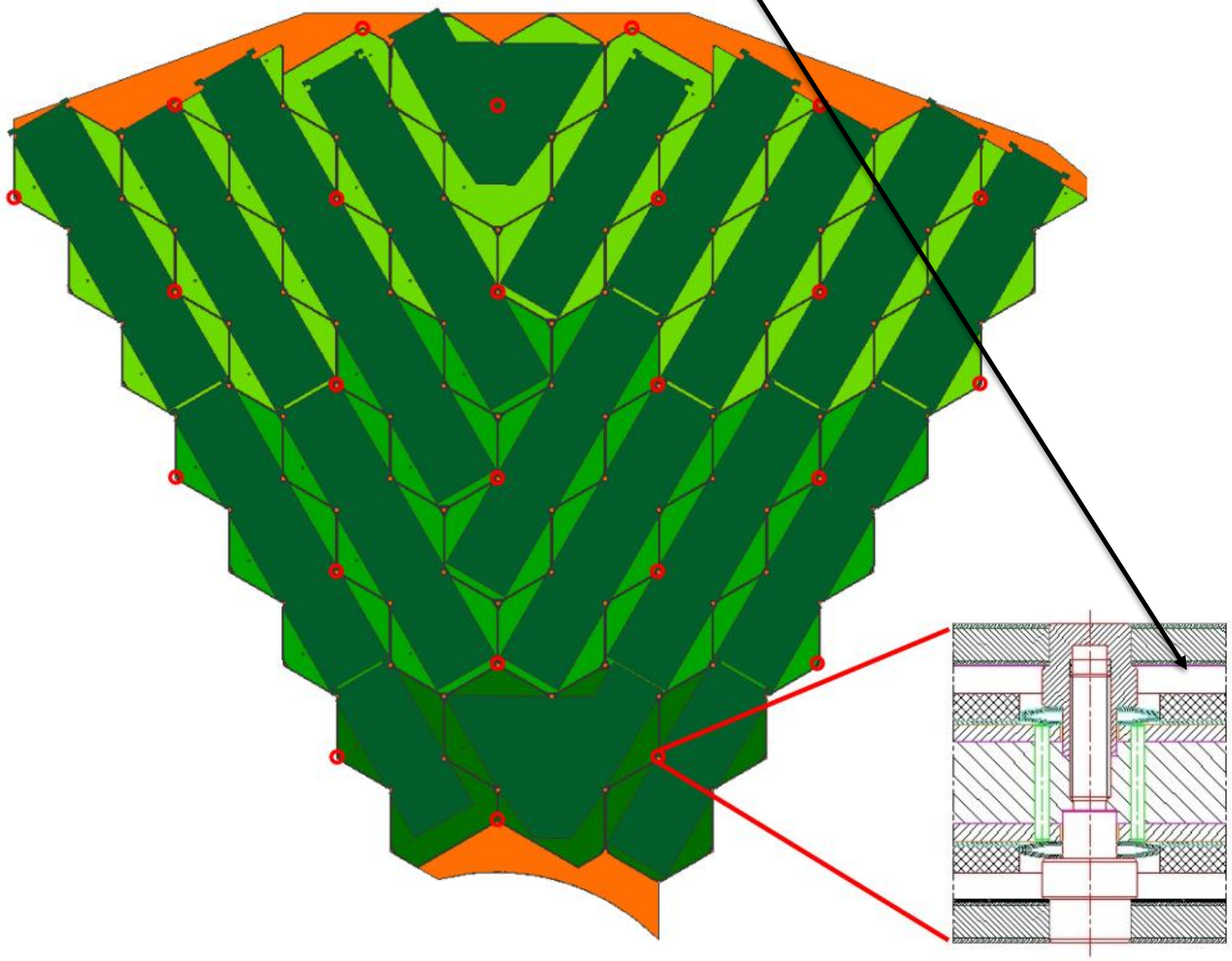


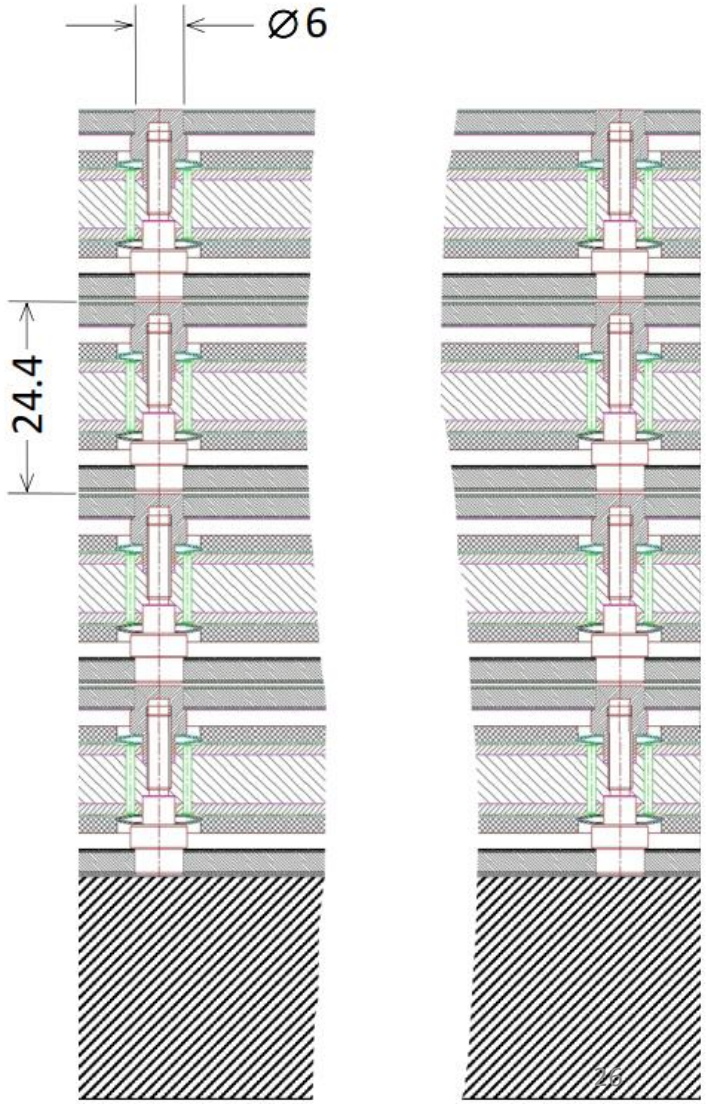




The ACTUAL box

All electronics (including optical components) must fit in this space.
Fighting to minimize this space while staying realistic.

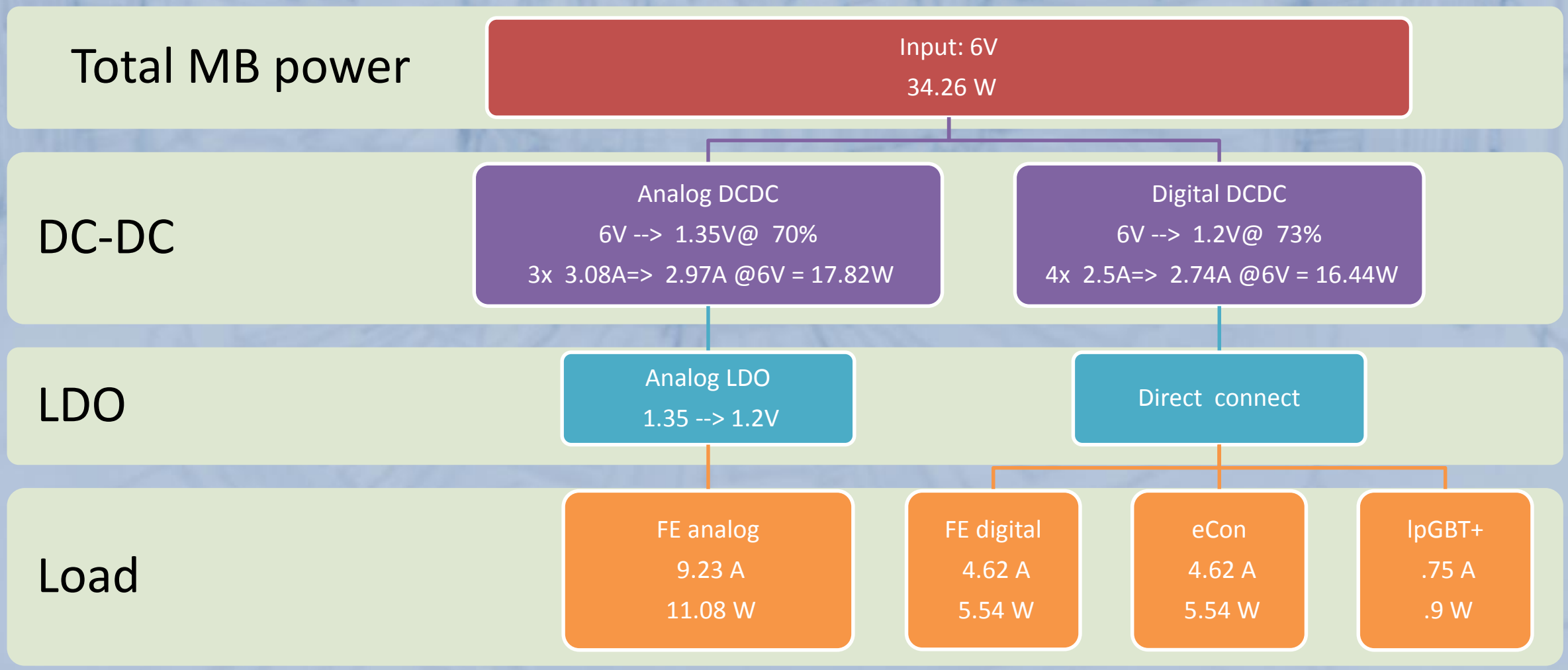




Power model for MB

Modules:	432ch:	2	192ch:	1	1086
Current per ch in mA	FE analog pwr:	8.5	Dig pwr:	4.25	
	eCon pwr :	4.25			
Other info	lpGBT+ (mA)	750			
	LDO dropout(mv)	150			
	Max FEAST current (A)	3.2			

Total MB power

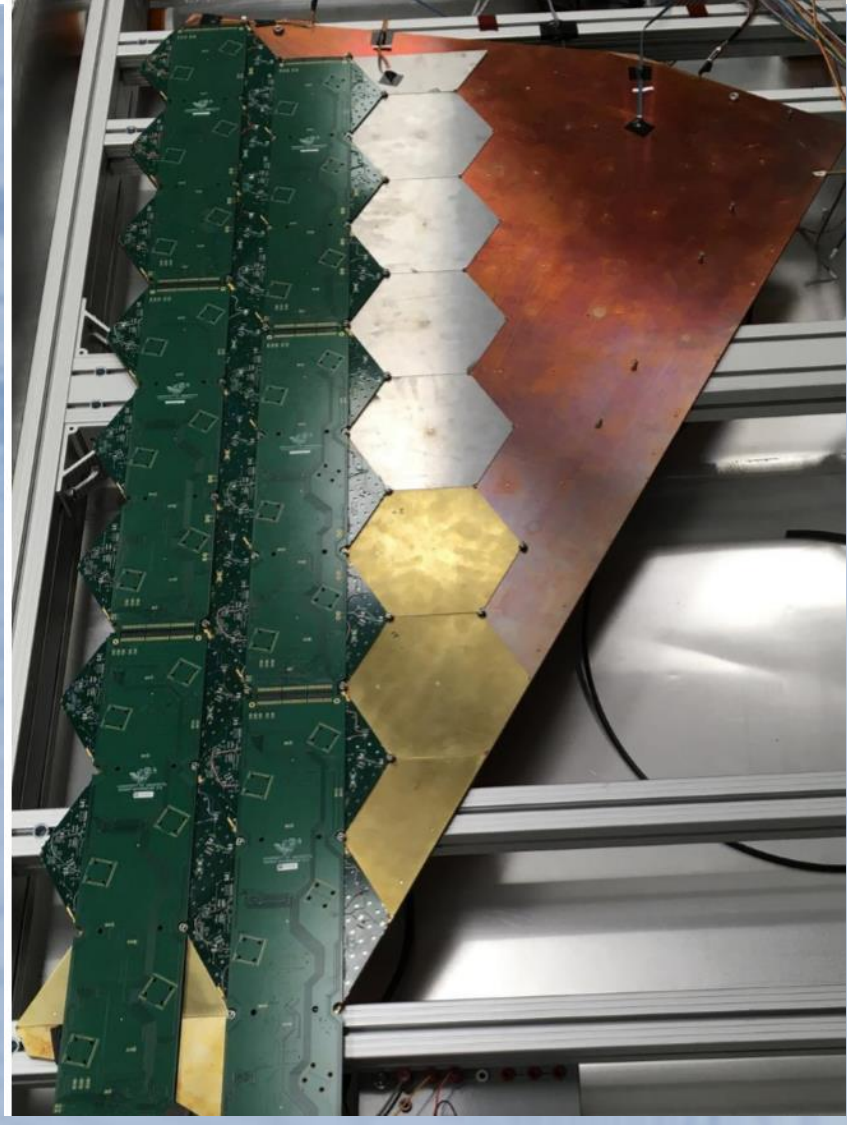


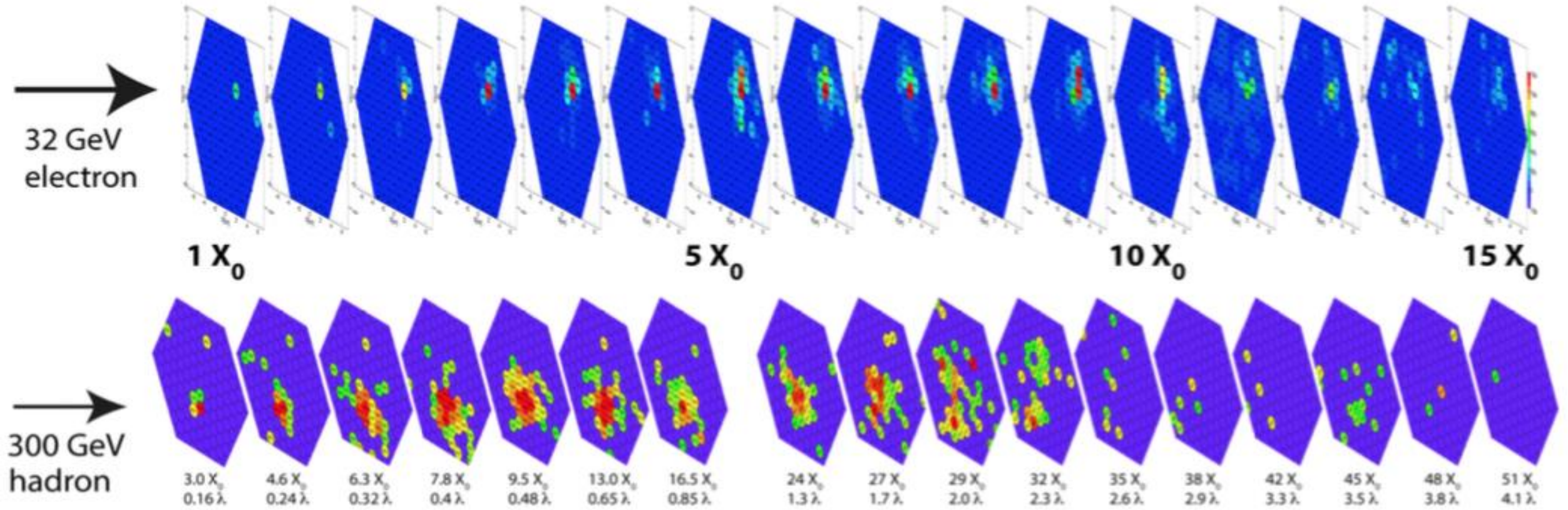
Next steps: System testing
Mechanical/thermal prototypes

Work started but much to do

- Cooling
- Mechanics and assembly
- Connectors

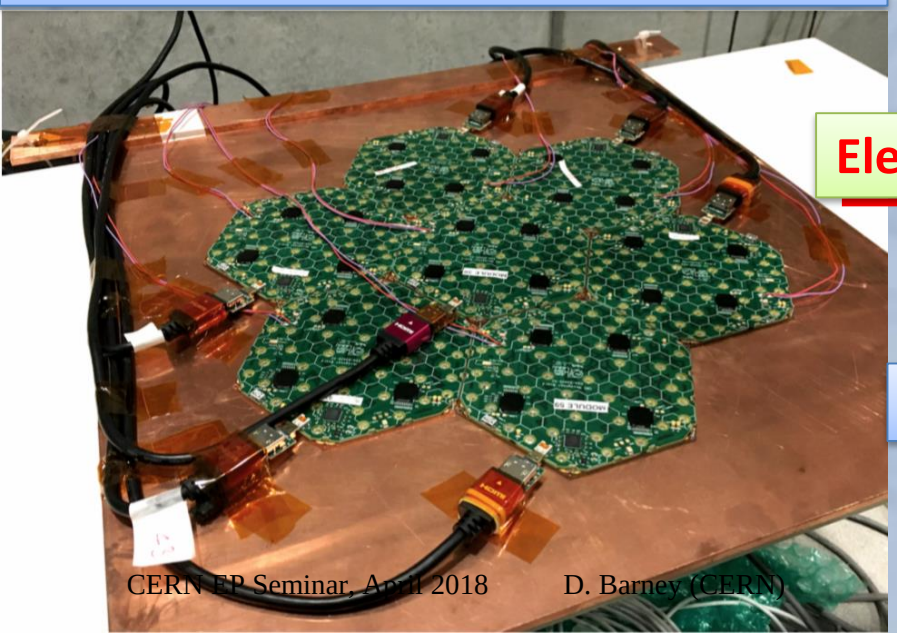
- Power distribution (up to 50W per motherboard)
- Bias distribution





Beam tests in 2016 & 2017 validated basic design;

Mips (for calibration) seen from muons and also single particles within hadronic showers



Si + Pb CE-E

Si + Pb front CE-H

CALICE AHCAL as rear CE-H

Electrons, pions, muons

Existing ASIC (Skiroc2) used in 2016; evolution (Skiroc2-CMS) used in 2017/18

Nearly 2 tonnes, 3m long

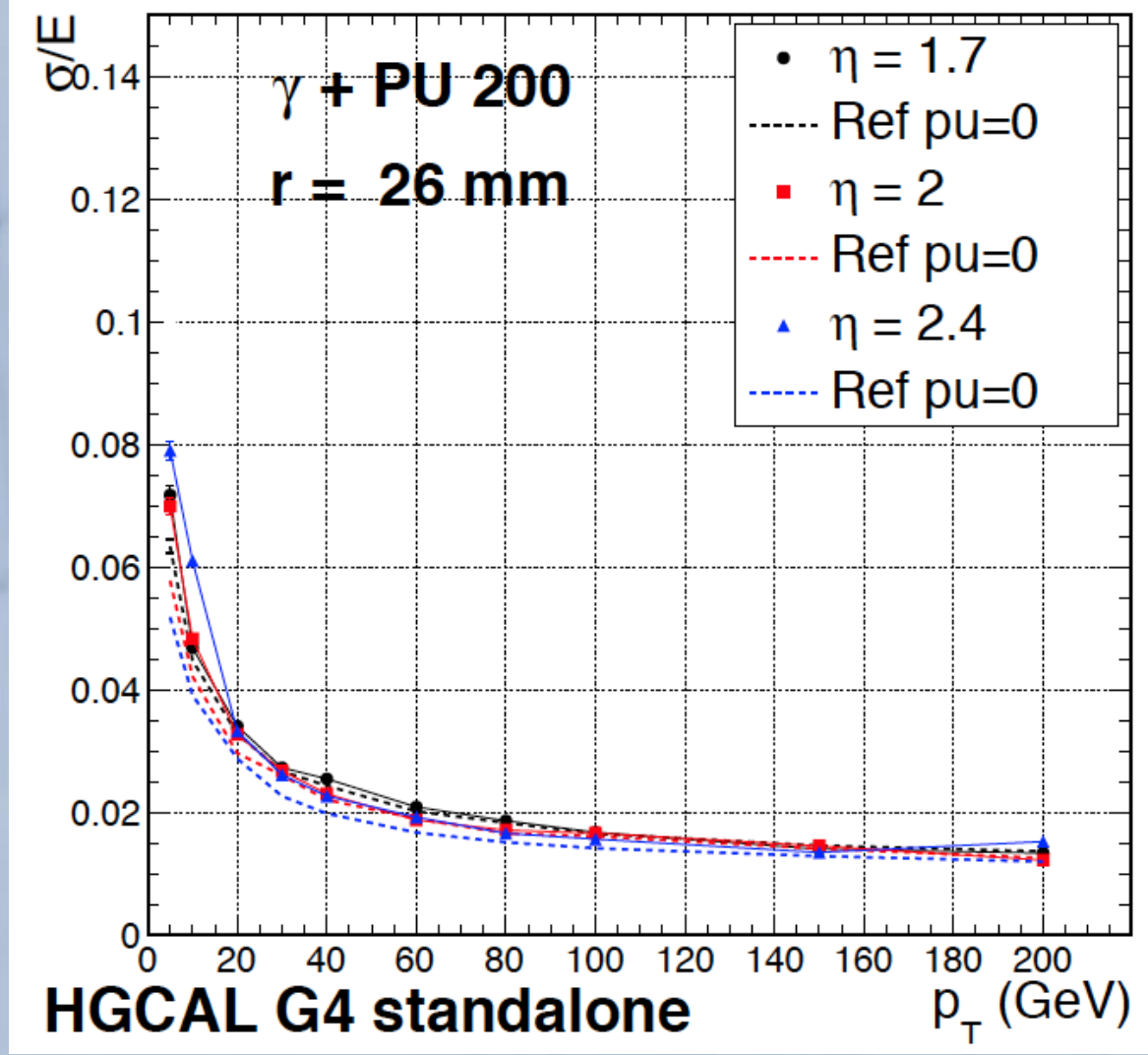
Quantities

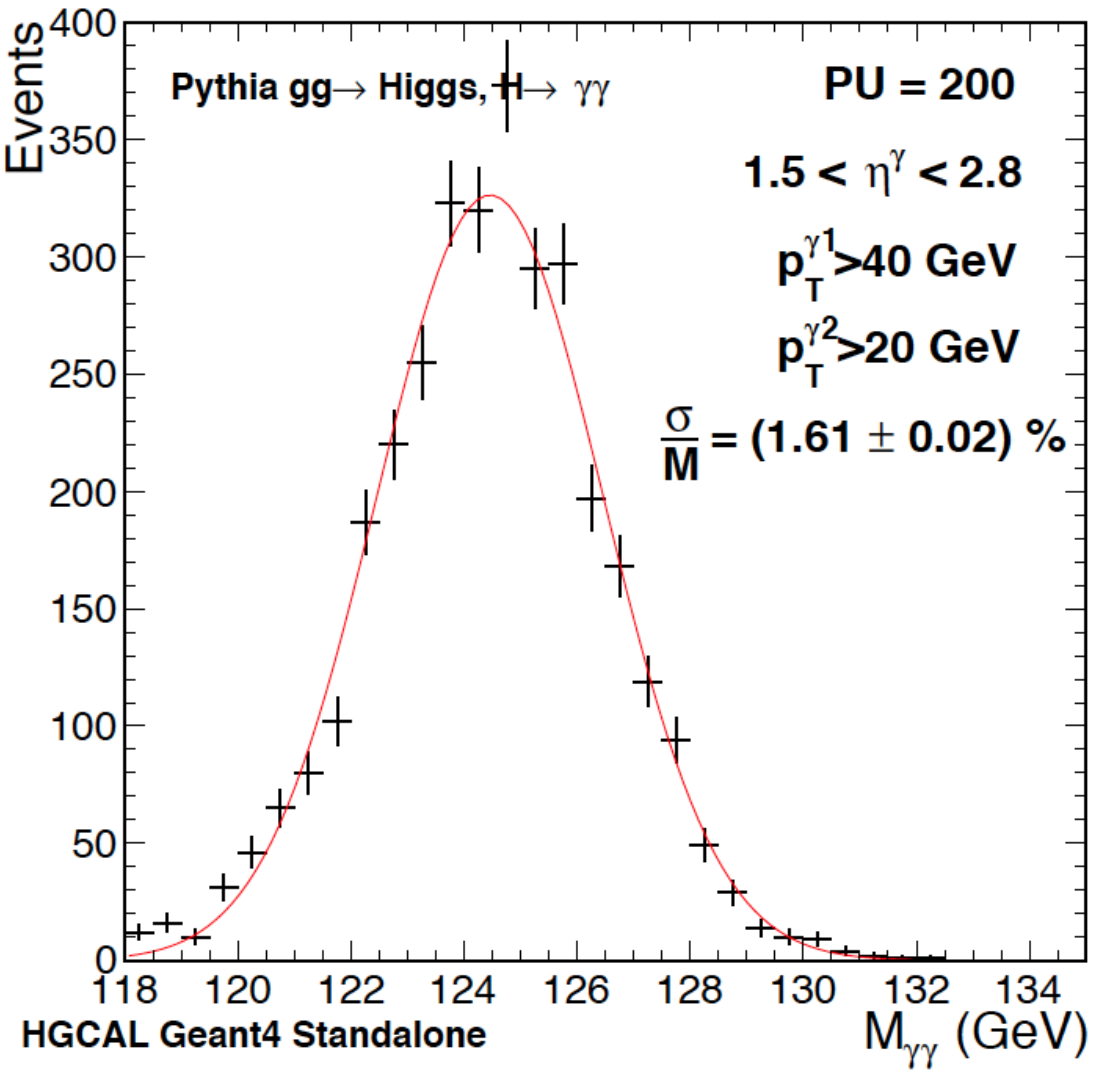
item	Quantity in HGC	
HGCROCs	100416	
Wafers (Si)	27336	1 per module
Tile Boards (scint)	3960	
Concentrators (both)	15888	2 per Motherboard
Motherboards	7944	
LpGBTs	7944	1 per Motherboard
Slow Control Adapter	7944	1 per Motherboard
Opto TX or RX	31776	1VTRX (3TX+1RX) per Motherboard
Optical fibres	23232	

Eyes on the Prize!

Single unconverted γ in CE-E reconstructed in r<2.6cm
→ **insensitive to pileup**

H-γγ, both γ in HGCAL
(γ do not convert in TK)
Pileup 200

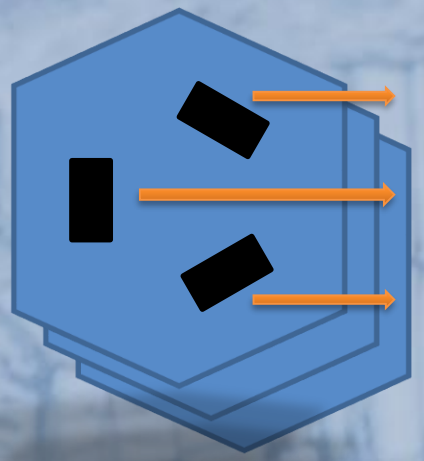




G4 simulation used to predict performance of HGCAL in presence of pileup: e/γ resolution

Thank you

Data Flow: Trigger



8bit (4+4 fp format) per TC
4 TC per 1.28gbps elink
12 links per module

36 elinks

ZS in eCon only
In MIP_T

Trig eCon

3x VL+ fibers

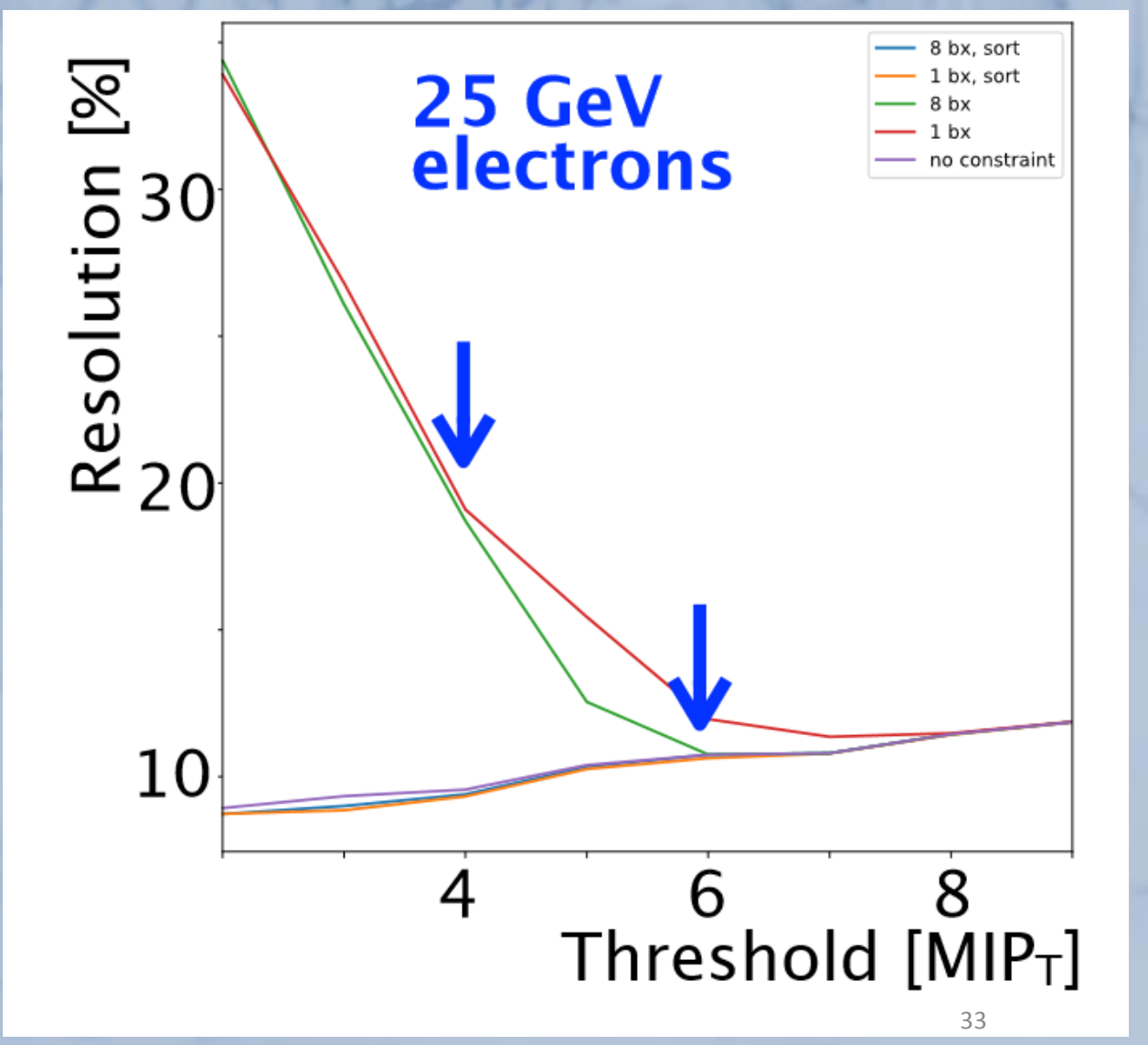
- Trigger Concentrator:
  - 36 input elink @ 1.28 (copy from lpGBT)
  - Sum
  - Threshold
  - Sort(?)
    - Max latency 8 xing

= output max ~25gbps to min ~3gbps

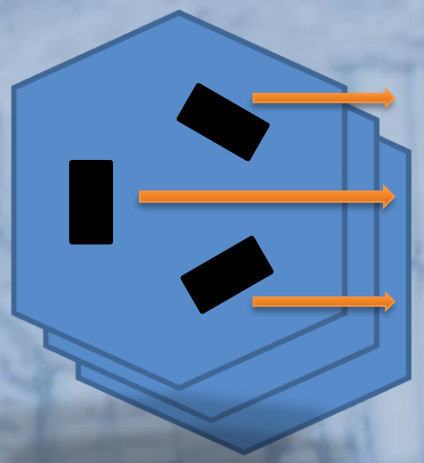
About 7500 fibers total in system

Trigger outputs are present only for ½ of the layers in CE-E

Must copy elink blocks / 10gbps blocks from lpGBT
And combine them!



Data Flow: DAQ



1.28gbps elink per HGCROC
3/6 elinks per module
ZS on HGCROC (threshold ~0.5MIP)

18 elinks

No ZS in eCon

DAQ eCon

7 elinks

lpGBT eCon

1x RX
1x TX fiber

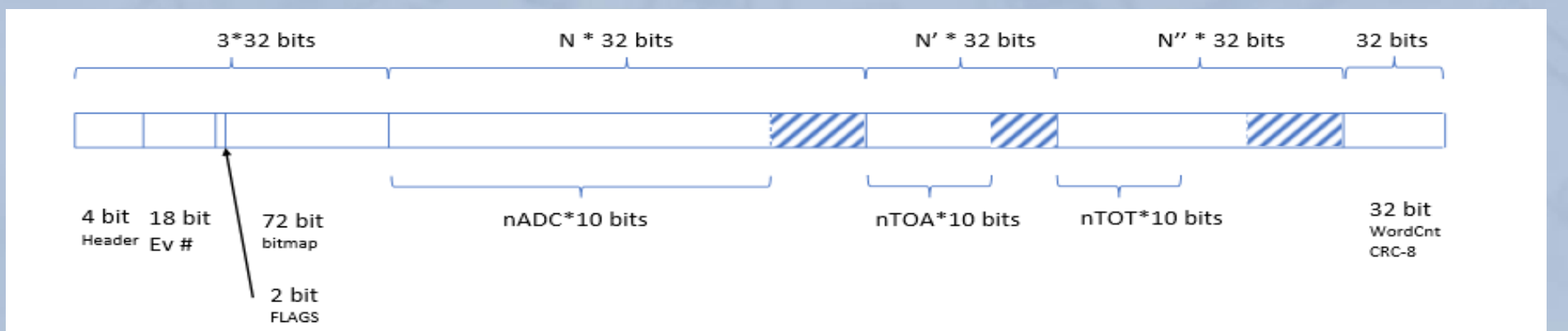
- DAQ Concentrator:
  - 18 input elink @ 1.28 (copy from lpGBT)
  - Buffering
  - No maximum latency

= output 7 x 1.28gbps max to lpGBT via elinks

About 8000 fibers total in system (every motherboard has lpGBT)

lpGBT also used to receive and distribute trigger/clock

Slow control via I2C and GBT-SCA



Imperial College London

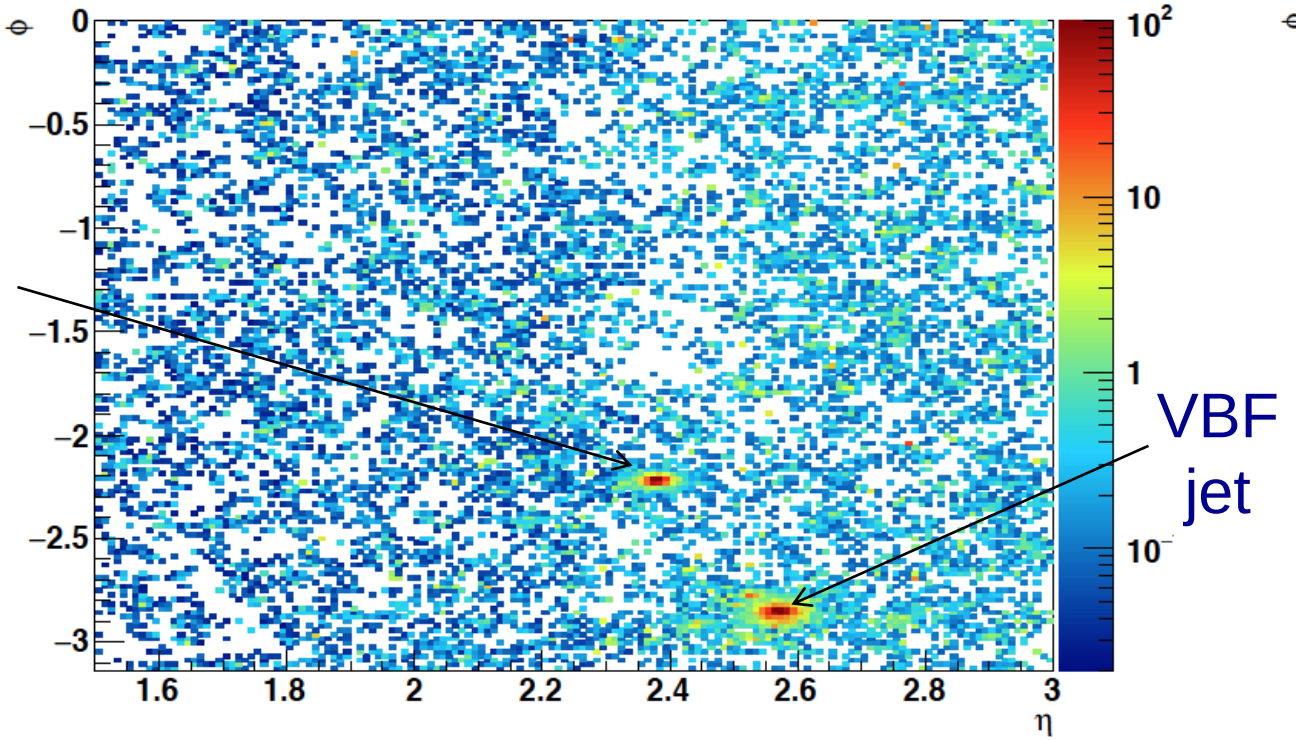
What is the Expected Performance?
Pileup Mitigation using Timing Resolution

Arises naturally from the choice of CE parameters and electronics

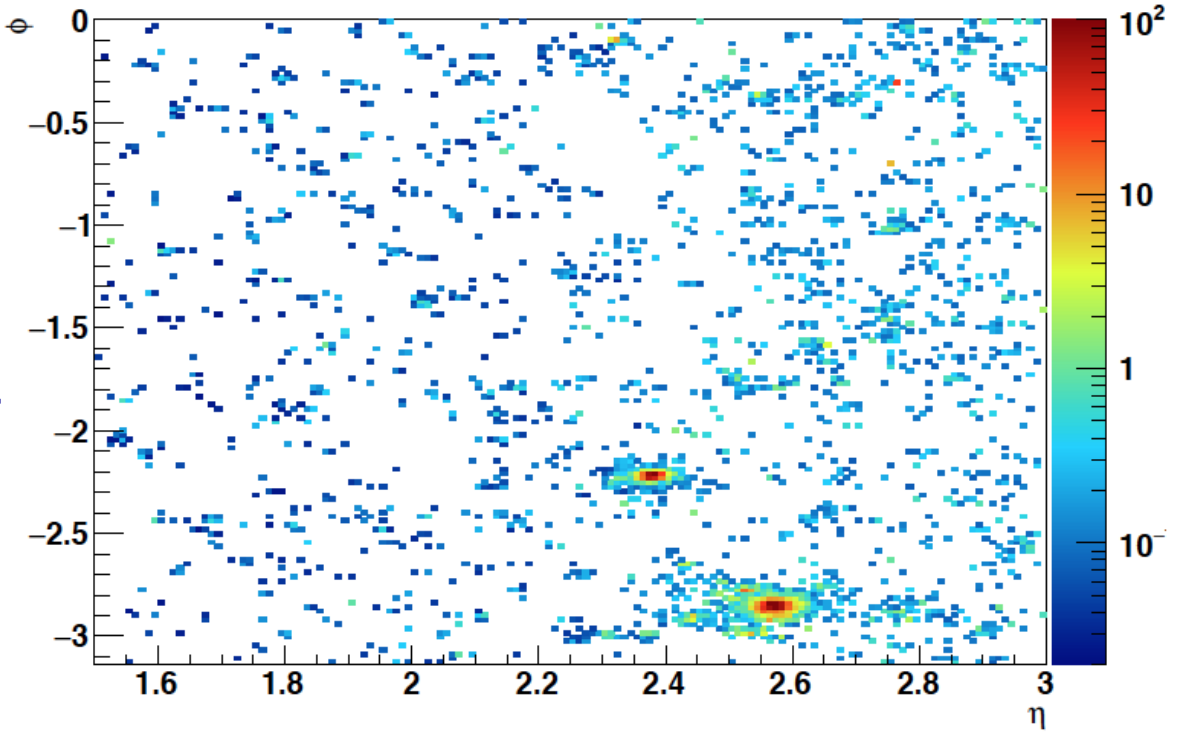
Figure of Merit: pileup mitigation (illustrative)

VBF ($H\rightarrow\gamma\gamma$) event with one photon and one VBF jet in the same quadrant,

No timing cut

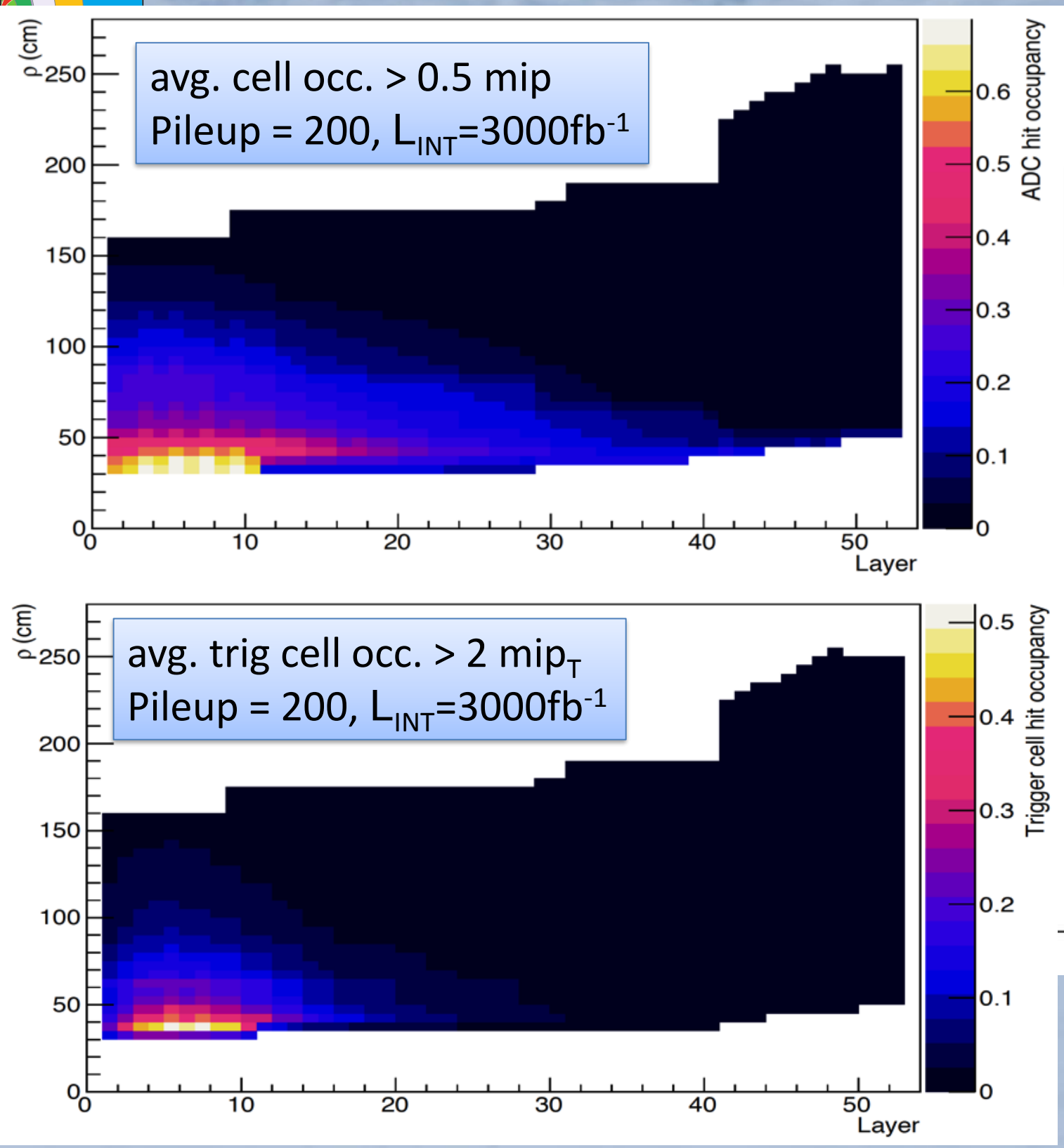


Cut $\Delta t < 90ps$ (3σ at 30ps)

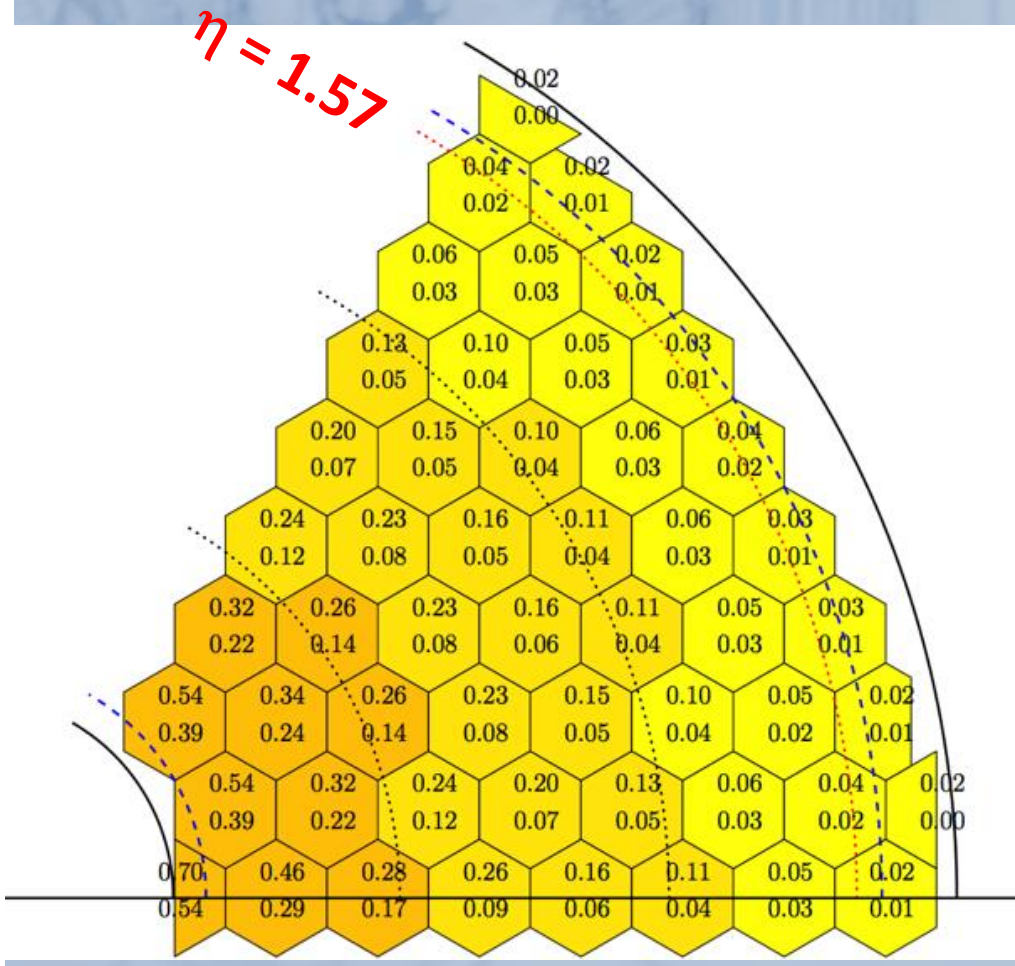


Plots show cells with Q > 12fC (threshold for timing measurement) projected to the front face of the endcap calorimeter.

Occupancy of cells reaches ~70% in a small high-η region, but is <20% for most of HGCAL



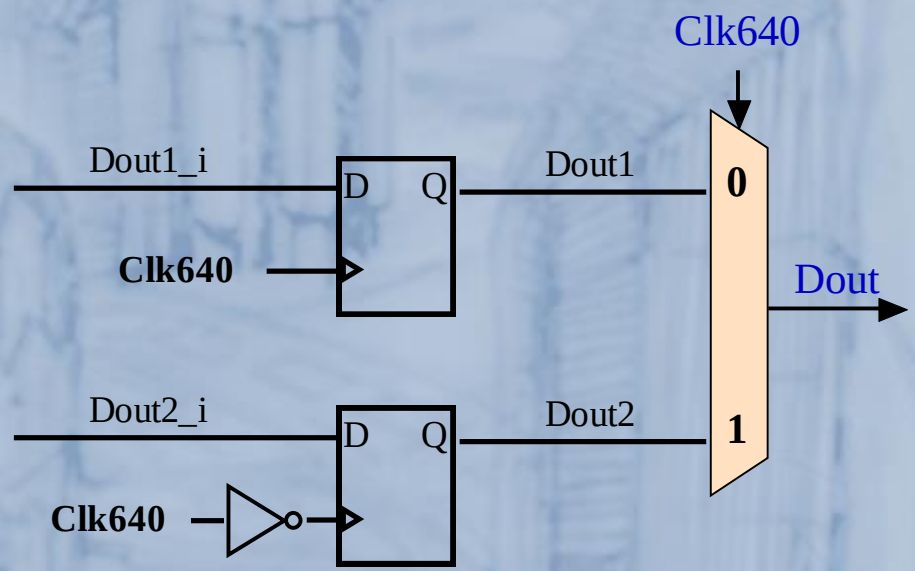
Top num.: avg. cell occ. > 0.5 mip
Bottom: avg. trig. cell occ. > 2 mip$_T$



Colours = different thicknesses of silicon sensors

Serializer and Elink for trigger path

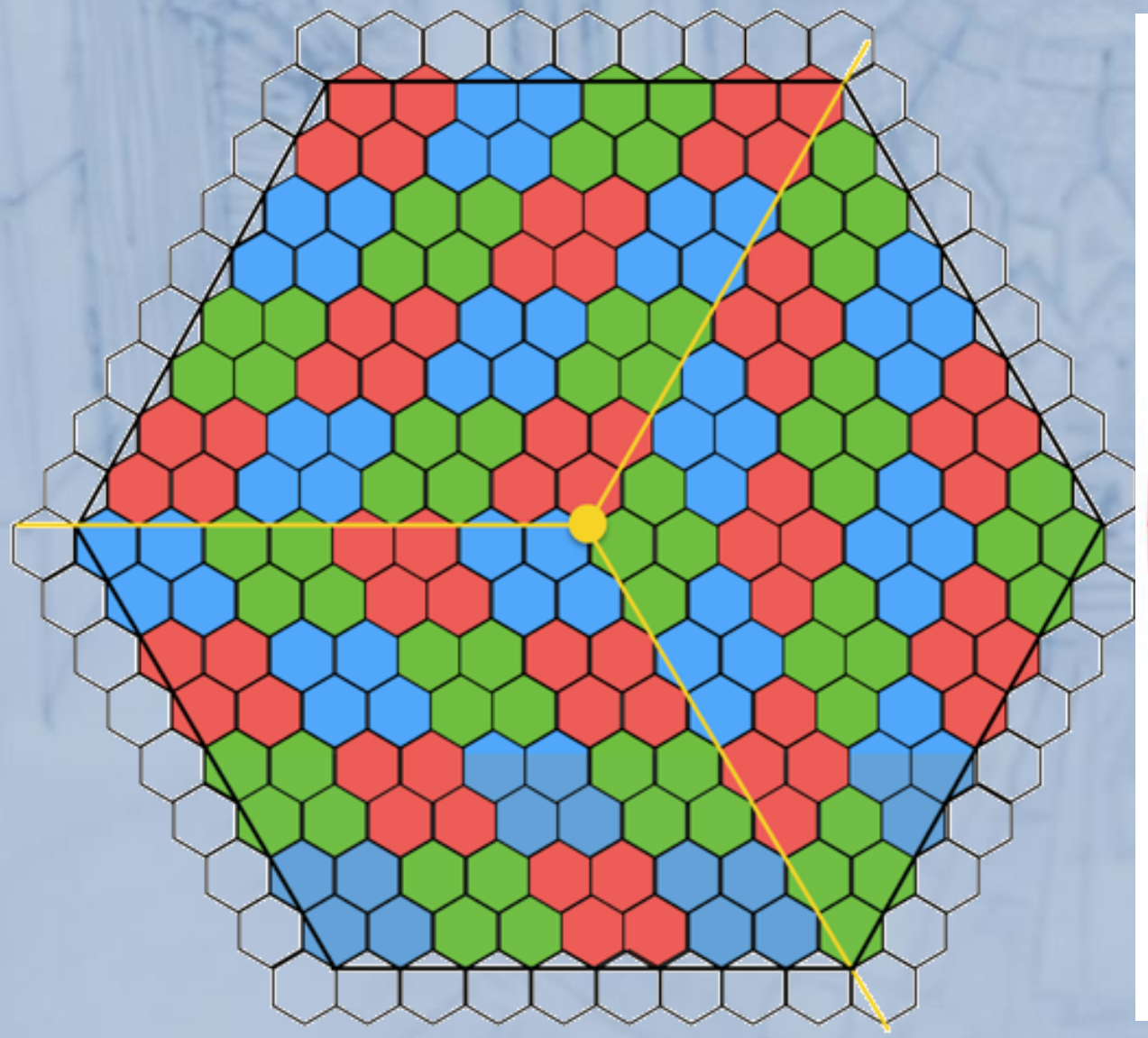
- The chip integrates 2 elink transmitter to handle the 64 bits from the trigger path
  - 4 channels are encoded into 8 bits (with 4+4 encoding)
  - 2 variants (fully digital or mixed ➔ way the last mux is done)
  - Possibility to readout a known frame (set by SC)
  - Default is 1,28 Gb/s (640 Mb/s possible)

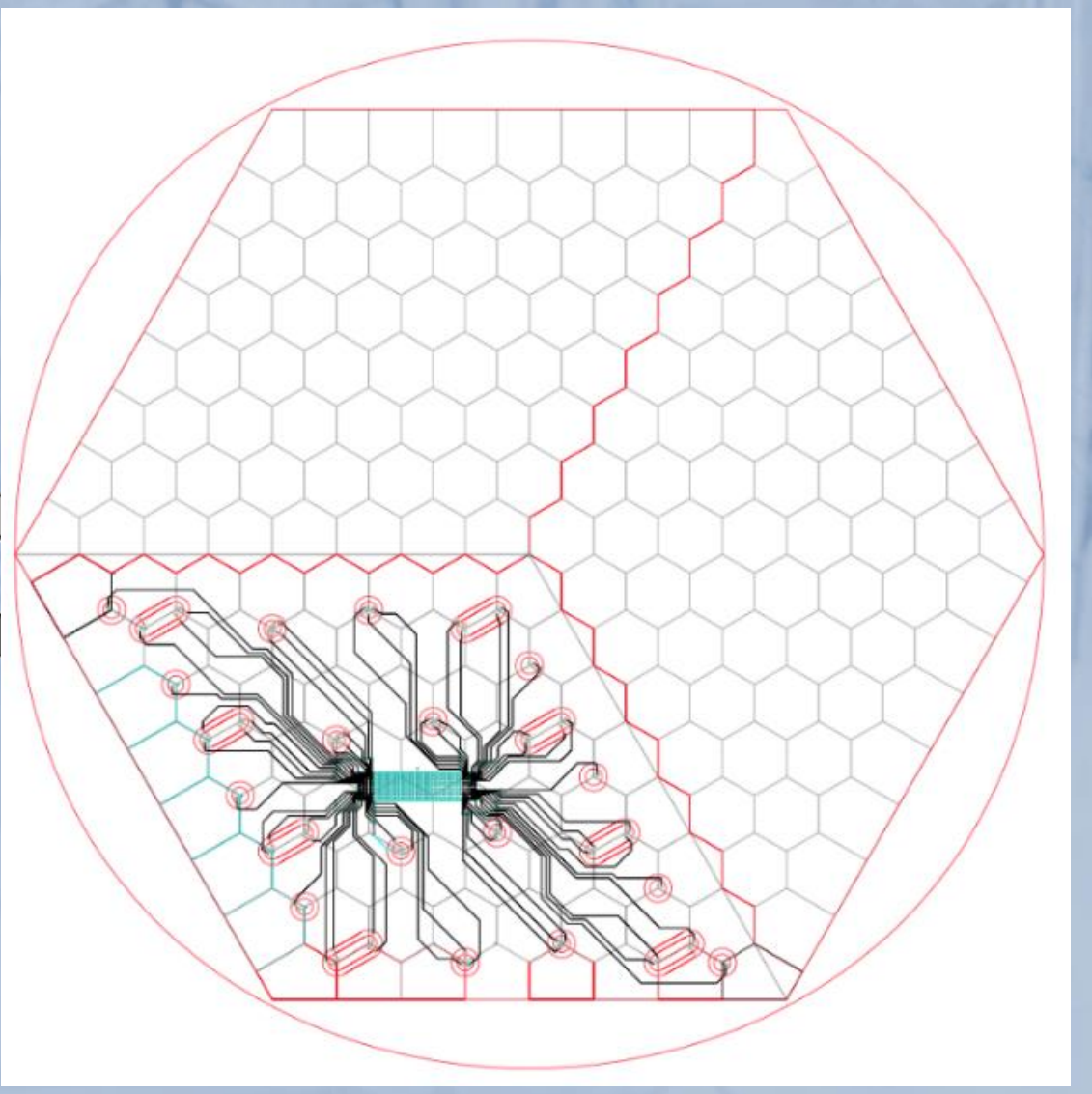


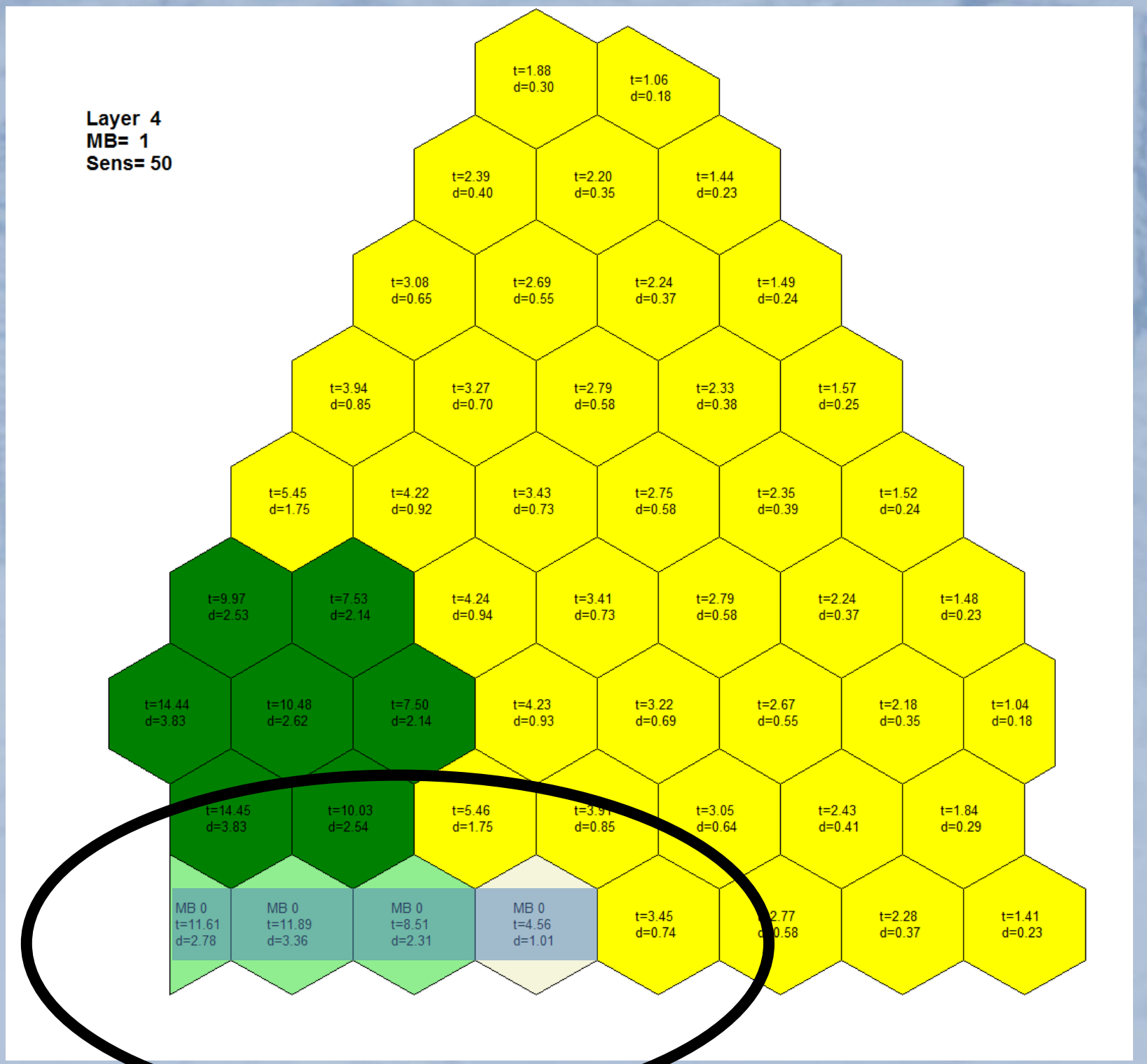
- Main specifications:
  - Data rate 1,28 Gb/s (internally 640M DDR)
  - Compatible with LpGBT protocol
  - Programmable Pre-emphasis (based on Paulo Moreira scheme)
  - Synchronization pattern on request (in place of trigger data)

Specification description	Value
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

Hexaboard



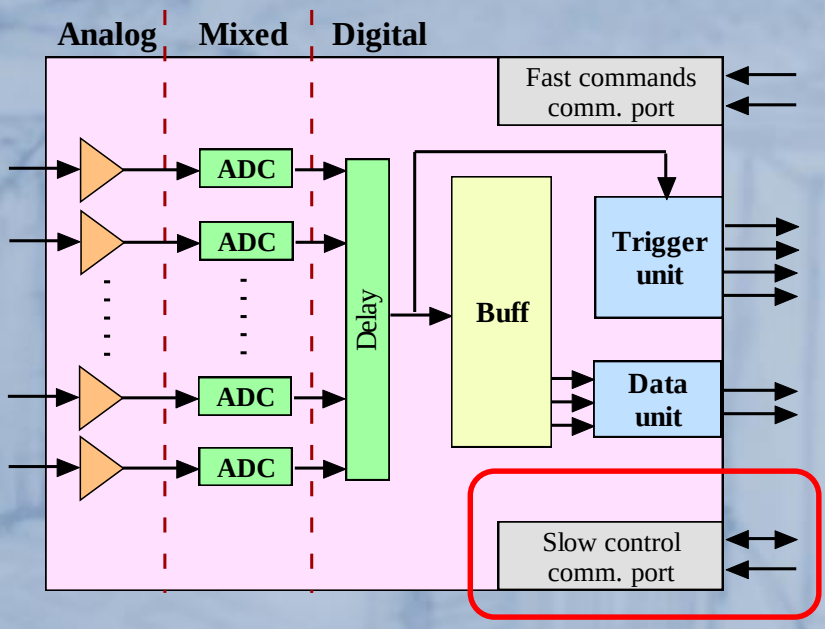


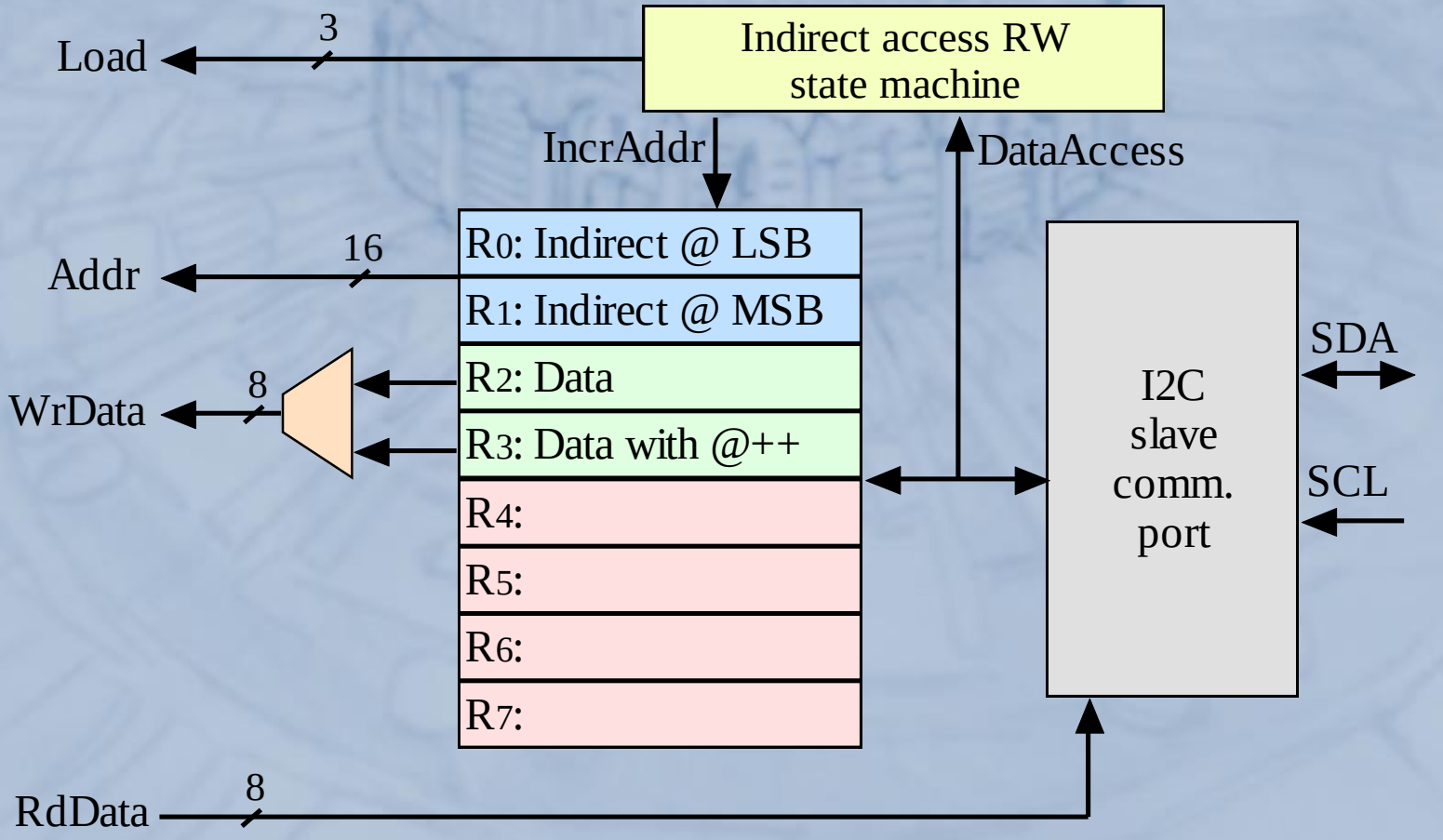

Layer 4
MB= 1
Sens= 50
t=1.88
d=0.30
t=1.06
d=0.18
t=2.39
d=0.40
t=2.20
d=0.35
t=1.44
d=0.23
t=3.08
d=0.65
t=2.69
d=0.55
t=2.24
d=0.37
t=1.49
d=0.24
t=3.94
d=0.85
t=3.27
d=0.70
t=2.79
d=0.58
t=2.33
d=0.38
t=1.57
d=0.25
t=5.45
d=1.75
t=4.22
d=0.92
t=3.43
d=0.73
t=2.75
d=0.58
t=2.35
d=0.39
t=1.52
d=0.24
t=9.97
d=2.53
t=7.53
d=2.14
t=4.24
d=0.94
t=3.41
d=0.73
t=2.79
d=0.58
t=2.24
d=0.37
t=1.48
d=0.23
t=14.44
d=3.83
t=10.48
d=2.62
t=7.50
d=2.14
t=4.23
d=0.93
t=3.22
d=0.69
t=2.67
d=0.55
t=2.18
d=0.35
t=1.04
d=0.18
t=14.45
d=3.83
t=10.03
d=2.54
t=5.46
d=1.75
t=3.05
d=0.64
t=2.43
d=0.41
t=1.84
d=0.29
MB 0
t=11.61
d=2.78
MB 0
t=11.89
d=3.36
MB 0
t=8.51
d=2.31
MB 0
t=4.56
d=1.01
t=3.45
d=0.74
t=2.28
d=0.37
t=1.41
d=0.23

I2C: implementation

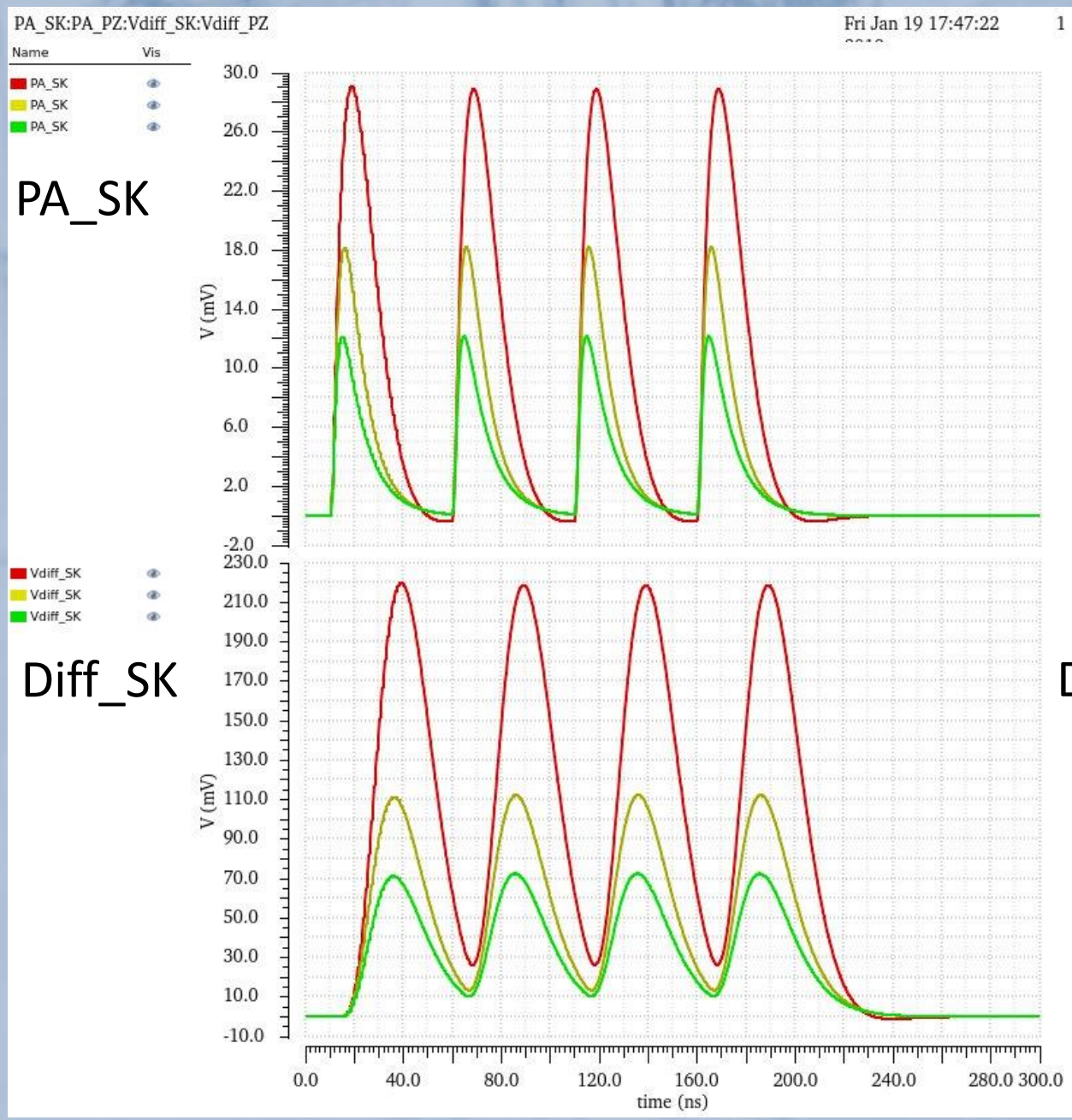
- List of direct access I2C registers:

I2C @	Register	Comments
0	ASIC parameter address (LSB)	Indirect @
1	ASIC parameter address (MSB)	Indirect @
2	Data	
3	Data with auto @++	Increment indirect @ after each access
4-7	Tbd (TMR status, parity…)	



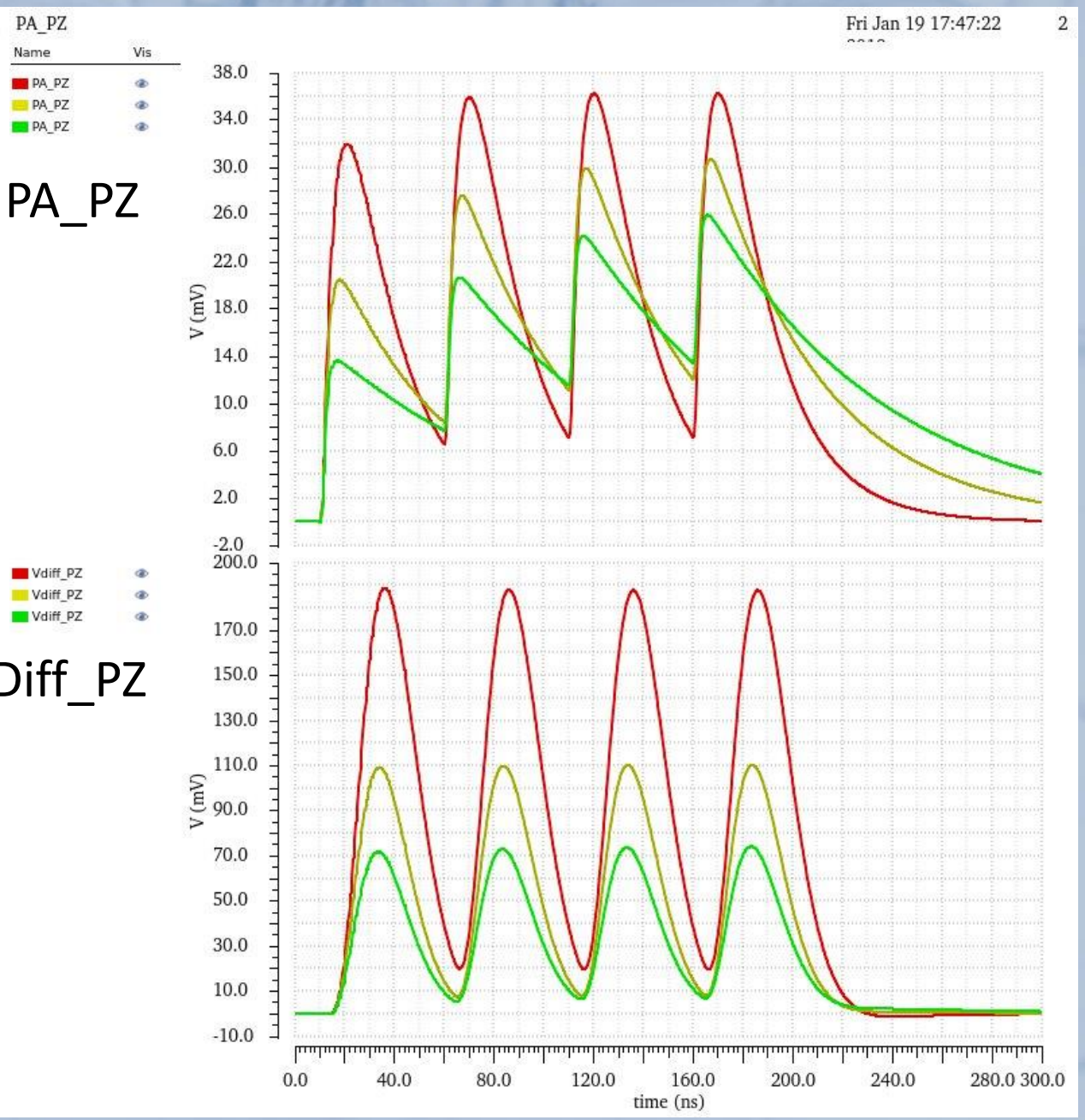


OOT pileup: 50% occupancy (max or typ ?)



PA_SK

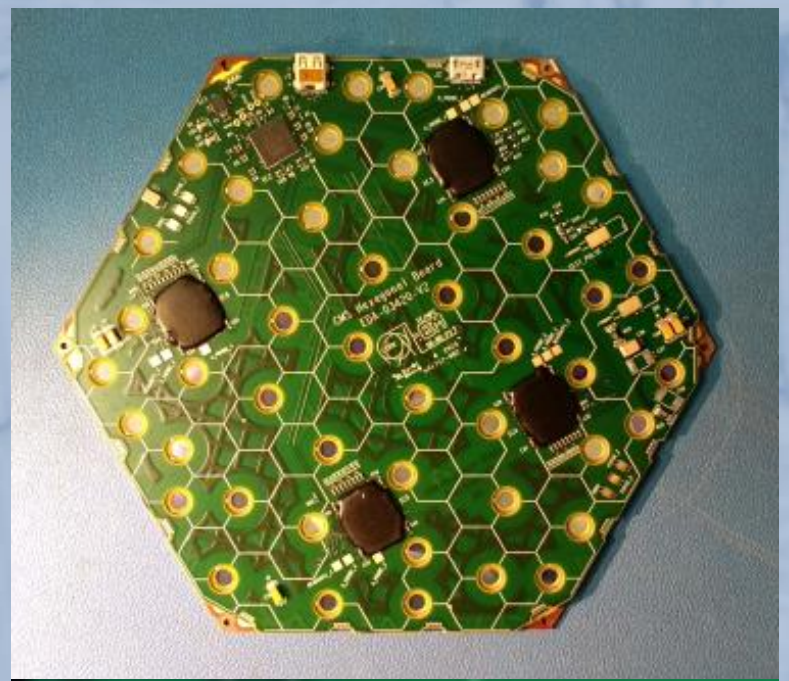
Diff_SK

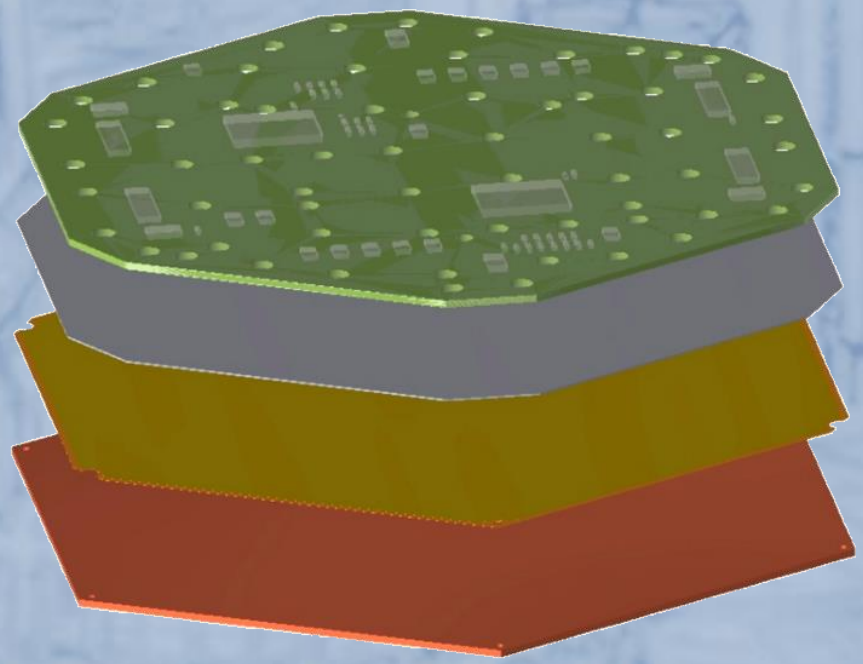


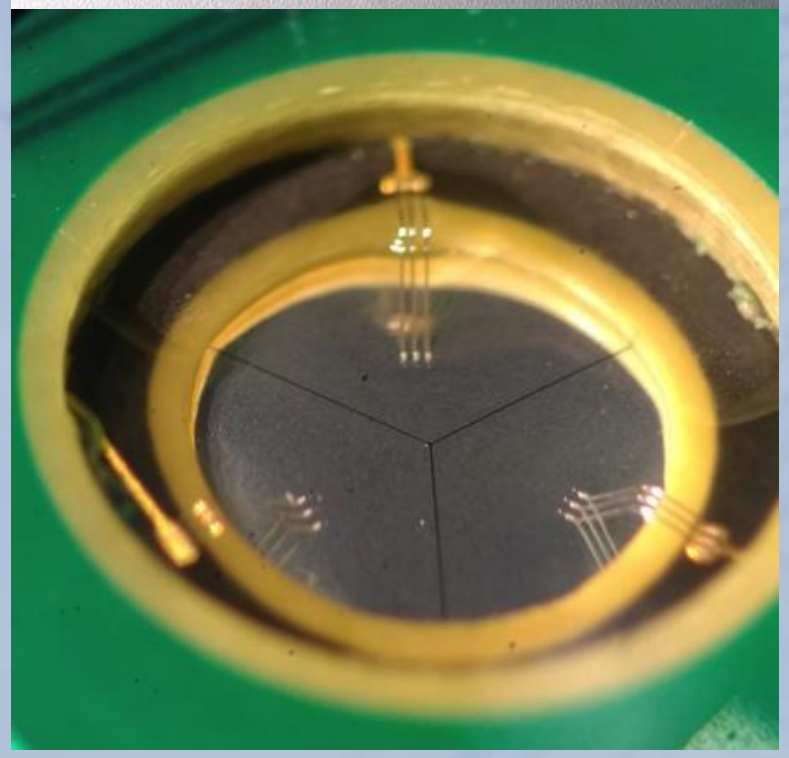
PA_PZ

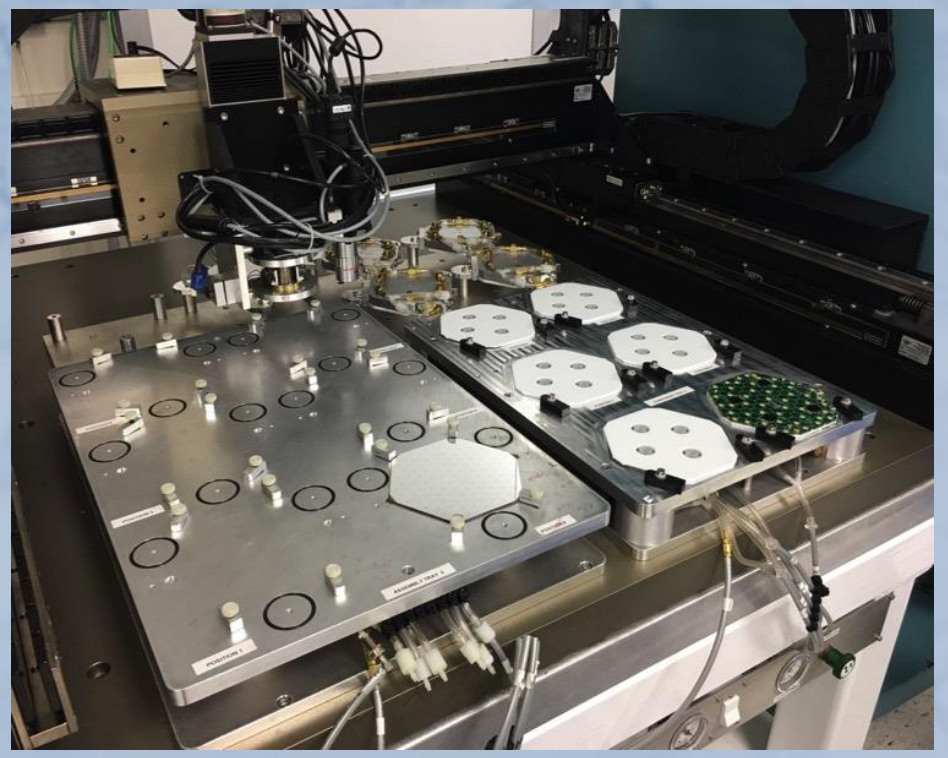
Diff_PZ

Module construction



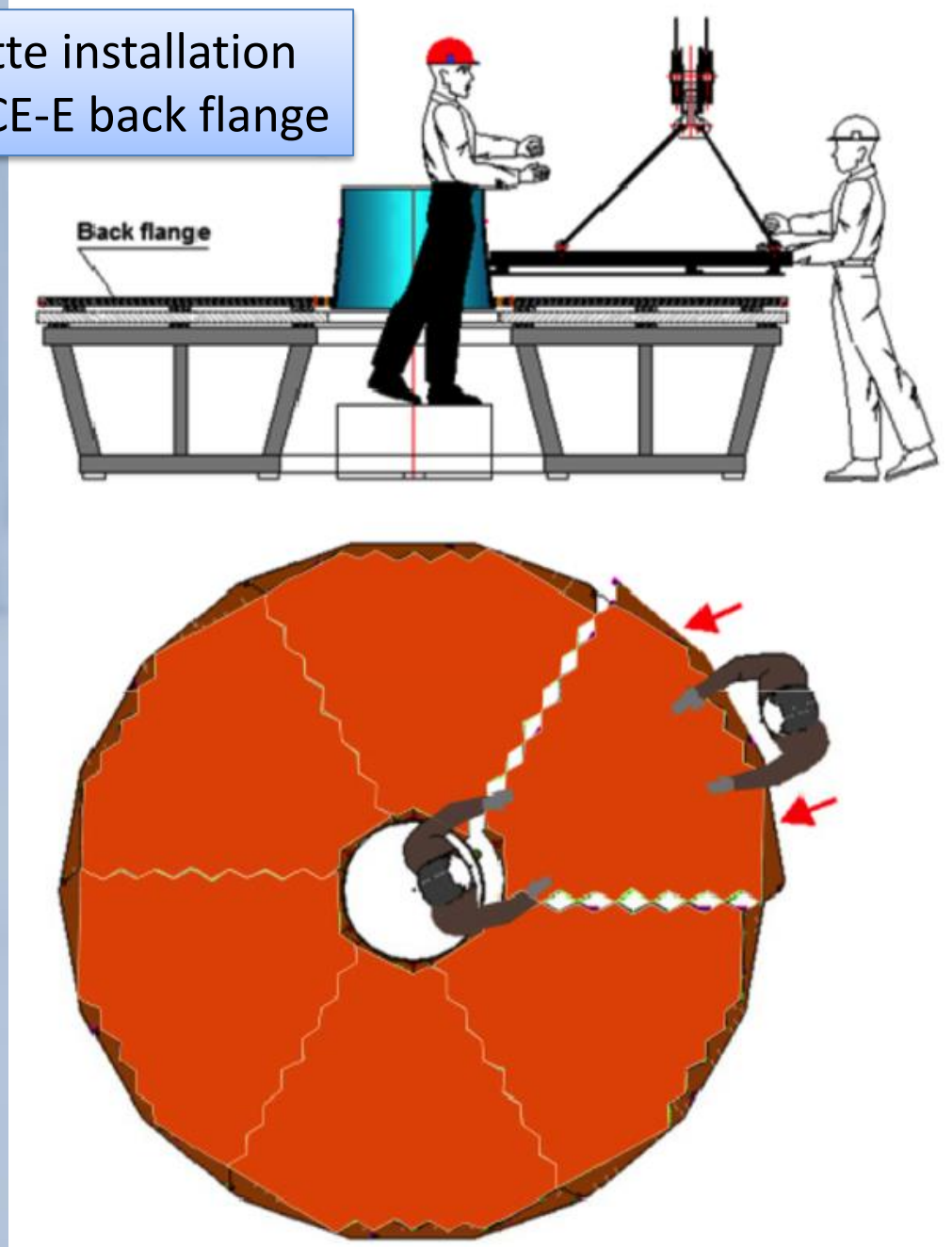


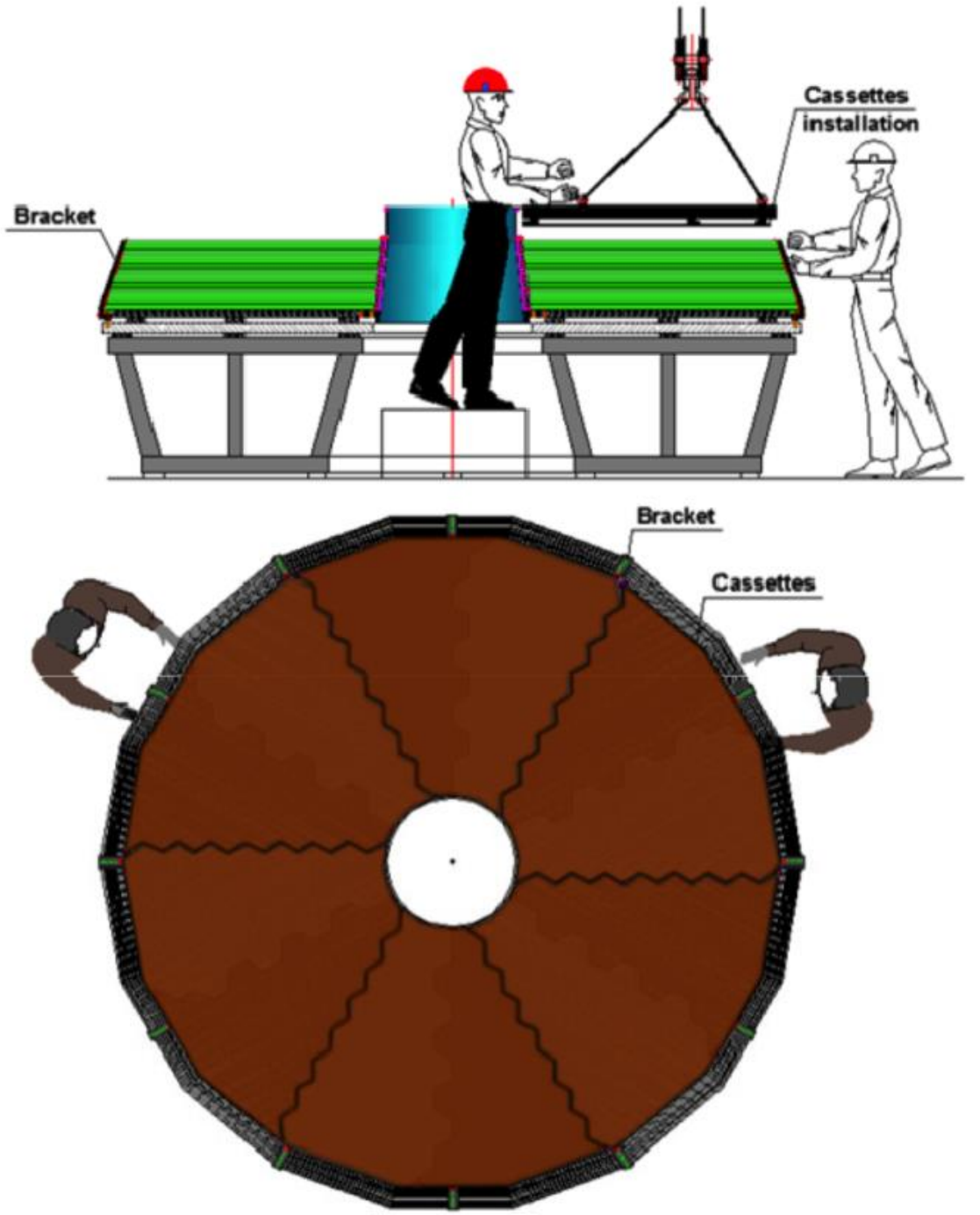




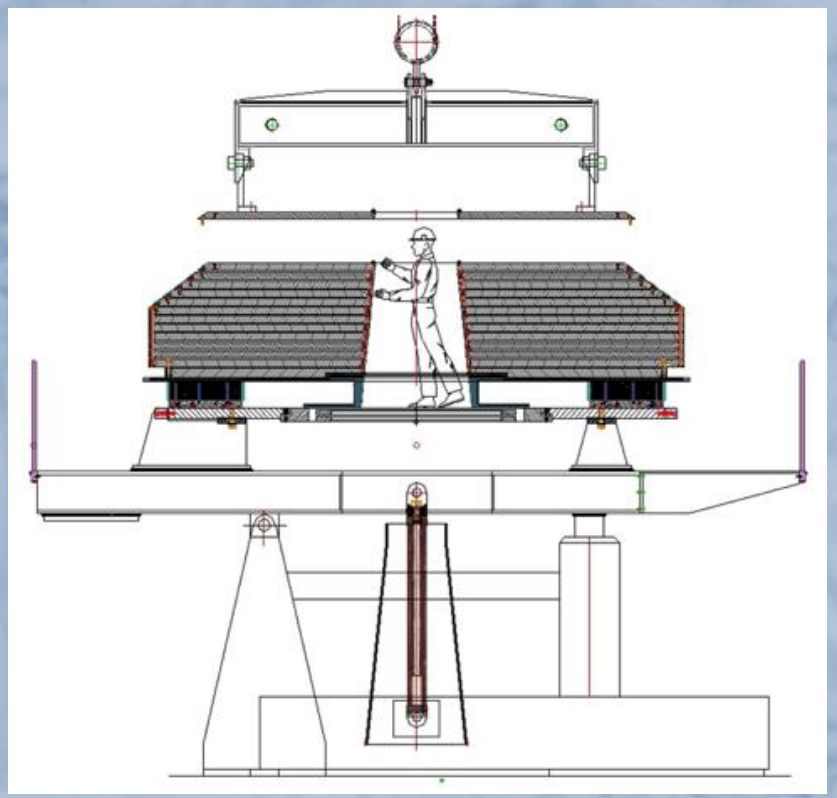
Assembling CE-E: self-supporting cassettes

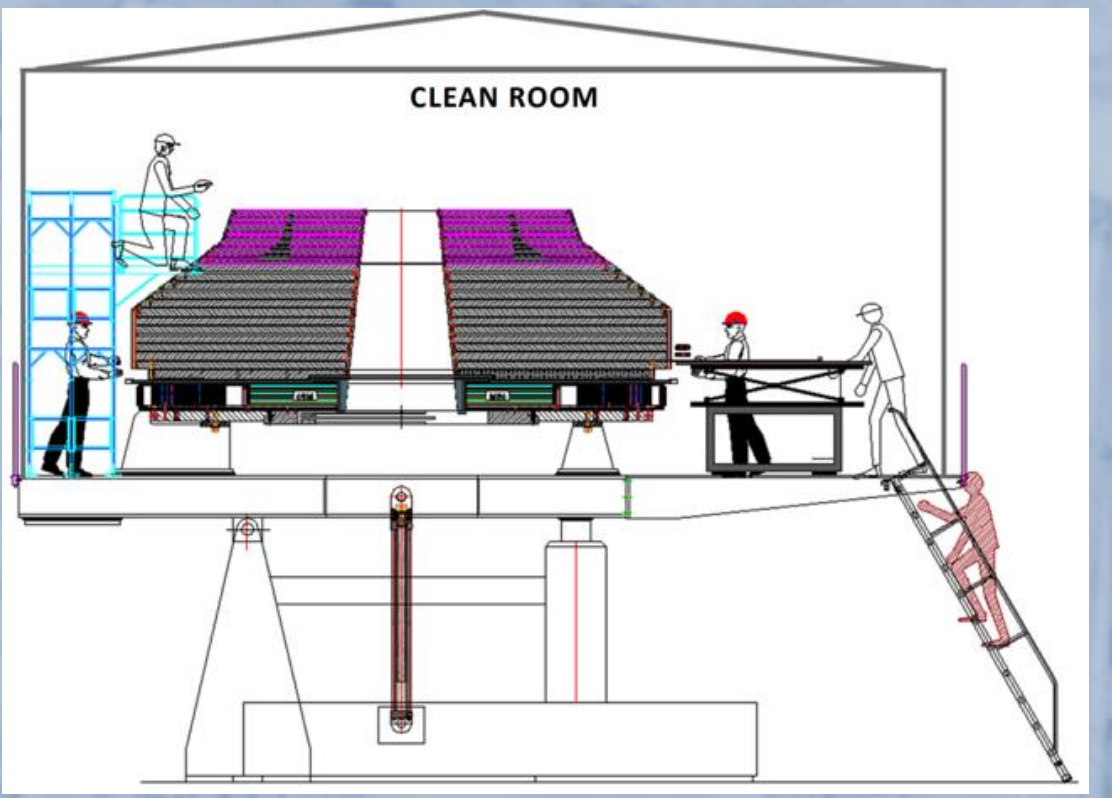
Cassette installation onto CE-E back flange

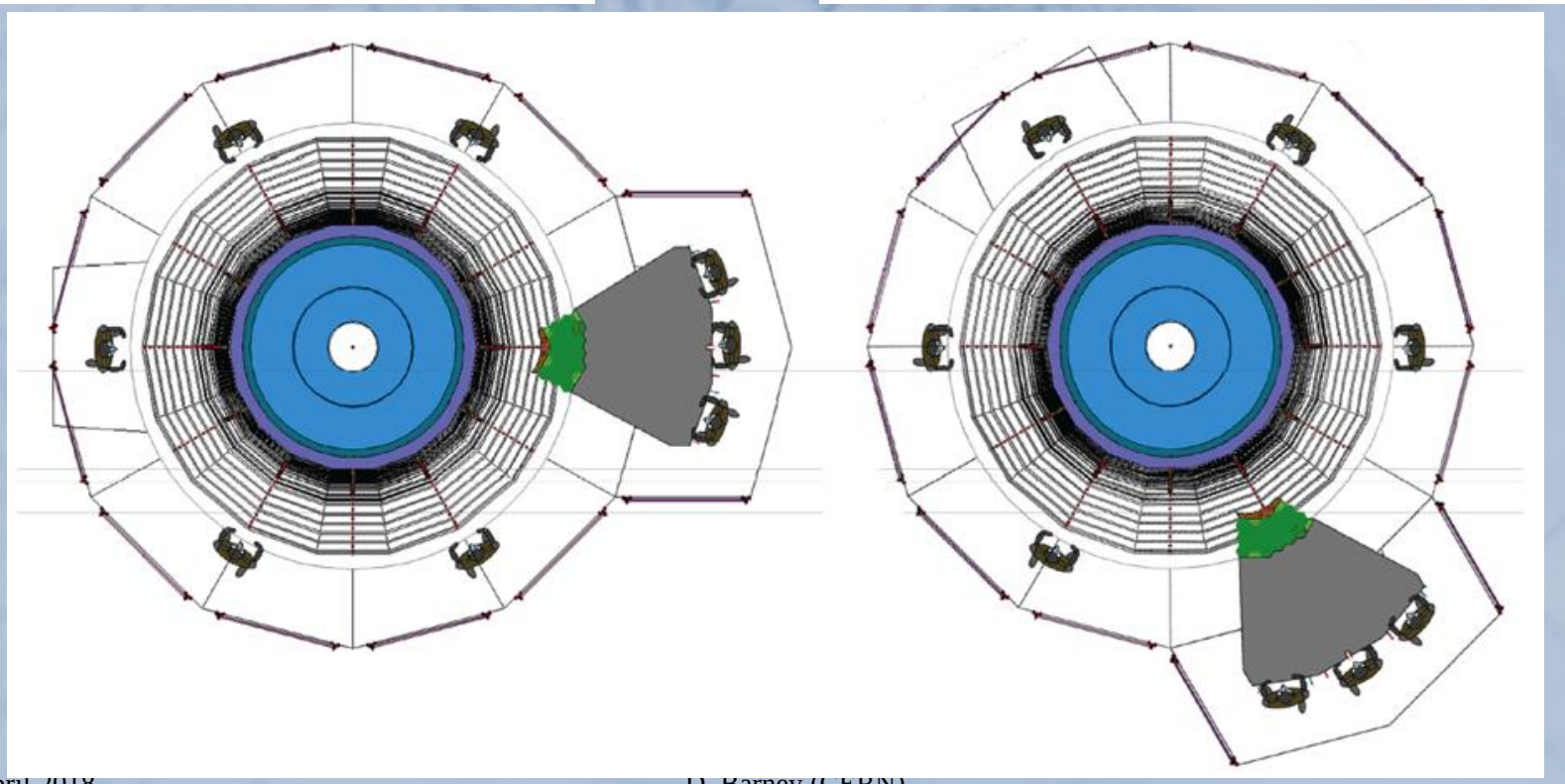




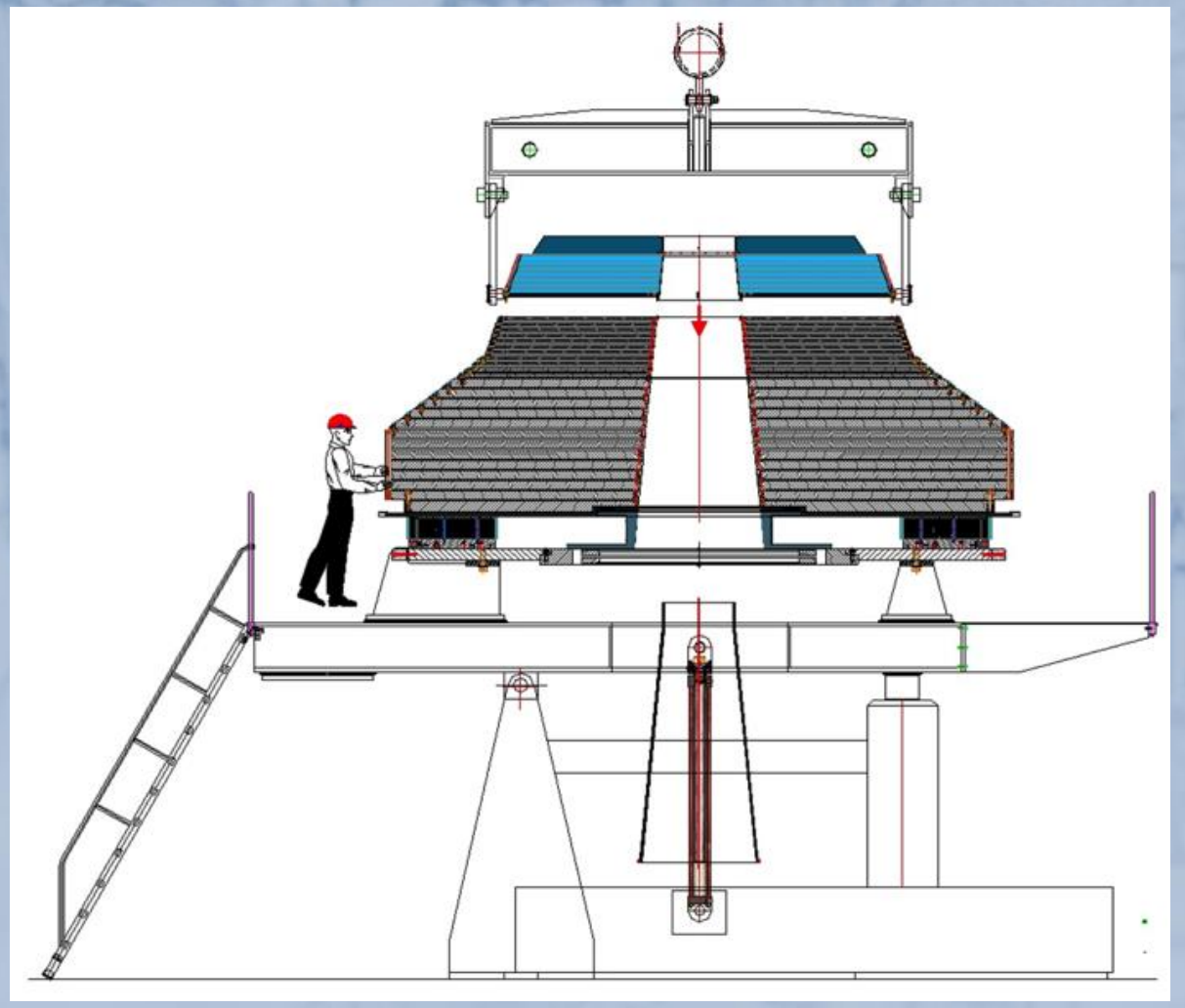
CE-H is assembled in two steps: absorber material, followed by insertion of cassettes

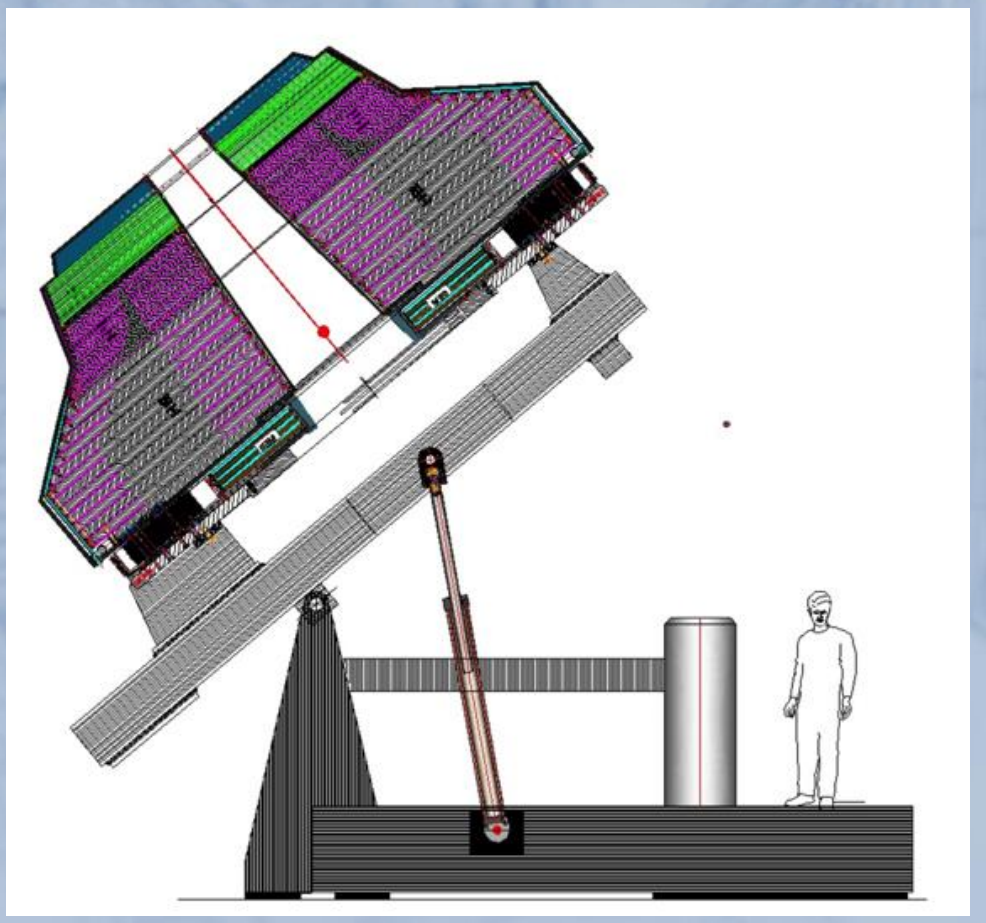






Final assembly steps: attach CE-E to CE-H, then rotate whole CE to vertical for lowering

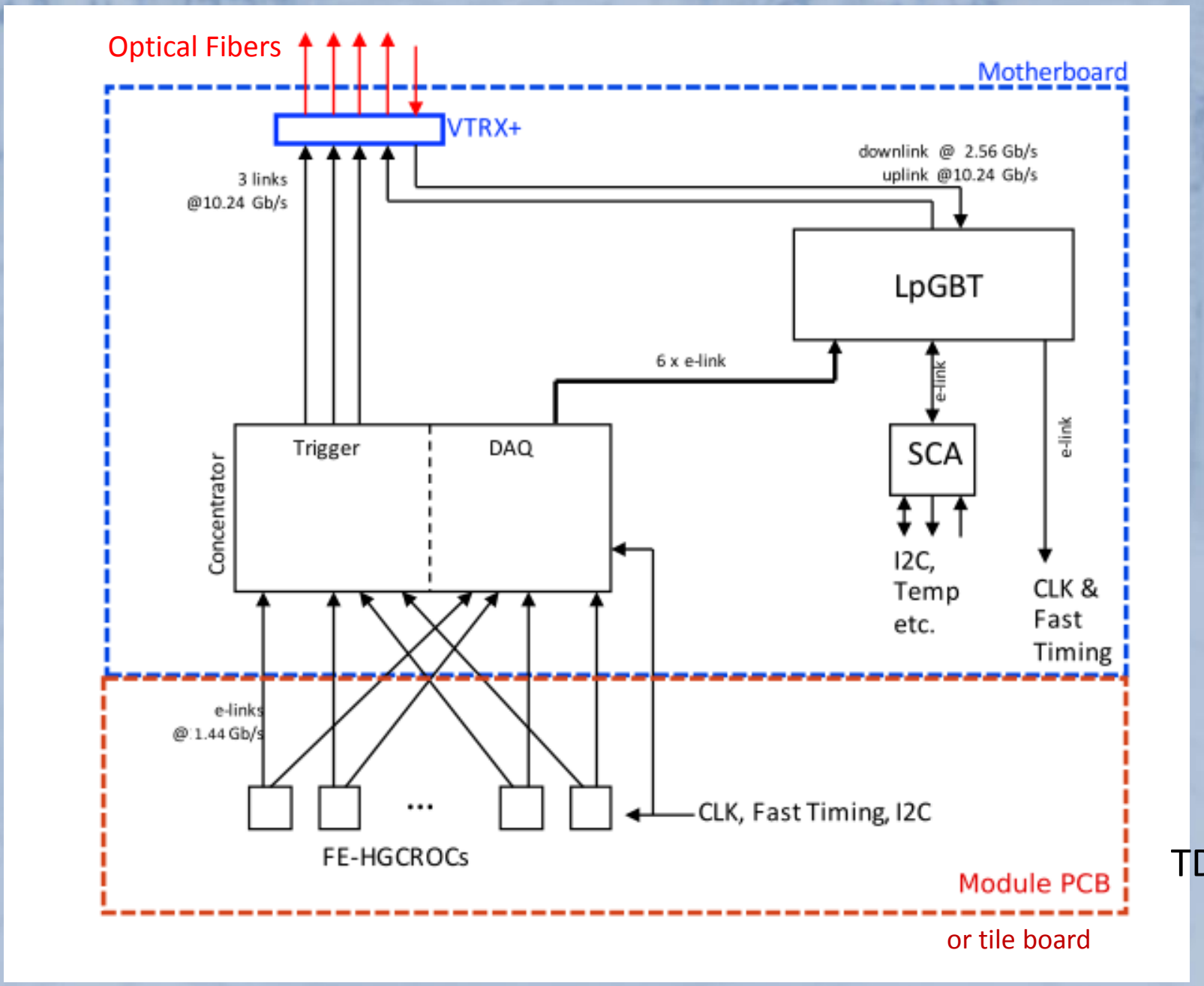




Readout Architecture

Concentration
Serialization
Optical transmission

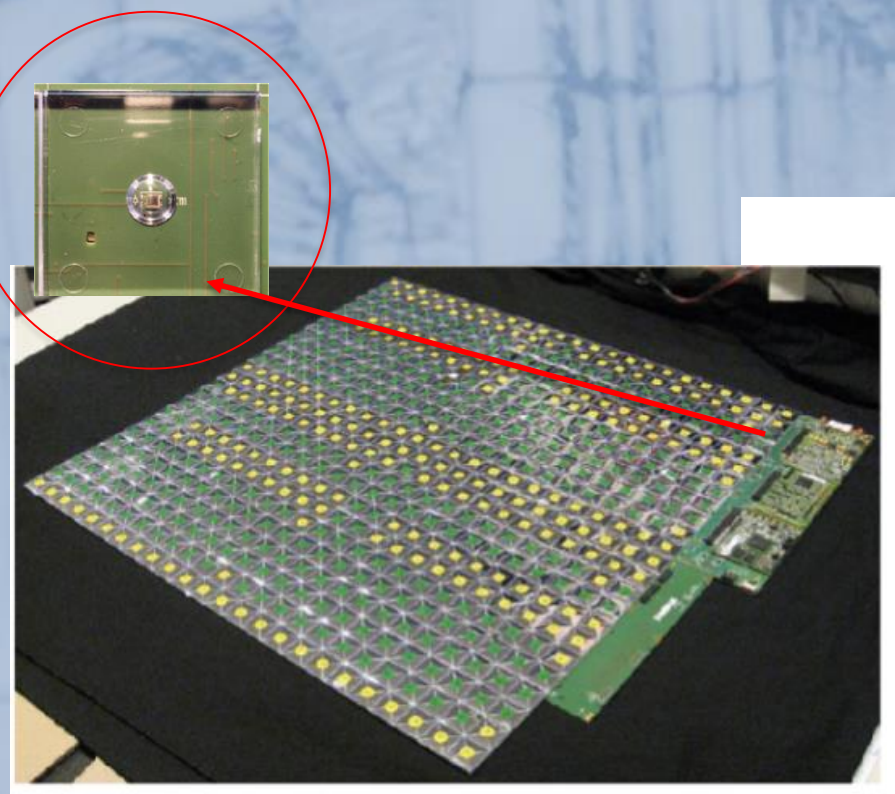
Q and T digitization
4 (9) cells Trigger Cells



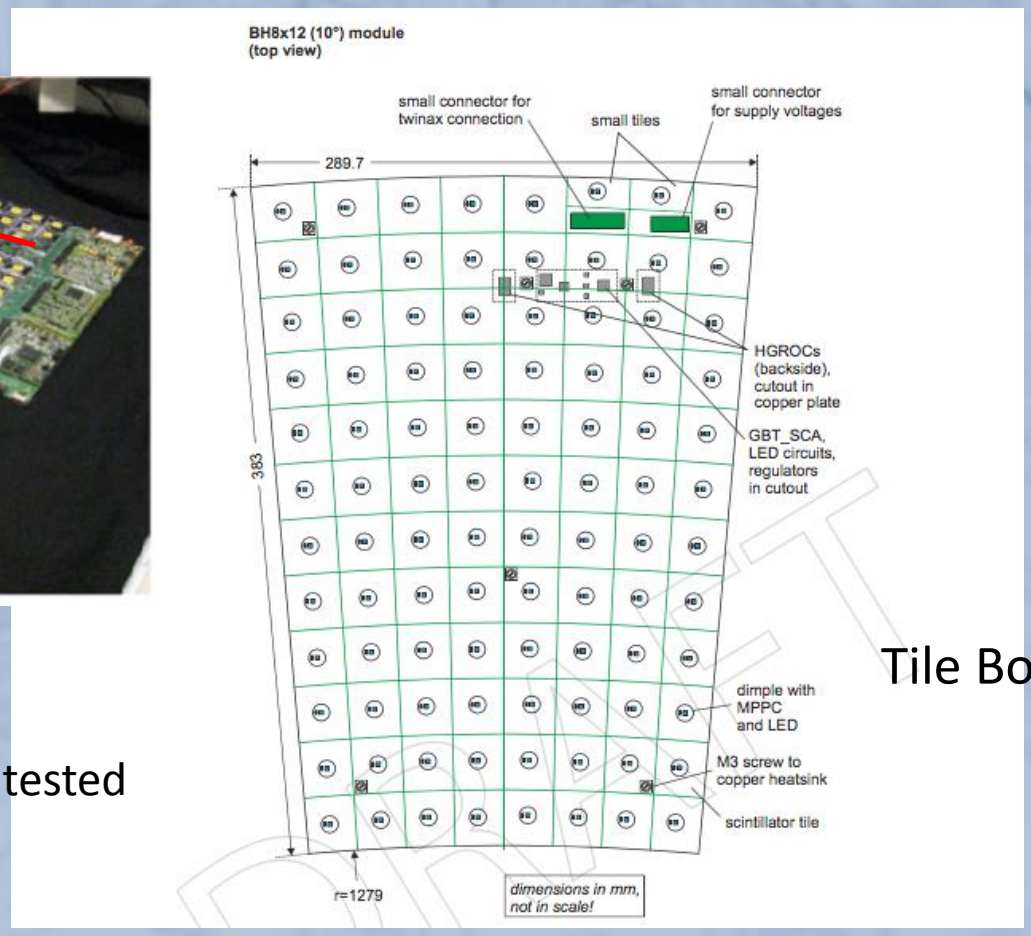
Fast and slow
Clock &
control

TDR Fig 8.1

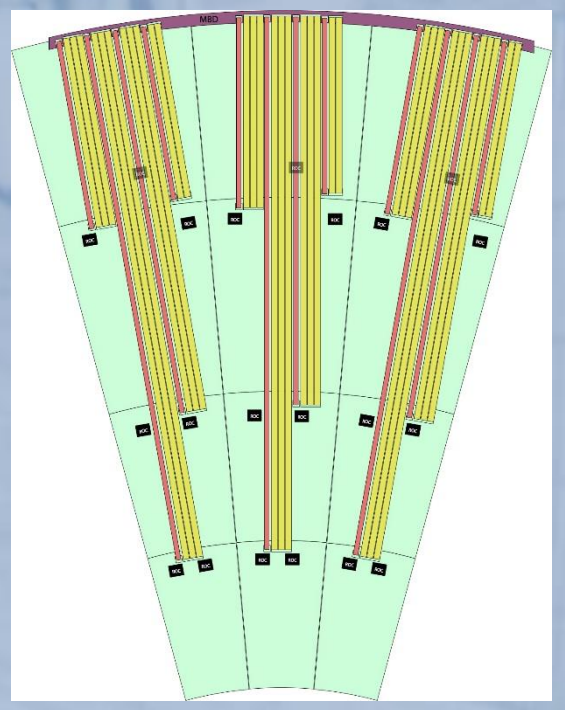
Physical implementation: Scintillator



CALICE HCAL Base Unit
11 full layers assembled, to be tested at SPS May-June. (DESY)



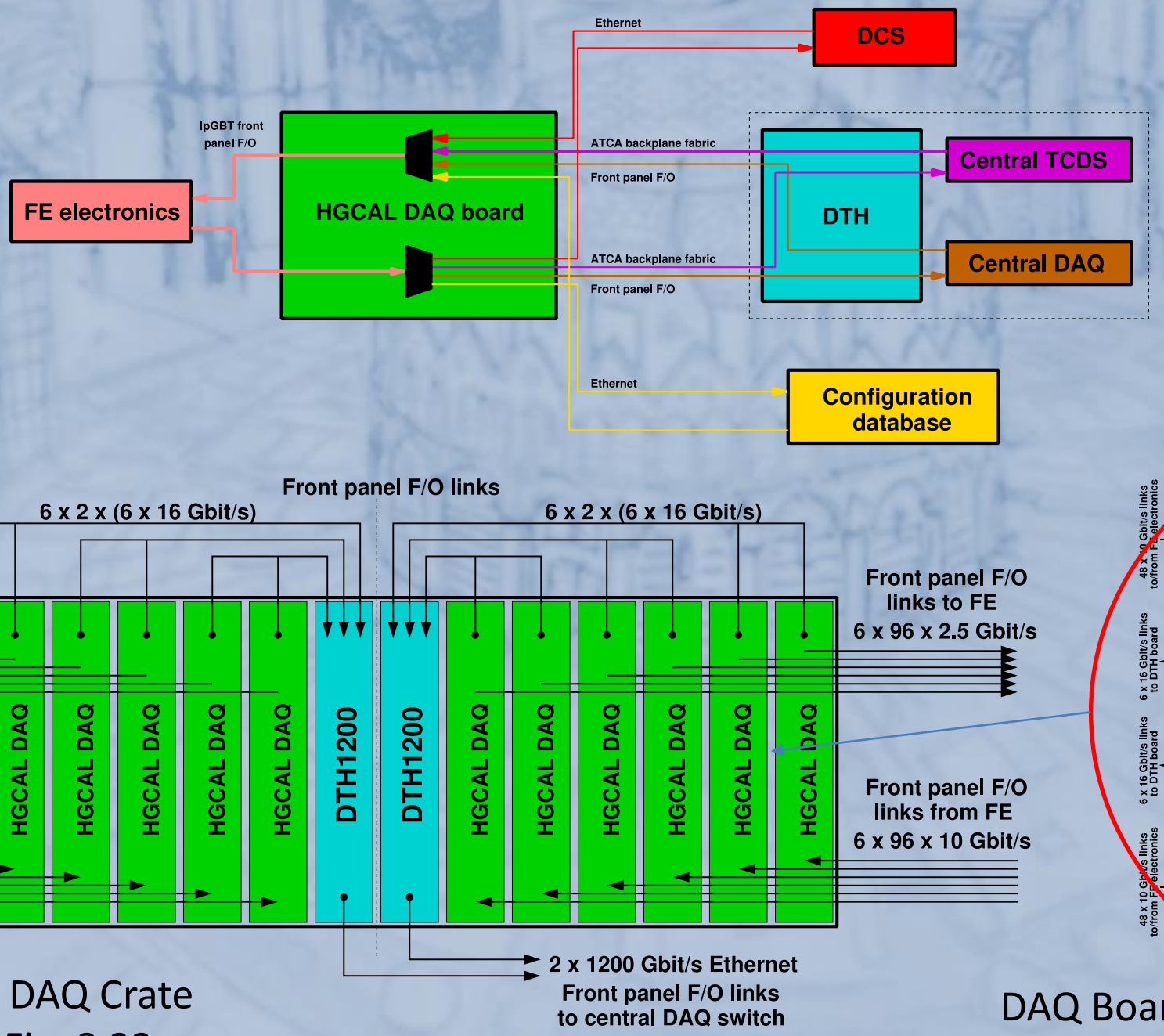
Tile Board
TDR Fig 7.27



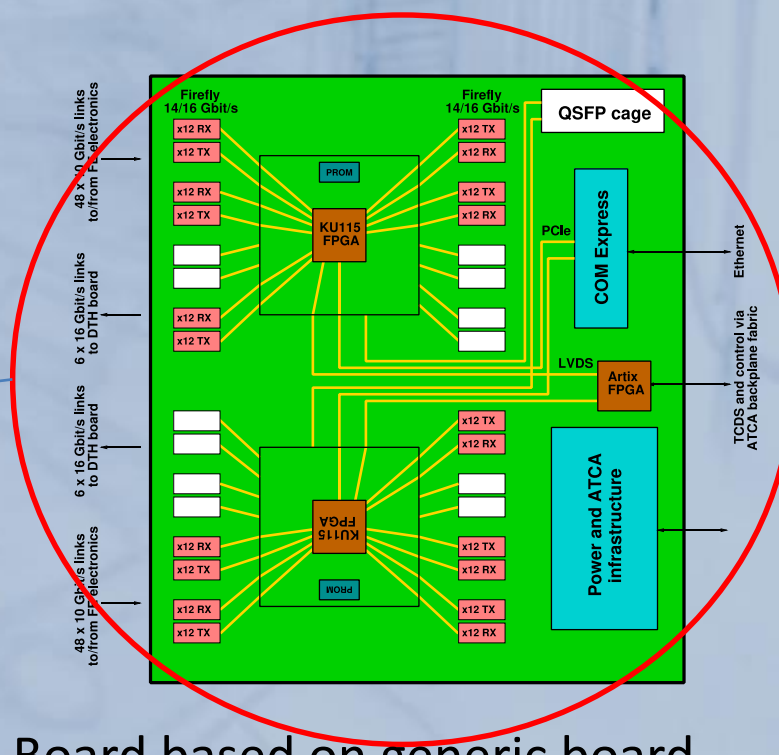
Tile Boards connecting to Motherboard
TDR Fig. 8.21

Back End Electronics: Data path

DAQ interfaces
TDR Fig. 8.30

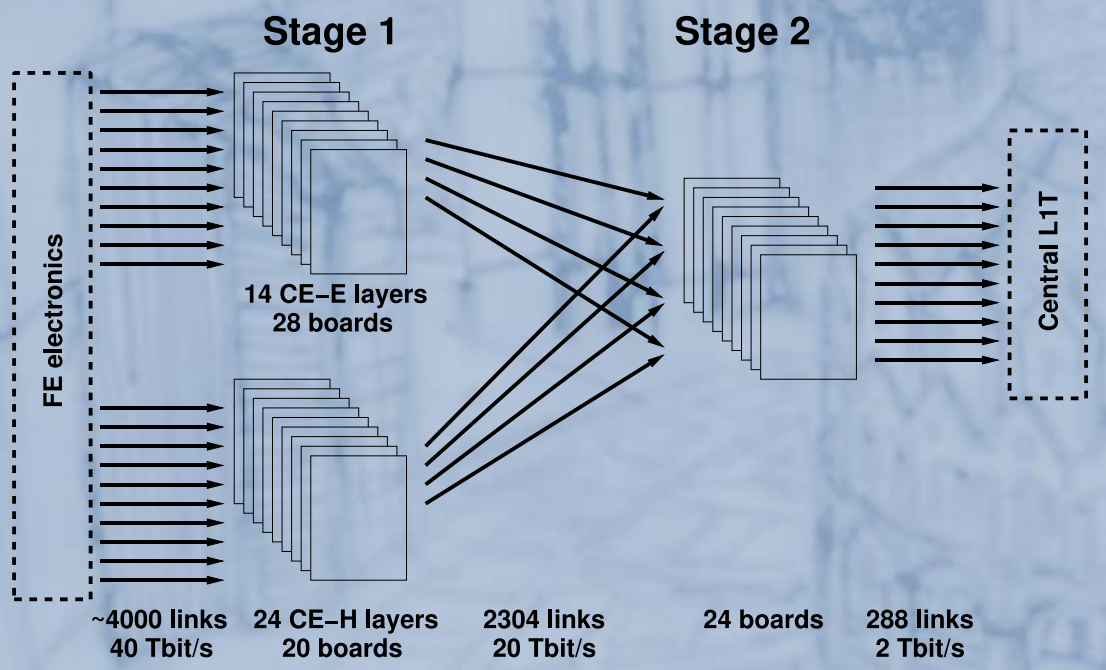


Atca DAQ Crate
TDR Fig. 8.33

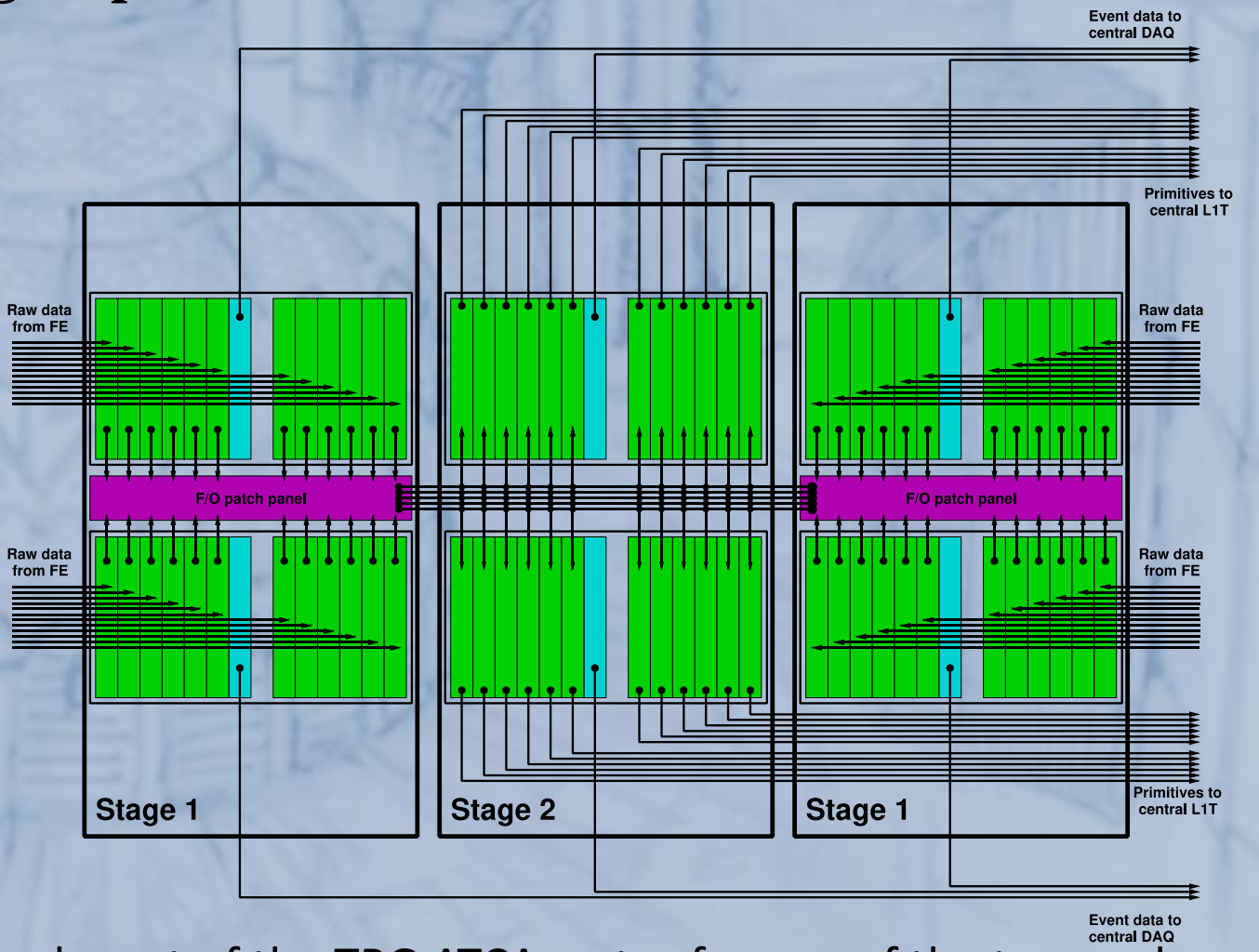


DAQ Board based on generic board
TDR Fig.8.32

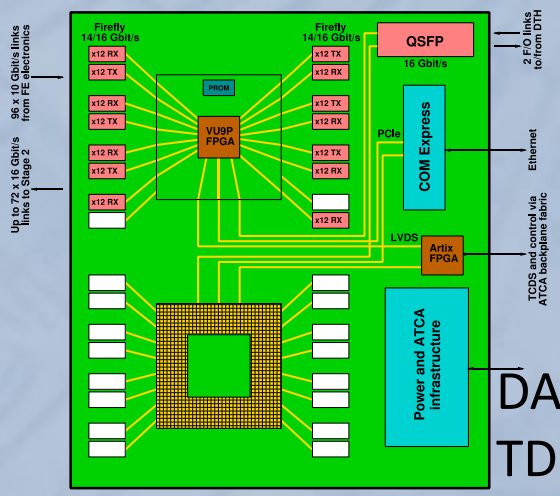
Back End Electronics: Trigger path



Major hardware components of the TPG for one endcap TDR Fig. 3.10



layout of the TPG ATCA crates for one of the two endcaps TDR Fig.8.44



DAQ Board based on generic board TDR Fig.8.43

Quantities Back End*

item	Quantity in CMS	
DAQ boards	84	
DTH 1200 Gb.s boards	14	2 per crate
DAQ crates	7	
TPG Boards stage 1	96	56 CE-E, 40 CE-H
TPG Boards stage 2	48	24 per endcap
DTH 400Gb/s boards	12	1 crate
TPG crates	12	