Status and Plans of RD53

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On behalf of RD53 Collaboration

RD53 Collaboration

RD53 is a collaboration among **ATLAS-CMS** communities for the development of **LARGE scale pixel chips for ATLAS/CMS phase-2 upgrades**

24 Institutions from Europe and USA:
Annecy-LAPP, Aragon, Bergen, Bonn, CERN, FH-Dortmund, FNAL, INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino), LBNL, Marseille-CPPM, New Mexico, NIKHEF, Orsay–LAL, Paris-LPNHE, Prague IP-FNSPE-CTU, RAL-STCF, Sevilla, Santa Cruz

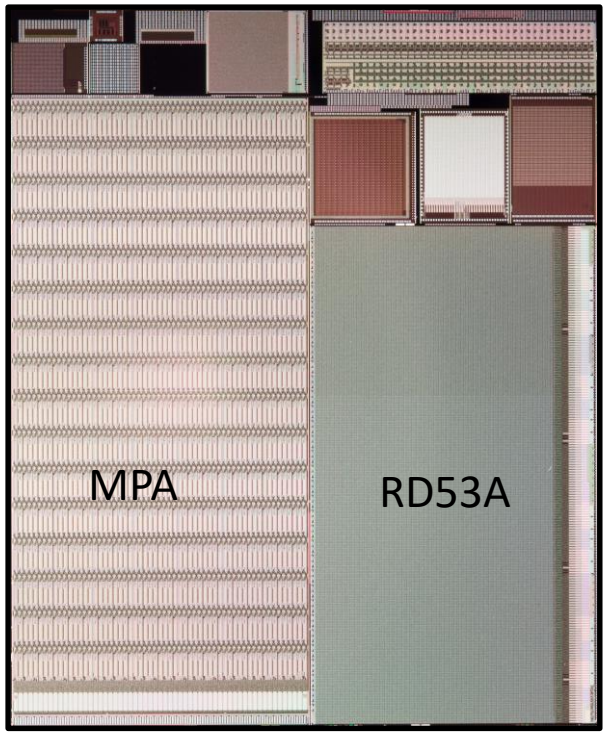
- **65 nm CMOS** is the chosen technology
- **RD53 goals**:
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Development of **tools and methodology** to efficiently design large complex mixed signal chips
  - Design of a **shared rad-hard IP library**
  - Design and characterization of **full sized pixel array chip**

RD53A

– **RD53A** is intended to demonstrate, in large format IC, the suitability of the chosen 65nm CMOS technology for the innermost layers of particle trackers for the HL-LHC upgrades of ATLAS and CMS

– RD53A is not intended to be a final production chip :

- size: 20 x 11.8 mm^2 (half size of production chip)
- 400 columns x 192 rows (50 x 50 μm^2 pixels)
- contains design variations for testing purposes
- wafer scale production allows prototyping of bump bonding assembly with sensor
  → performance measurement
- will form the basis for production designs of ATLAS and CMS: architecture designed to be easily scalable to a full scale chip



– Submitted at the end of August 2017 (shared engineering run with CMS MPA/SSA and other test chips for cost sharing)

RD53A Specifications

Technology	65 nm CMOS
Pixel size	50x50 um^2
Pixels	400x192 = 76800 (50% of production chip)
Detector capacitance	< 100 fF (200 fF for edge pixels)
Detector leakage	< 10n A (20 nA for edge pixels)
Detection threshold	<600 e-
In-time threshold	<1200 e-
Noise hits	< 10^{-6}
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1 MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤ 1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500 Mrad at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1 W/cm^2 including ShLDO losses
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

http://cds.cern.ch/record/2113263

RD53A core design team

RD53A chip: Jorgen (CERN), Maurice (LBNL)
- Specifications
- Documentation
- General organization

RD53A chip integration/verification: Flavio (Bari), Deputy: Tomasz (Bonn)

Floorplan: Flavio(Bari), Dario(LBNL)
- Pixel array, Bump pad
- EOC
- Power distribution
- Bias distribution
- Analog/digital isolation
- Integration/verification

Analog FEs: Luigi (Bergamo/Pavia), Ennio (Torino), Dario (LBNL)
- Specification/performance
- Interface (common)
- Analog isolation
- Digital/timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Distribution of global analog signals
- Verification of integration

Calibration, Monitoring and IP integration: Francesco (Bergamo/Pavia) , Mohsine (CPPM), Flavio (Bari)
- Specification/performance
- Interface
- Analog isolation
- Digital/ timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Verification of integration

Digital: Tomasz (Bonn)
- **Verification framework: Elia (CERN), Sara (CERN)**
  - Framework
  - Hit generation/ import MC
  - Reference model / score board
  - Monitoring/verification tools
  - Generic behavioural pixel chip
  - SEU injection
- **Architecture: Elia (CERN), Sara (CERN), Andrea (Torino), Luca (Torino),**
  - Evaluation – choice: Performance, Power, Area, ,
  - Simulation/Optimization
  - Functional Verification
  - SEU immunity
- **Pixel array/pixel regions: Sara (Cern), Andrea (Torino)**
  - Latency buffer
  - Core/column bus
- **Readout/control interface: Roberto (Pisa), Francesco (Parigi)**
  - Data format/protocol
  - Rate estimation / Compression
  - Implementation
- **Configuration: Roberto (Pisa), Andrea (Torino), Luca (Torino)**
  - External/internal interface
  - Implementation
- **Implementation: Dario (LBNL), Luca(Torino), Andrea (Torino), Sara (CERN)**
  Script based to "quickly" incorporate architecture/RTL changes
  - RTL - Synthesis
  - Functional verification
  - SEU verification
  - P&R
  - FE/IP integration
  - Clock tree synthesis
  - Timing verification
  - Power verification
  - Physical verification
  - Final chip submission

Digital lib.: Dario (LBNL), Mohsine (CPPM), Sandeep (FNAL)
- Customized rad tol library
- Liberty files (function, timing, etc.) Characterized for radiation
- Custom cells (Memory, Latch, RICE)
- Integration with P&R
- Radiation tolerance
- Integration in design kit

Power: Michael (Dortmund), Sara (CERN), Stella (CERN)
- Shunt-LDO integration
- On-chip power distribution
- Optimization for serial powering
- System level power aspects
- Power Verification

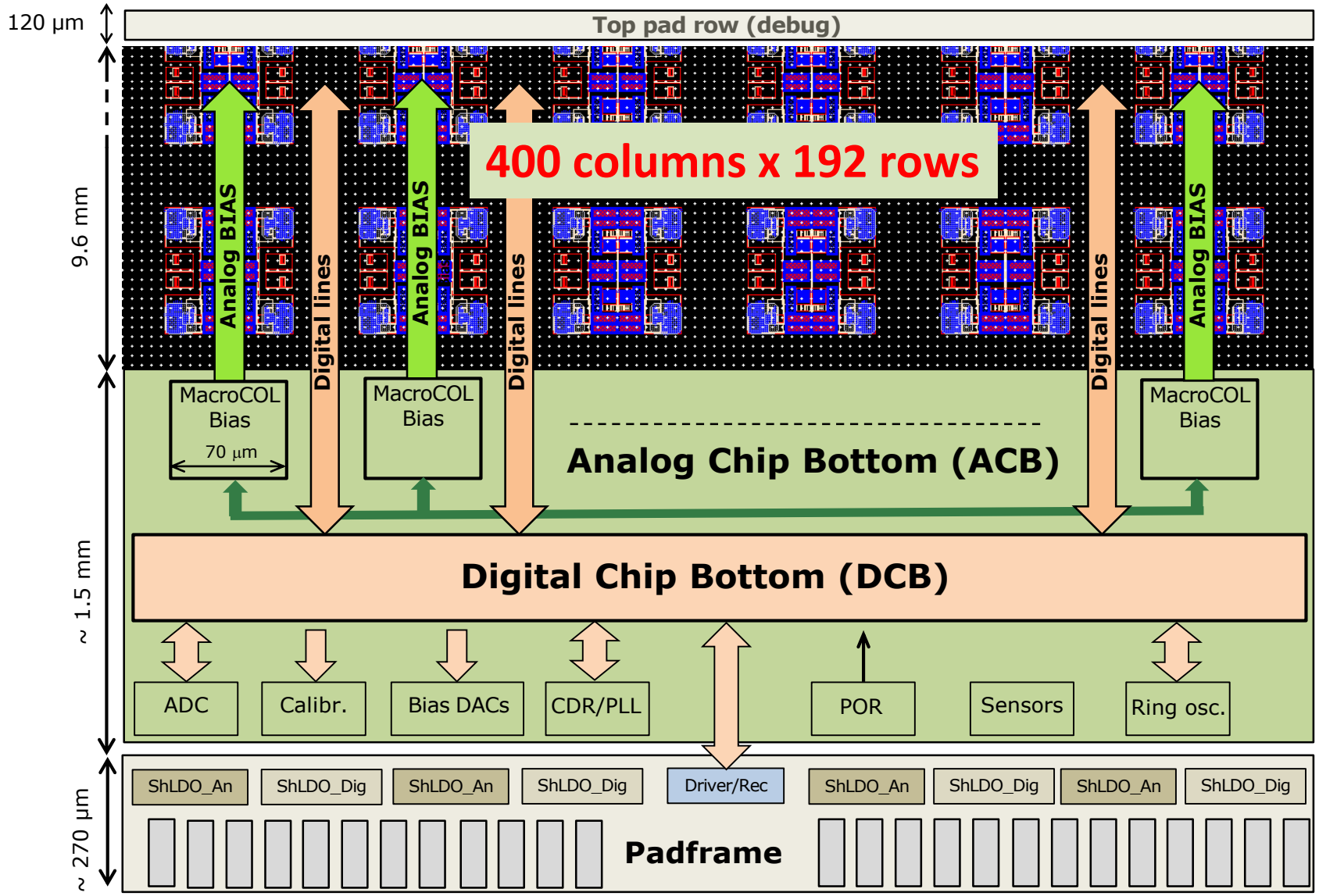
IO PADFRAME: Hans (Bonn)
- Wirebonding pads, ESD, SLVS, Serial readout**, Shunt-LDO**, analog test input/output

Testing optim.: Luca (Torino)
- Testability
- Scan path

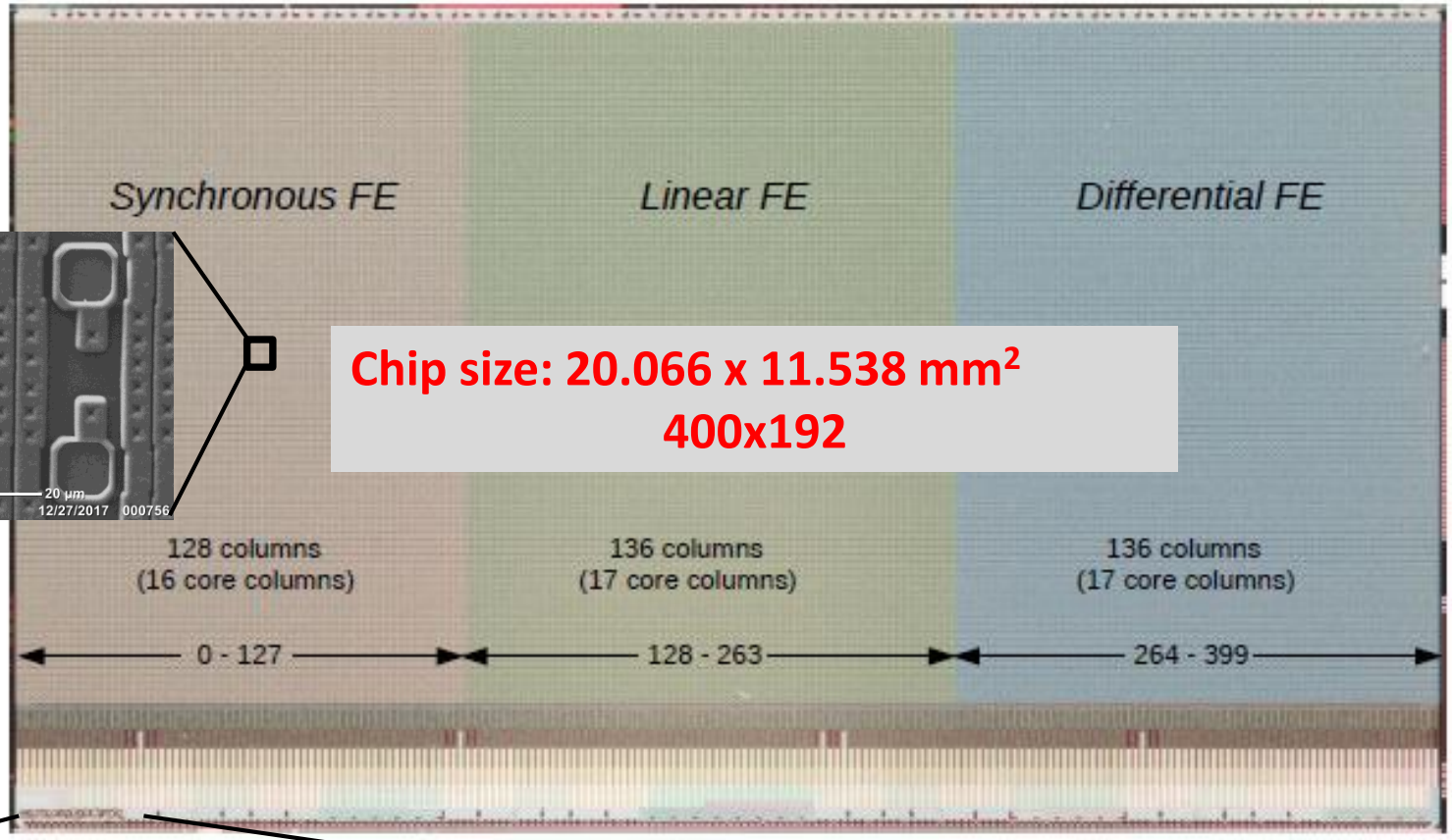
Support and services:
- Tools, design kit: **Wojciech (CERN)**
- Cliosoft repository: **Elia (CERN), Wojciech (CERN)**
- Radiation effects and models: **Mohsine (CPPM)**

+ IP designers from RD53 Institutes

RD53A functional floorplan



RD53A



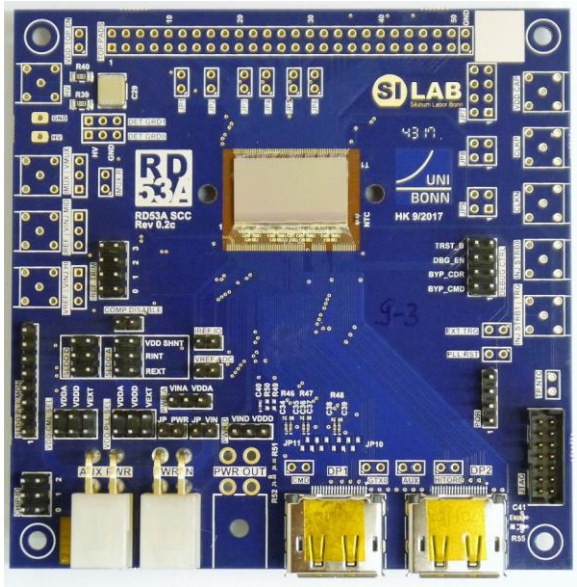
Chip size: 20.066 x 11.538 mm²
400x192

- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**

Chip doc on CDS: http://cds.cern.ch/record/2287593

RD53A testing plans #1

RD53A Single Chip Card



- **Two test systems**:
  - **BDAQ53** – Bonn University → https://gitlab.cern.ch/silab/bdaq53
  - **YARR** – LBNL → https://gitlab.cern.ch/YARR/YARR
- **Functional testing** of RD53A (on-going)
- **Distribution** of setups across collaboration has started

Weekly RD53A testing meetings with latest test results, where anybody from ATLAS and CMS pixel communities can join in

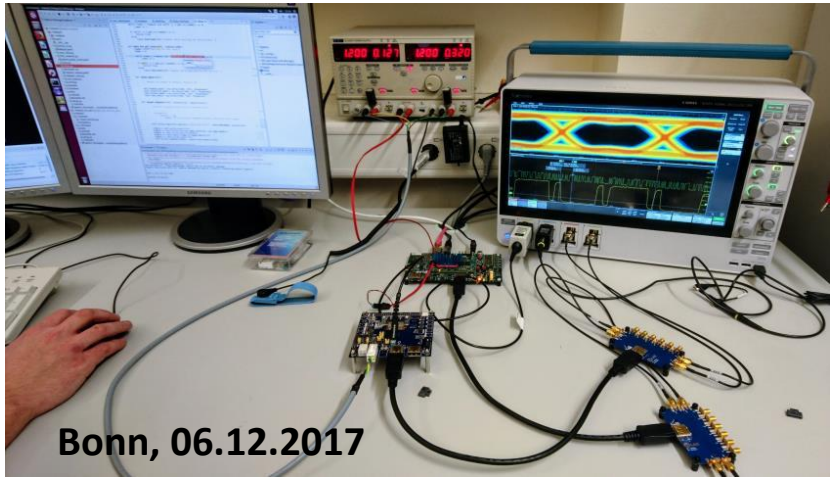
RD53A public plots: https://twiki.cern.ch/twiki/bin/view/RD53/RD53APublicPlots

RD53A testing plans #2

- **Radiation campaigns** in different sites
  - X-rays @CERN (March 2018: done, next period at the end of April 2018)
  - Low dose rate X-rays irradiation (May-June)
  - Gammas, protons, …. : being planned
- **Wafer probing**:
  - Developed needle probes card for fast sequential testing of RD53A on wafers
  - Probe testing being debugged with single chips. Whole wafer probing to begin soon
- **Bump-bonding with first sensors**:
  - 3 wafers under processing at IZM for bump-bonding to CMS and ATLAS sensors (April 2018)

RD53A measurements

- Preliminary results shown in next slides are from measurements performed by:
  - ❑ Bonn University
  - ❑ CERN
  - ❑ INFN Torino
  - ❑ LBNL
  - ❑ FH-DORTMUND



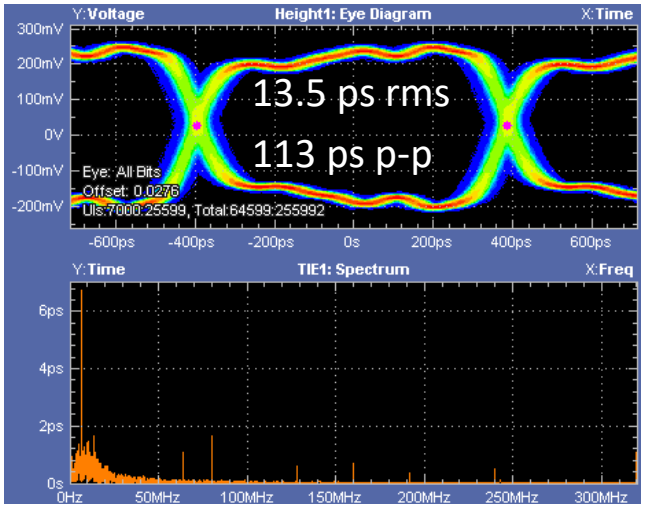
- **The chip is fully operating using its normal I/O ports (no backup)**
  - **160 Mbps CMD input (LVDS) → Clock + Data**
  - **CML output (Aurora link)**

- PLL locks
- Aurora link is stable (single link @ 1.28 Gbps)
- Command decoder responds → We can configure and readout the chip

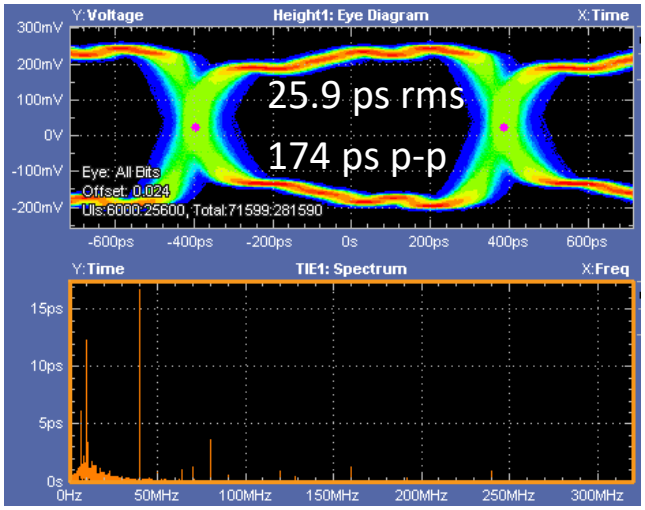
CDR/PLL

- The CDR/PLL recovers data and clock from input stream @ 160 MHz
- It works fine but in certain conditions we encounter a lock issue currently being investigated. Proposed solution is under verification across supply, T and radiation and will allow to operate RD53A reliably in the different test sites
- Moreover, it exhibits a jitter higher than expected from simulations
- Output link jitter strongly influenced by chip activity

No CLK to matrix, all columns off



CLK send to matrix, all columns on

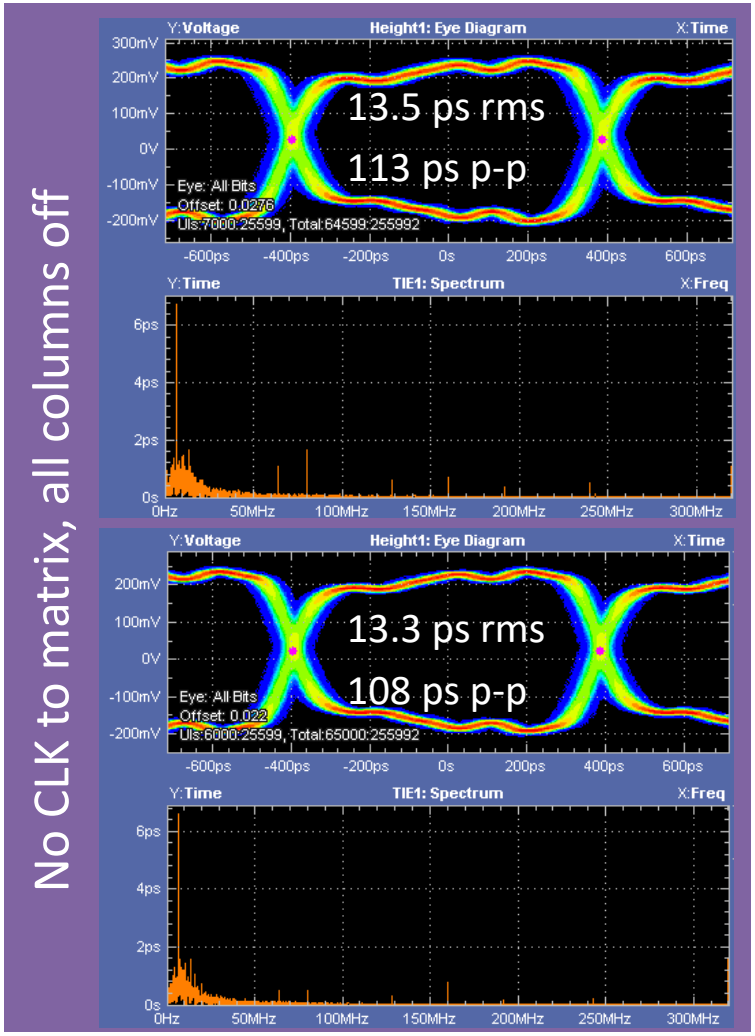


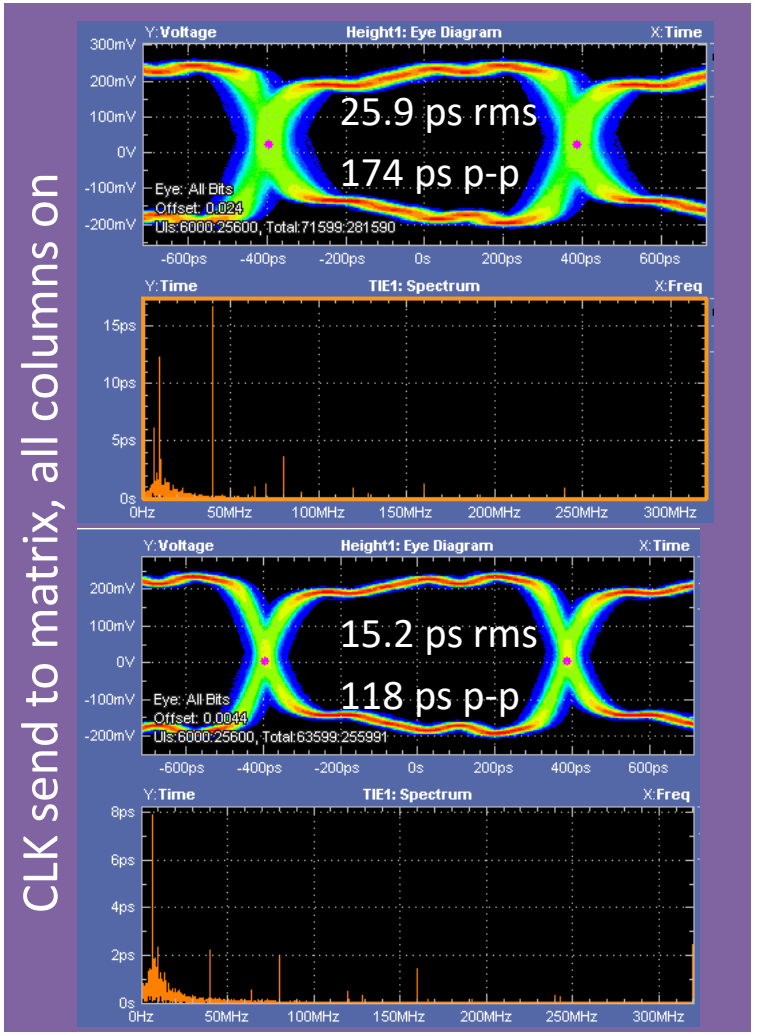
Jitter problem caused by missing buffers for the configuration bits
Confirmed by surgical fix in few chips using FIB (Focused Ion Beam) → see next slide

CDR/PLL post FIB measurements

Not modified

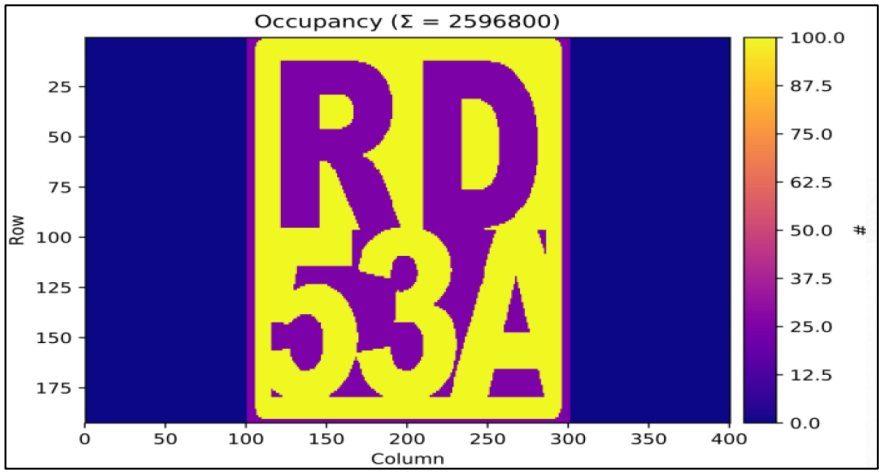
FIB edited



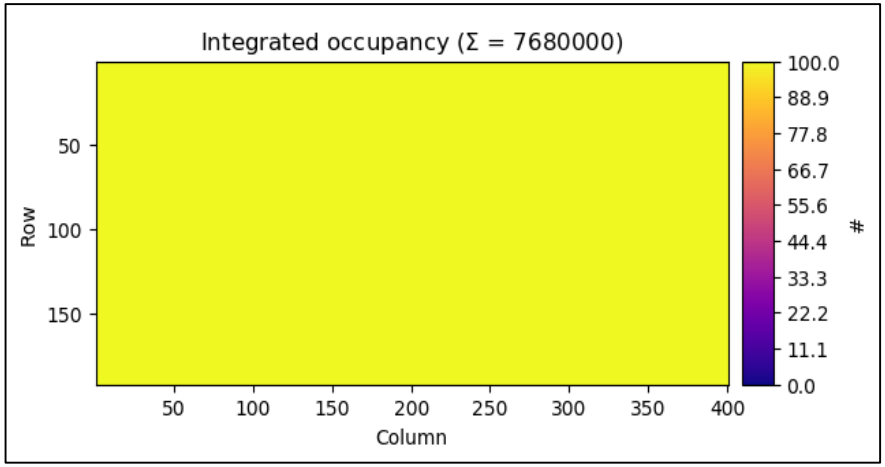


- Bug fix implemented for production chip
- Prototype submission in summer to test farther improvements

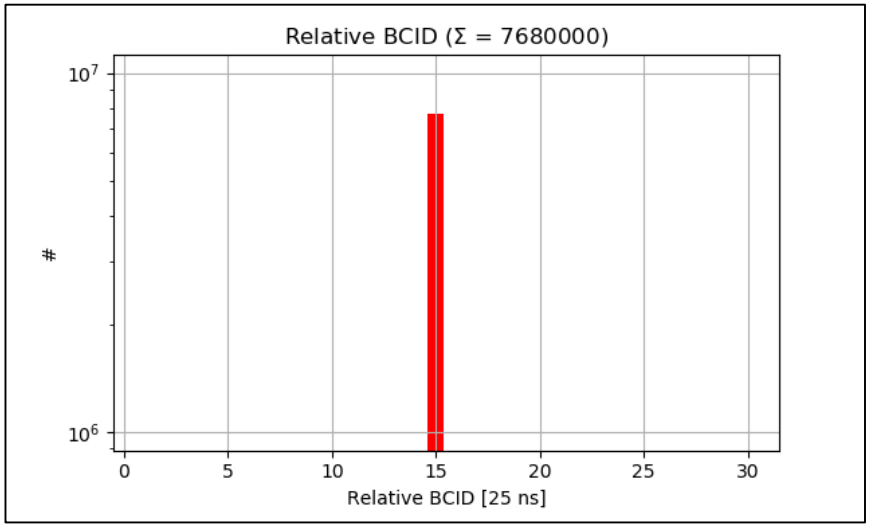
Digital scan (all FE flavours)

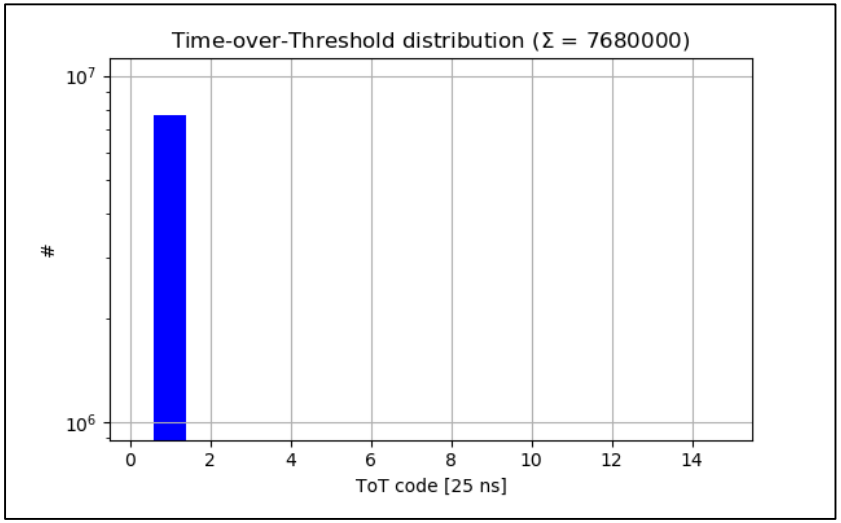


Complex mask



Full chip

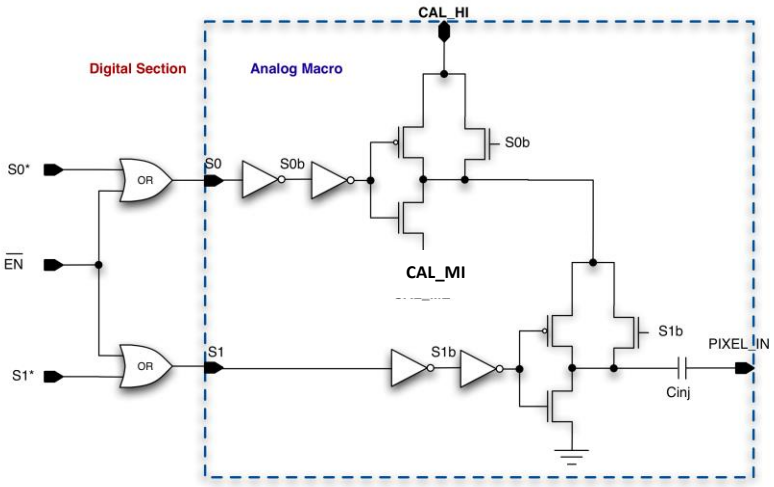




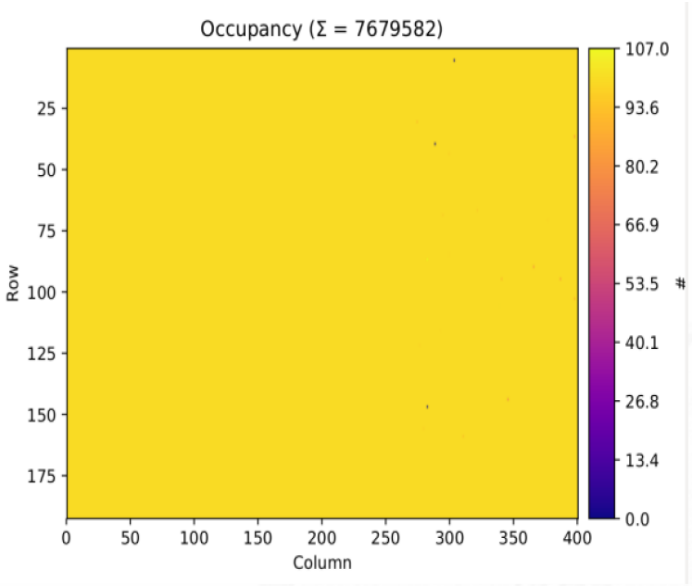
Analog scan (all FE flavours)

Calibration circuit (inside pixel)

- Local generation of the analog test pulse starting from 2 DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)
- Two operation modes which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time
- Cal levels generated by 12 bit VDACs



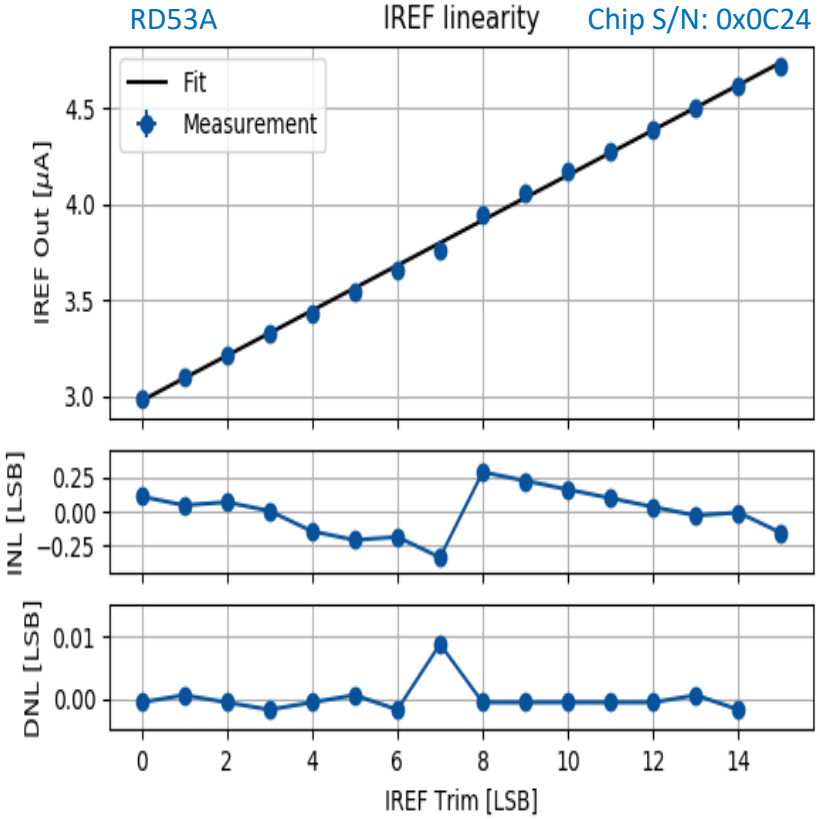
- Full chip responds
- High injection (30 ke$^-$)

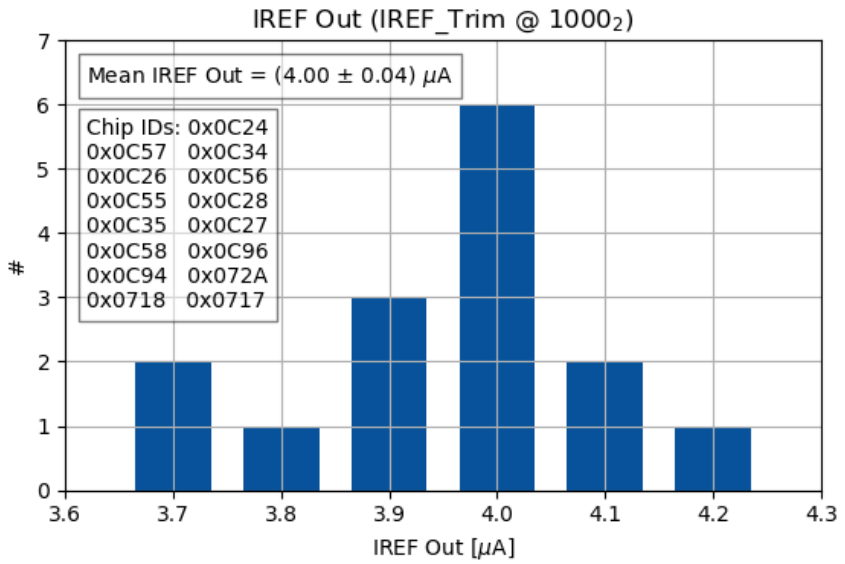


Bias, calibration and monitoring

IREF measurement and trimming

- All biases are provided by internal current DACs, using an internally generated reference current IREF (**4 µA** nominal) derived by a Bandgap Reference circuit (independent from T, tolerant to TID)
- To compensate for process variations, we can tune IREF by means of 4-bit DAC (wire bonding settings)

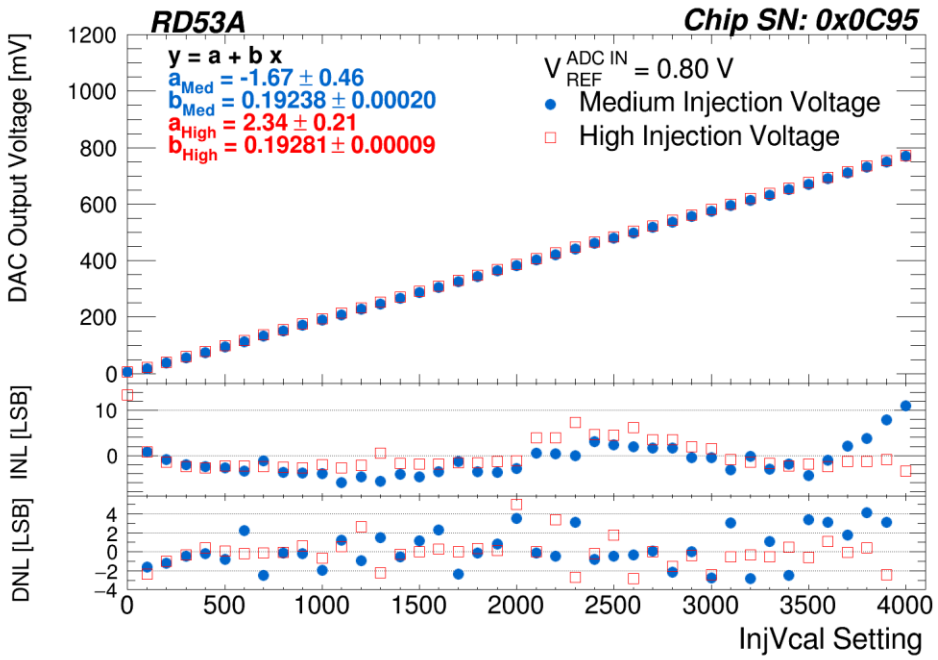




Statistical evaluation of the IREF output for IREF Trimming setting = 8 for a sample of 15 chips

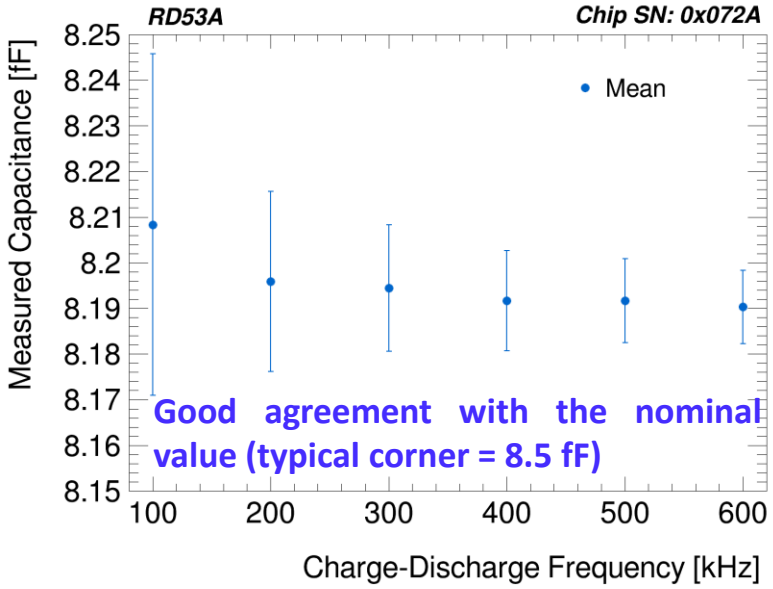
Calibration circuitry *(based on 12-bit DACs and inj. cap)*

Characterization of injection 12-bit DACs



Measurement of injection capacitance

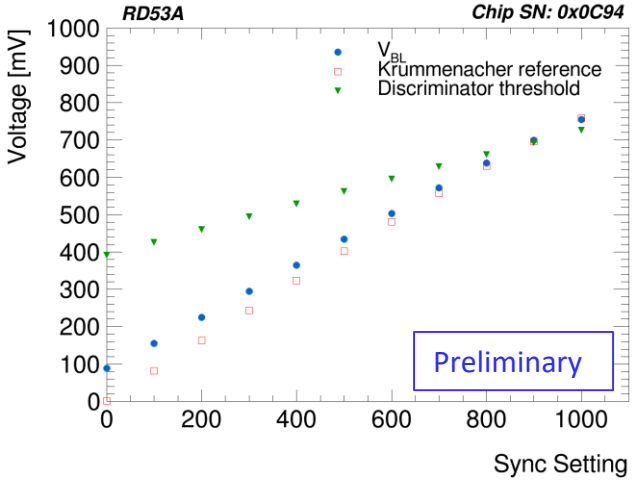
- Each RD53A has two banks of injector capacitors (top left – top right) for the purpose of measuring the capacitance.
- Methodology: cyclically charging and discharging the banks, the capacitance can be deduced from the frequency and measured current

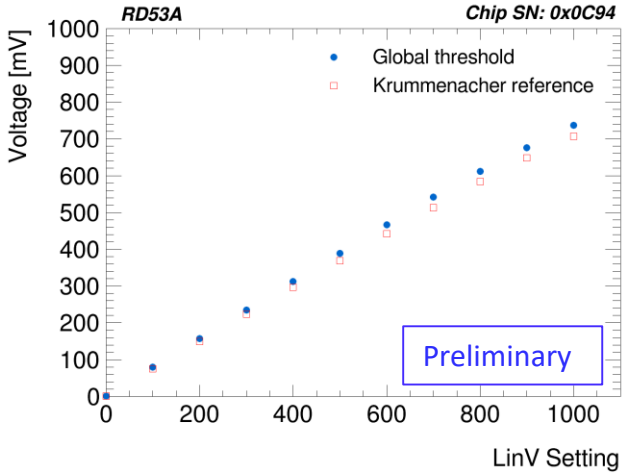


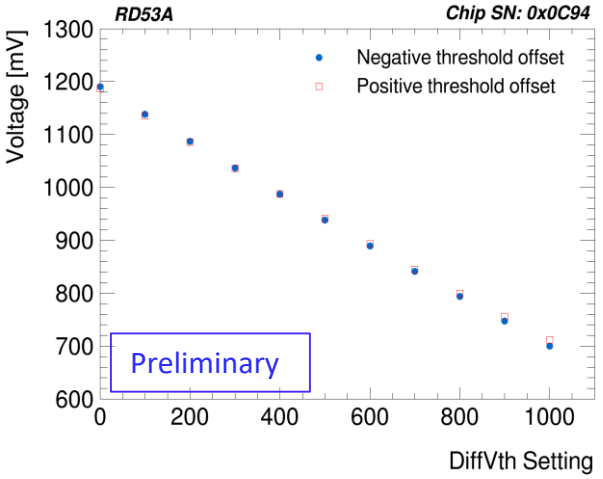
Considering C_{inj} ~ 8.2 fF → Q_{inj} ~ 10 e^-/DAC (close to simulated value 12 e^-/DAC)

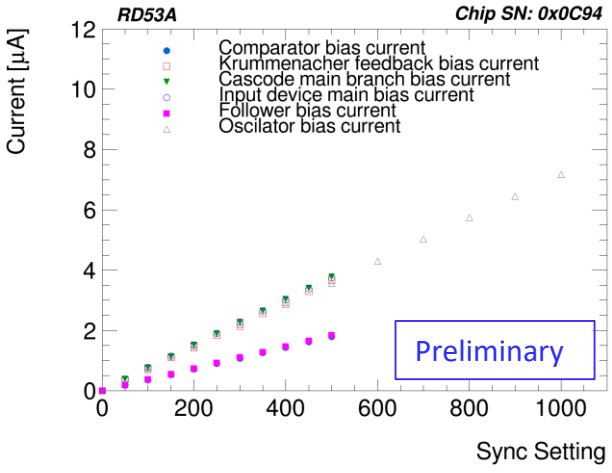
Scan of Bias 10-bit DACs

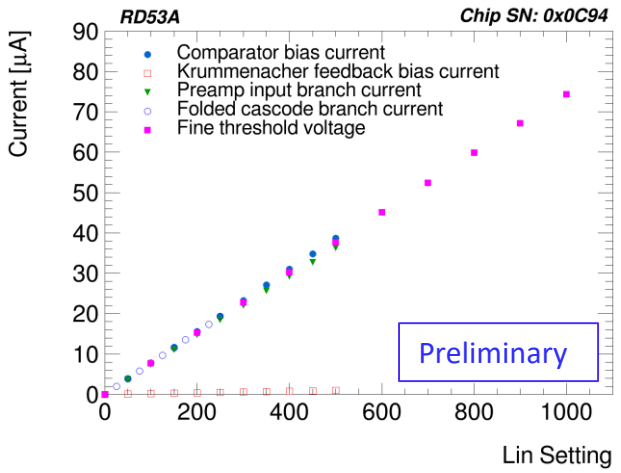
- All internal bias currents and voltages can be monitored using internal 12-bit ADC and can be accessed on two multiplexed outputs: IMUX and VMUX (used also for ADC calibration)
- Voltages on top row, currents on bottom row

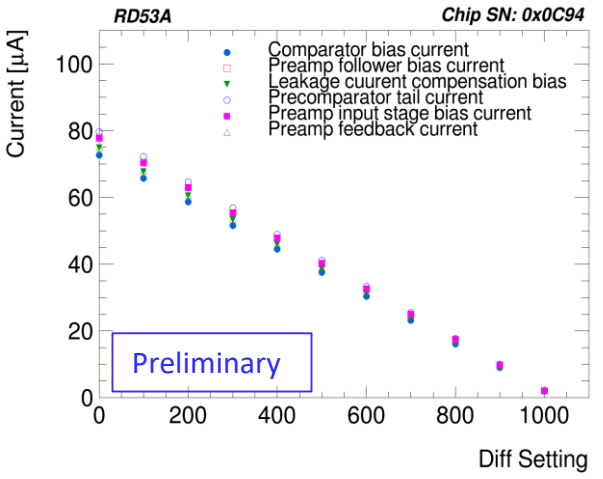








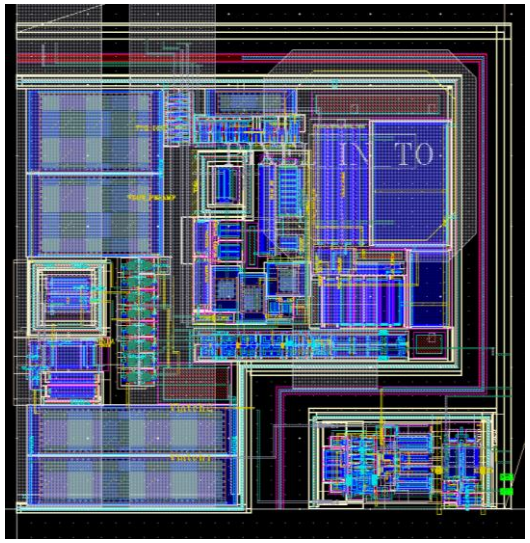


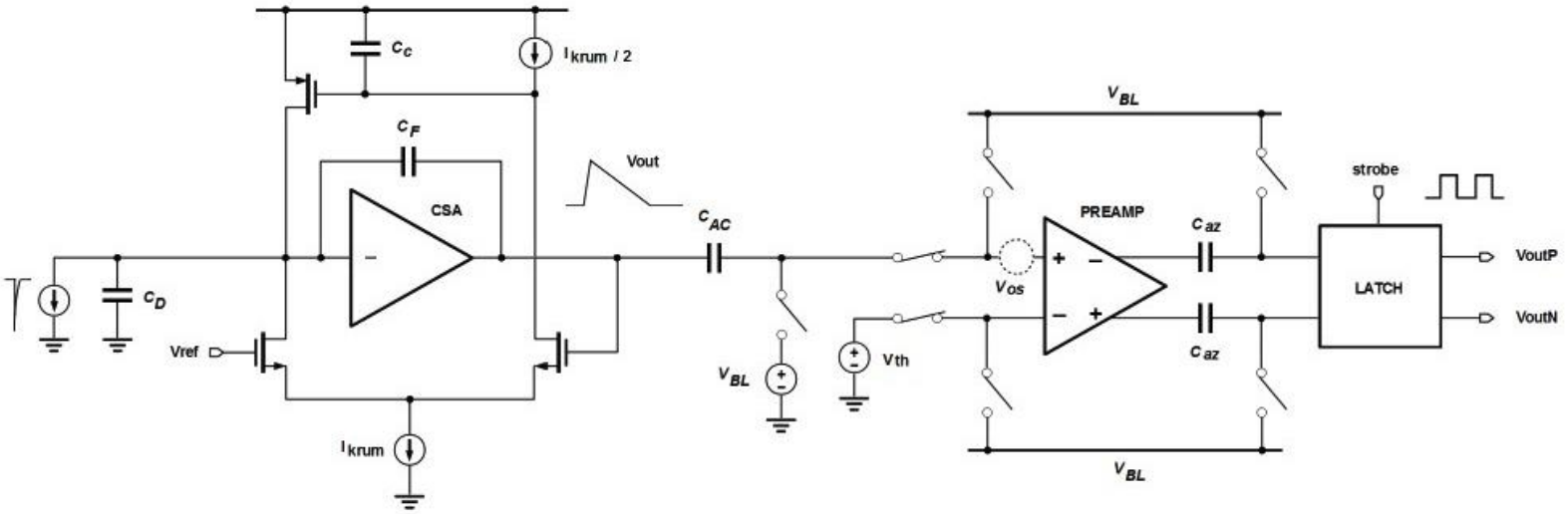


Analog Front-Ends

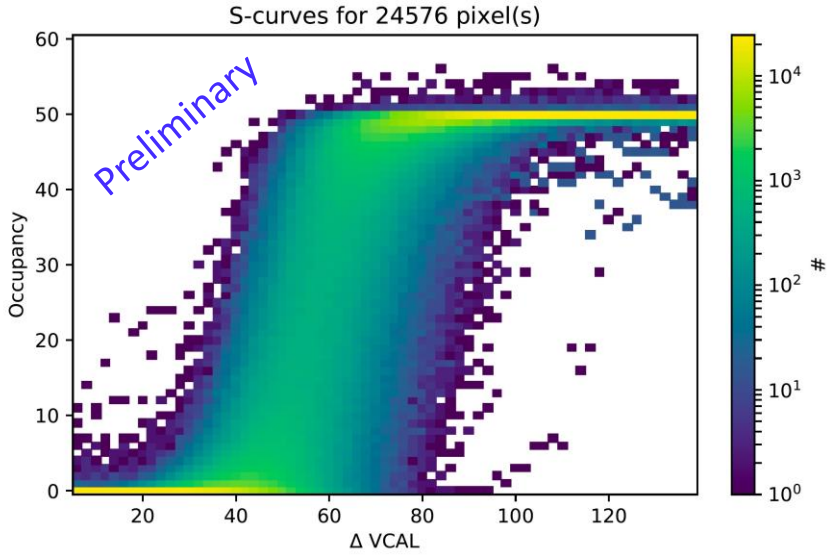
Synchronous FE preliminary results

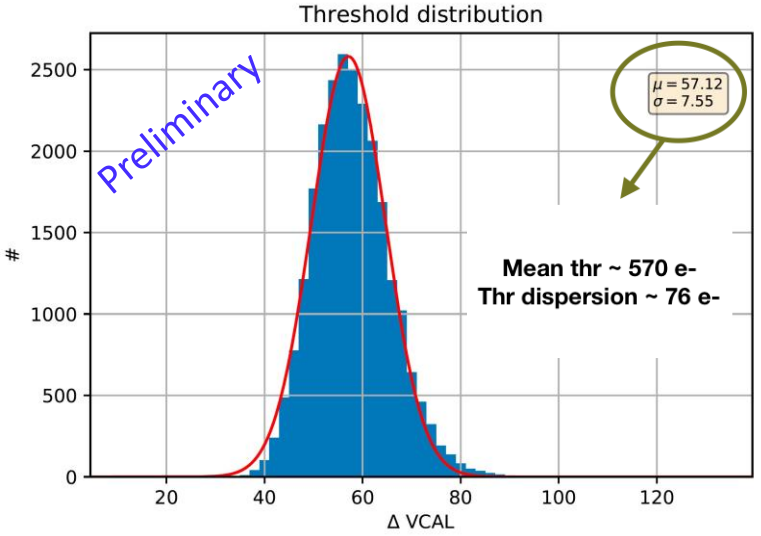
- Telescopic-cascoded CSA with Krummenacher feedback for linear ToT charge encoding
- Synchronous hit discriminator with track-and-latch comparator
- Threshold trimming using the auto-zeroing technique (no local trim DAC)
- ToT counting using 40 MHz clock or fast counting using latch as local oscillator (100-900 MHz)
- Efficient self-calibration can be performed according to online machine operations

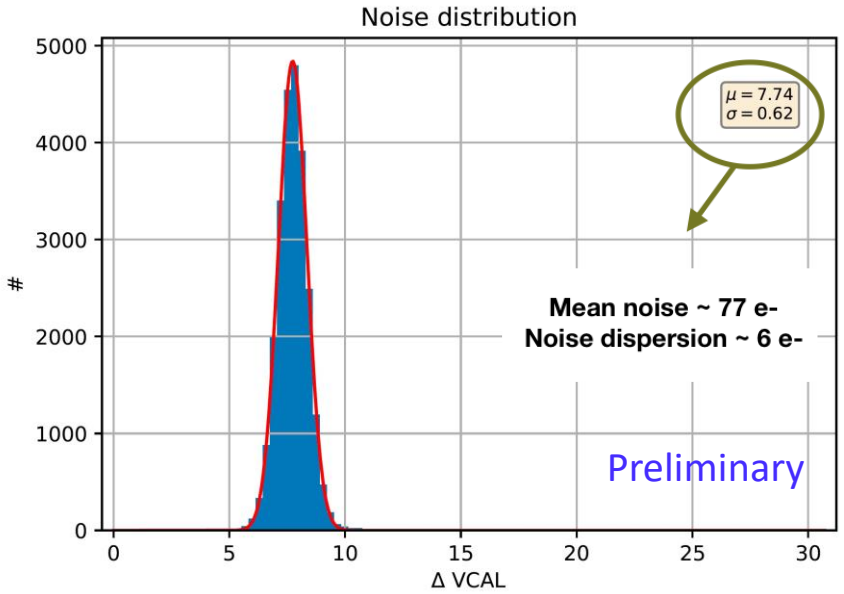


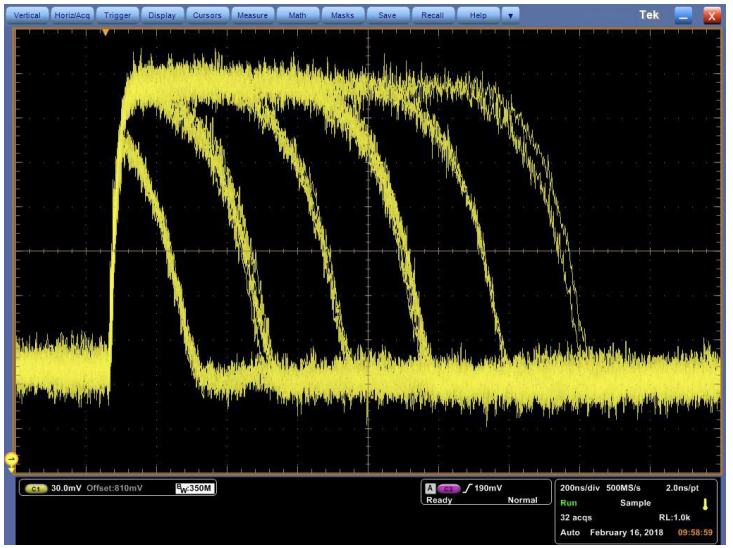


Synchronous FE test results





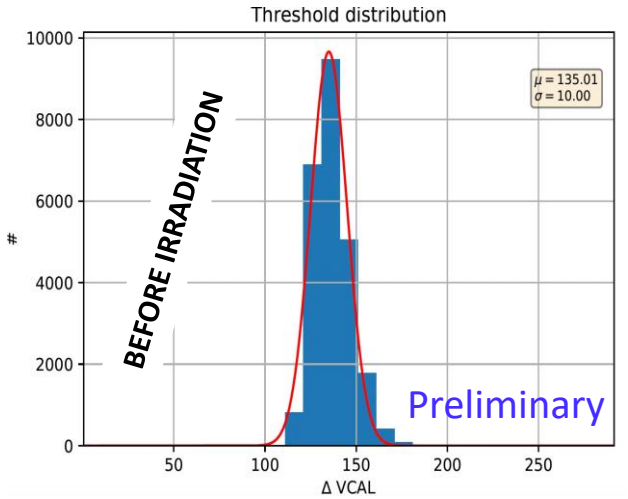


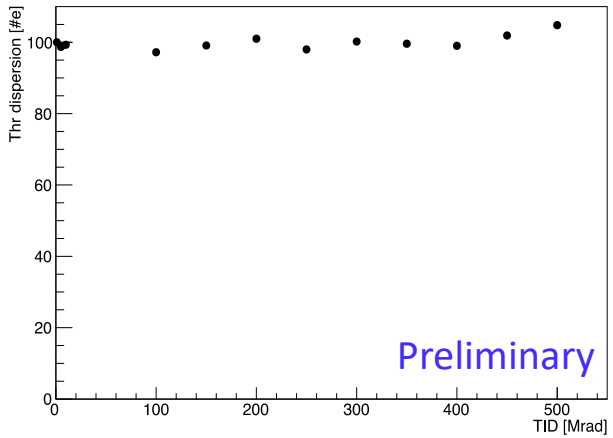


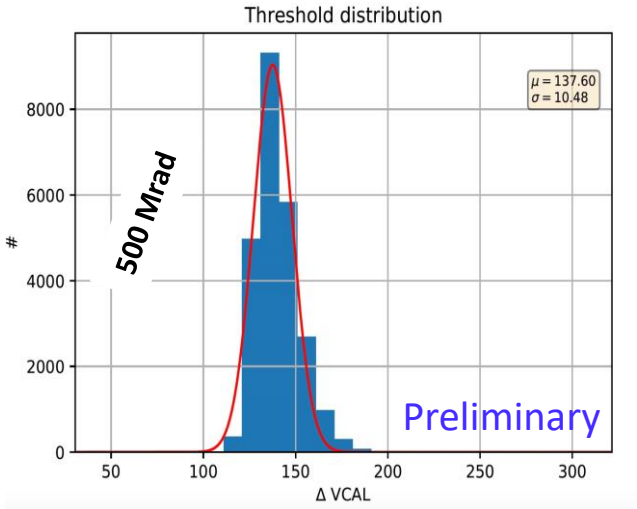
All these values are compliant with simulations

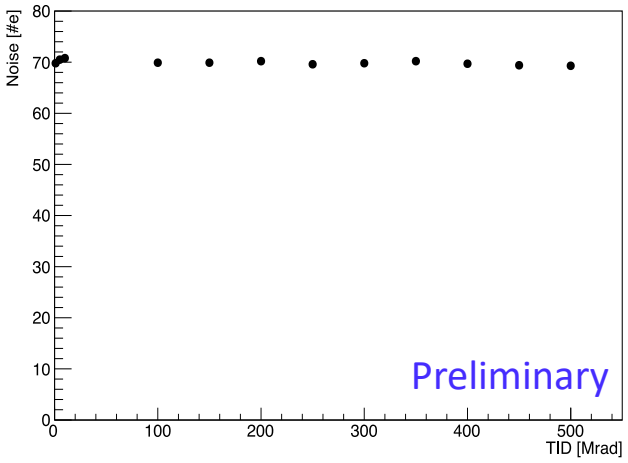
Synchronous FE irradiation test results

An X-ray irradiation campaign has been performed at CERN in March. Results shown here are for a -10°C campaign up to 500 Mrad





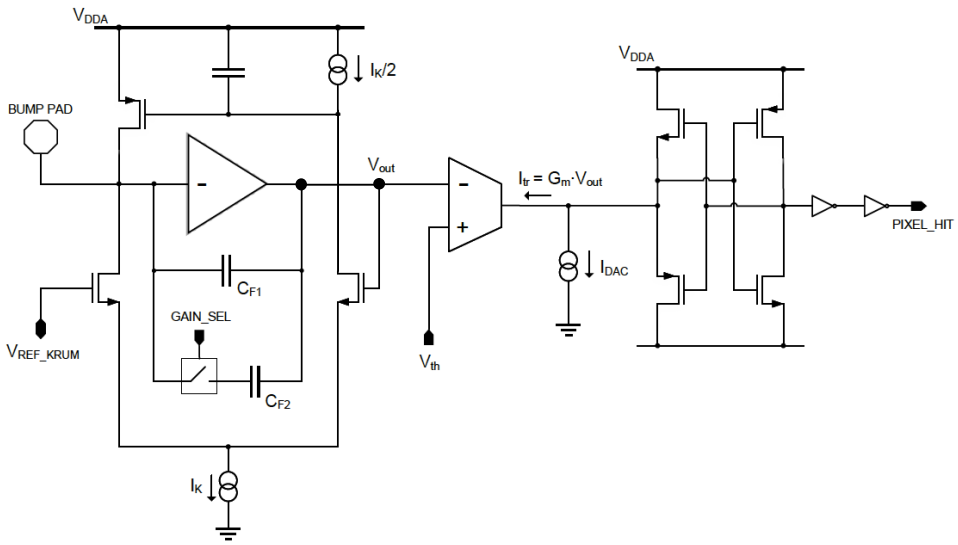


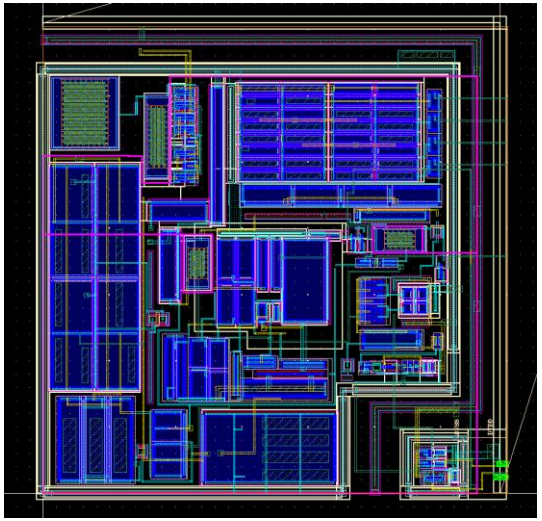


The behavior of the synch FE is very slightly modified by radiation

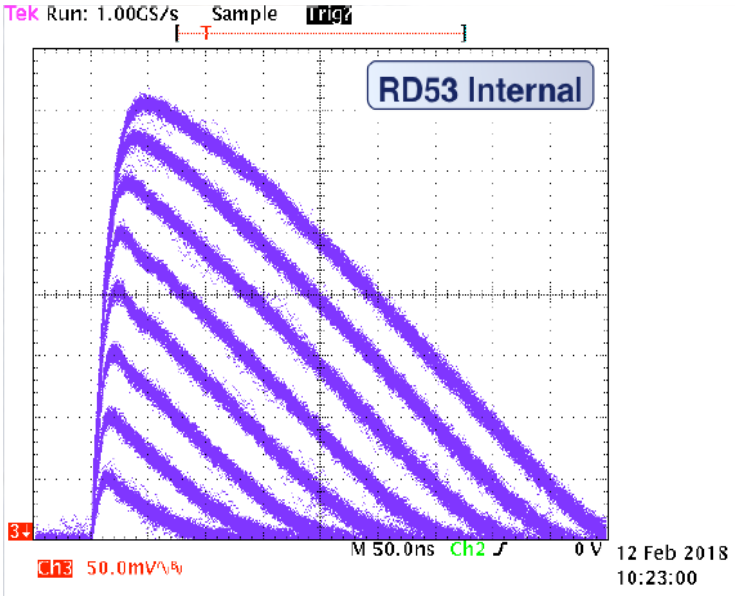
- The threshold dispersion increases of around 5 electrons
- The threshold mean decreases of around 25 electrons
- Both threshold dispersion and noise do not show significant changes as a function of TID

Linear FE results

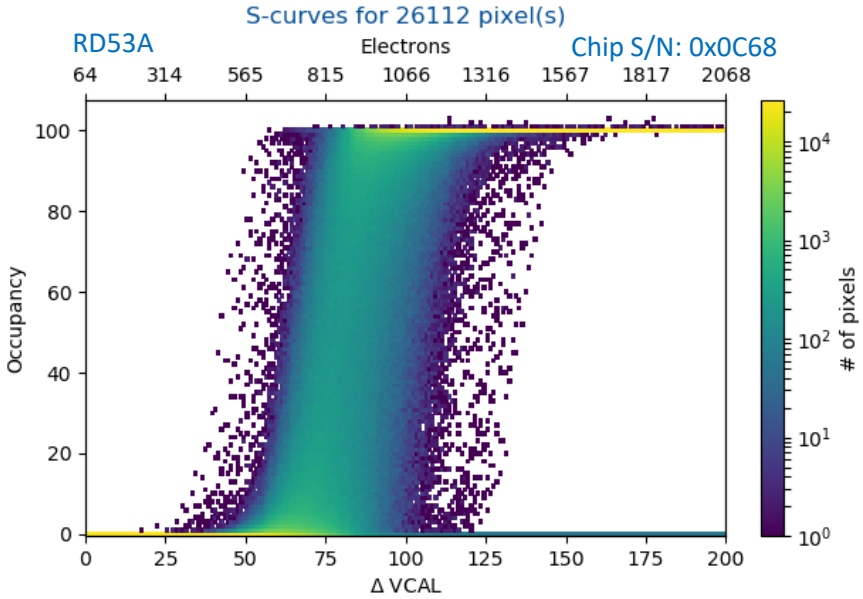


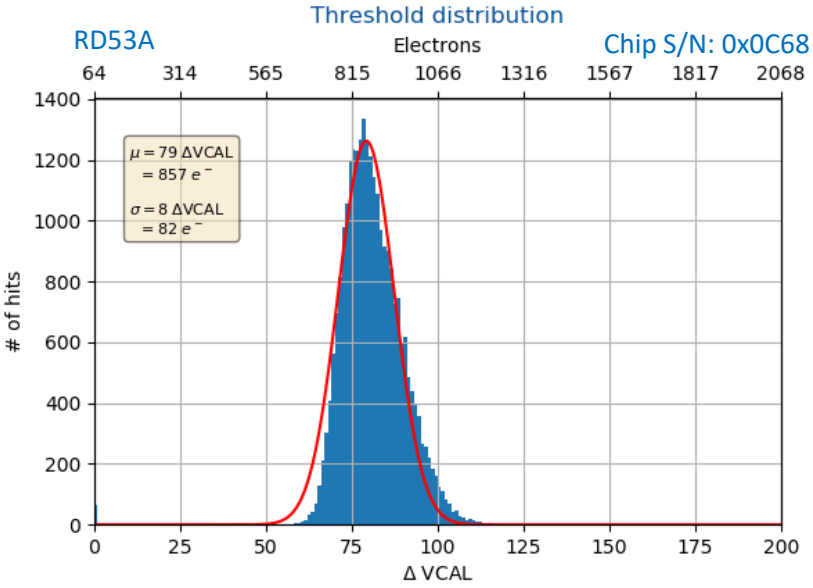


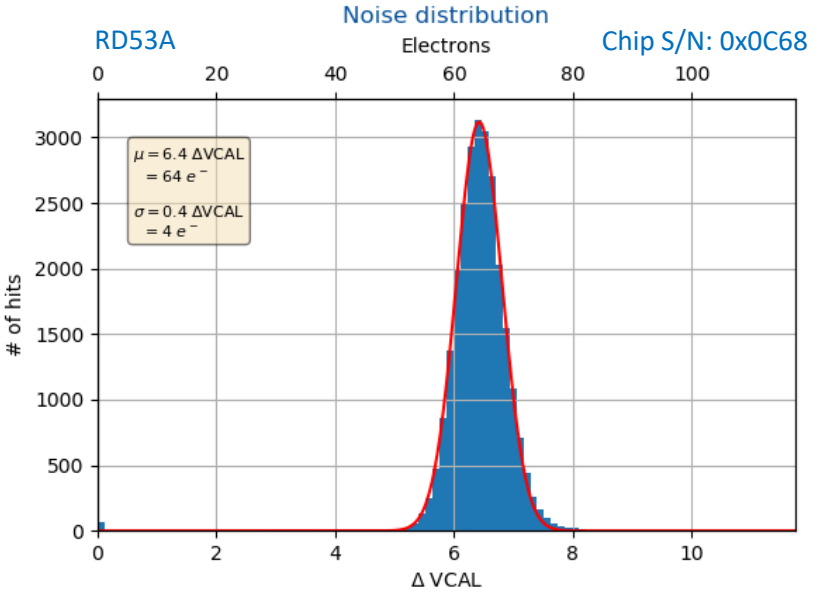
- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Asynchronous, low power **current comparator**
- **4 bit local DAC for threshold tuning**



Linear FE (after noise-based tuning)



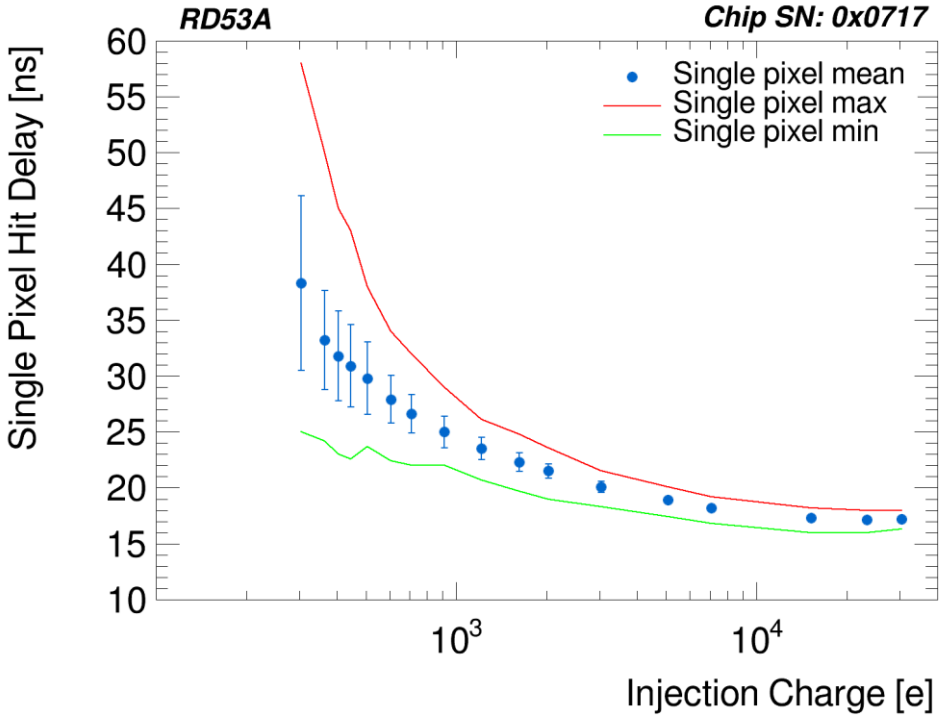




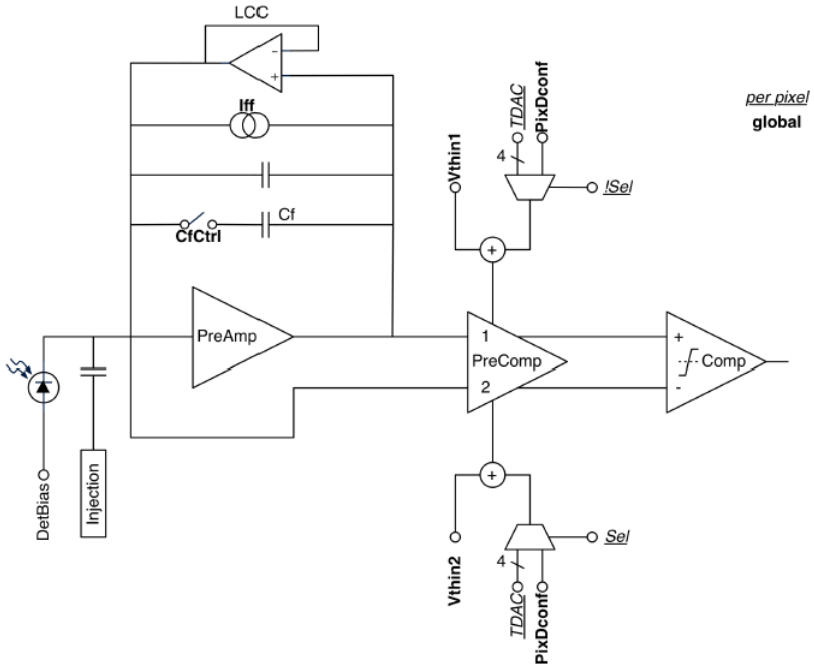
- Linear FE is fully functional and can be operated at low threshold
- Tuning procedure under optimization
- ENC ~ 64 e- rms

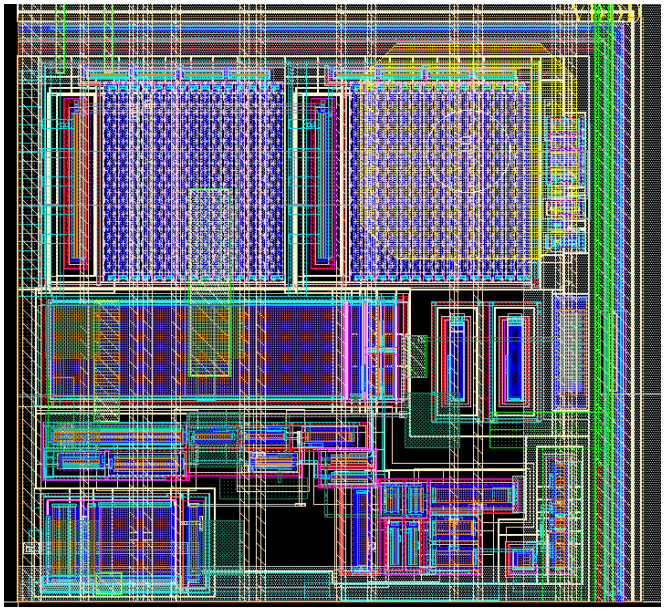
Time Walk of Linear FE

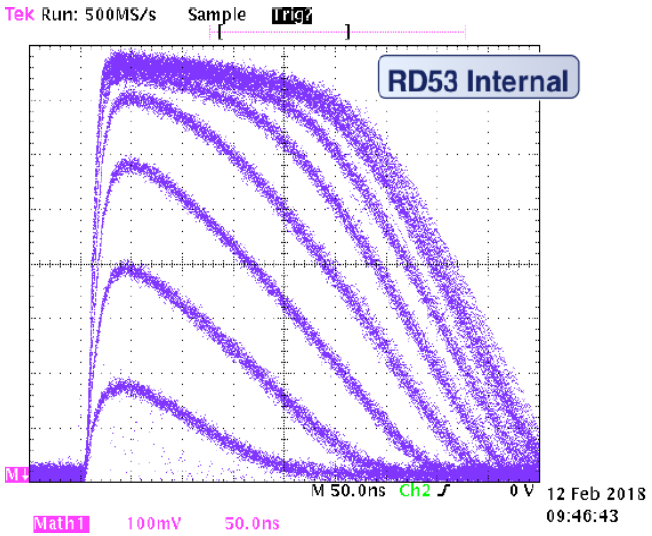
- Hit delay (timewalk) for one pixel in row 0 of the linear front end
- Delay is measured between the injection control signal (Cal_Edge) and the RD53A prompt hit output.
- The observed minimum delay of 17ns includes all internal chip signal propagation delays and scope probe delays, as well as the front end combined delay.
- Threshold for this single pixel ~ 300 e-



Differential FE





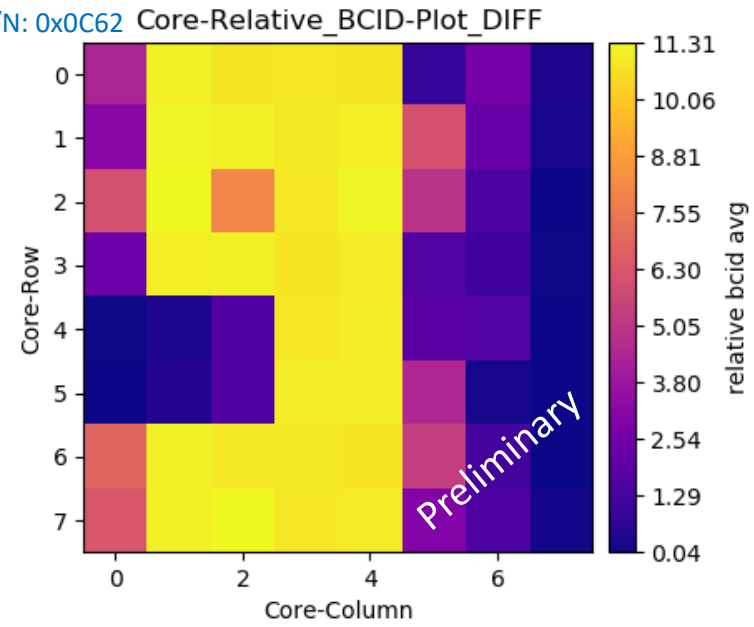


- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation**
- **Threshold adjusting** with global 8bit DAC and local 4+1 bit DAC

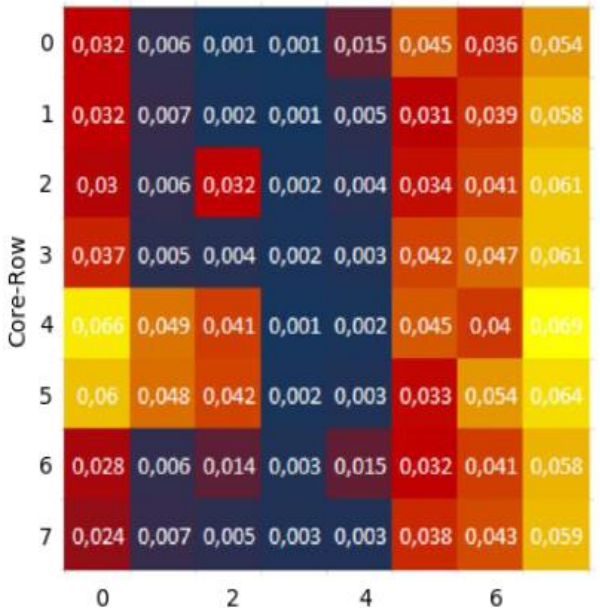
Differential FE

- Bug in the A/D interface: missing P&R constraint on the Diff. FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT
- Will improve A/D verification strategy for production chips

RD53A
Chip S/N: 0x0C62

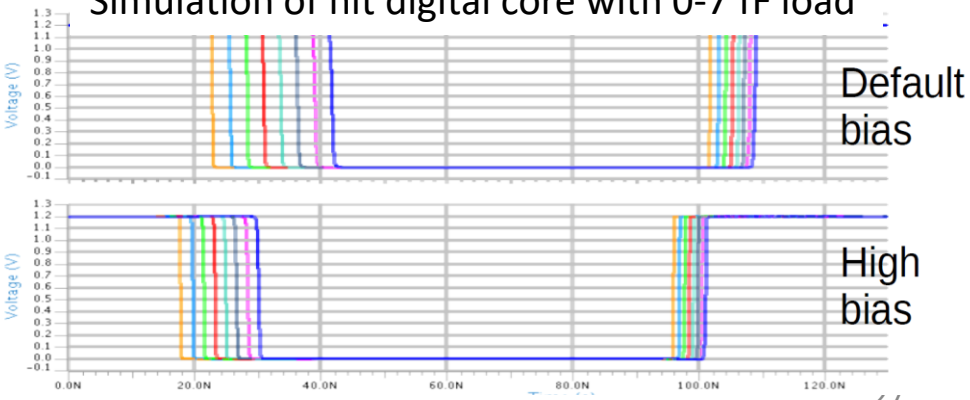


Extracted outdisc net load [pF]



- Partially recovered increasing comparator bias current and decreasing preamp discharge current
- **This bug does not prevent the Diff FE full characterization**

Simulation of hit digital core with 0-7 fF load

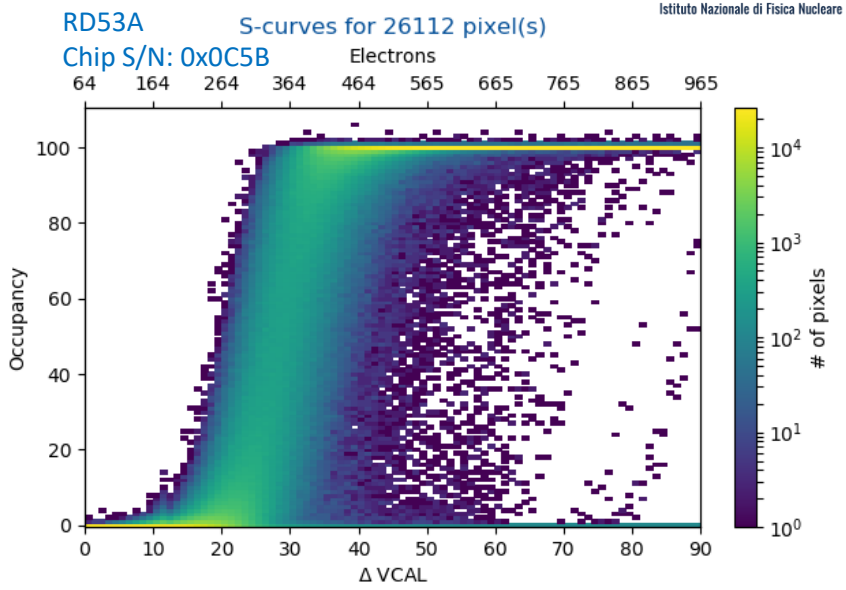


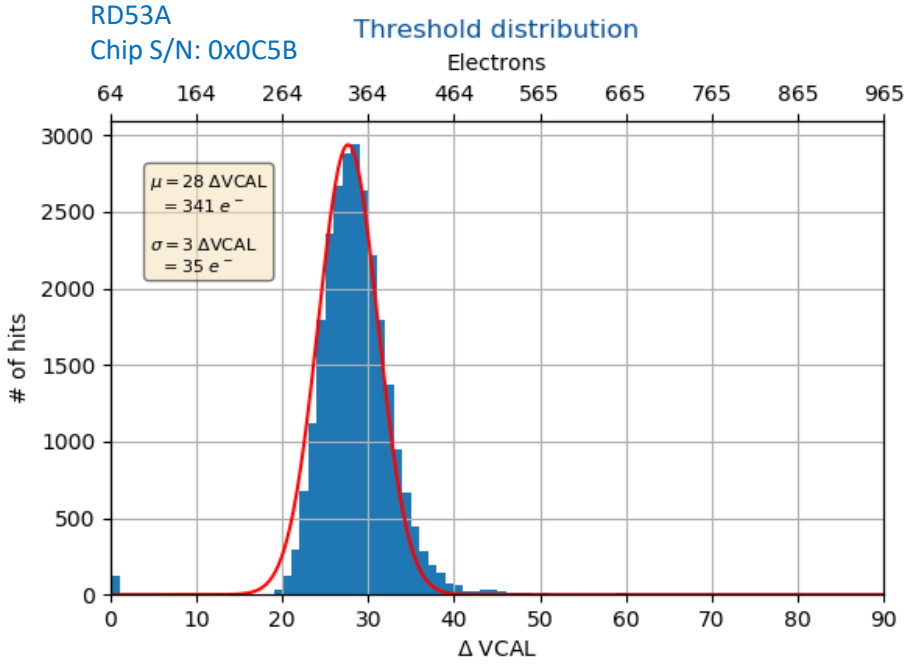
Differential FE (after noise-based tuning)

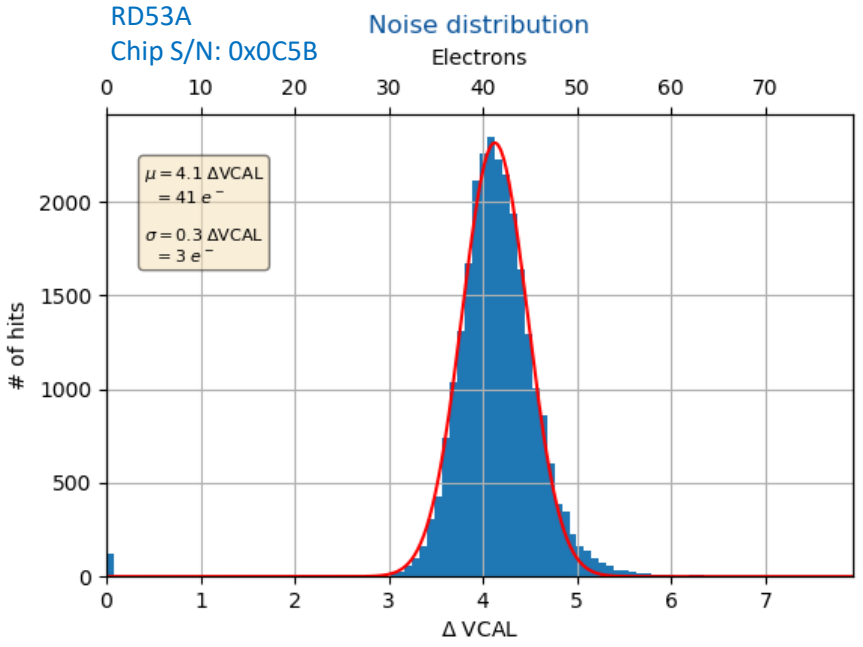
Non default parameters to minimize the effect of load capacitance:

- Increased comparator current
- Decreased discharge preamp. current

→(slower respect to nominal)

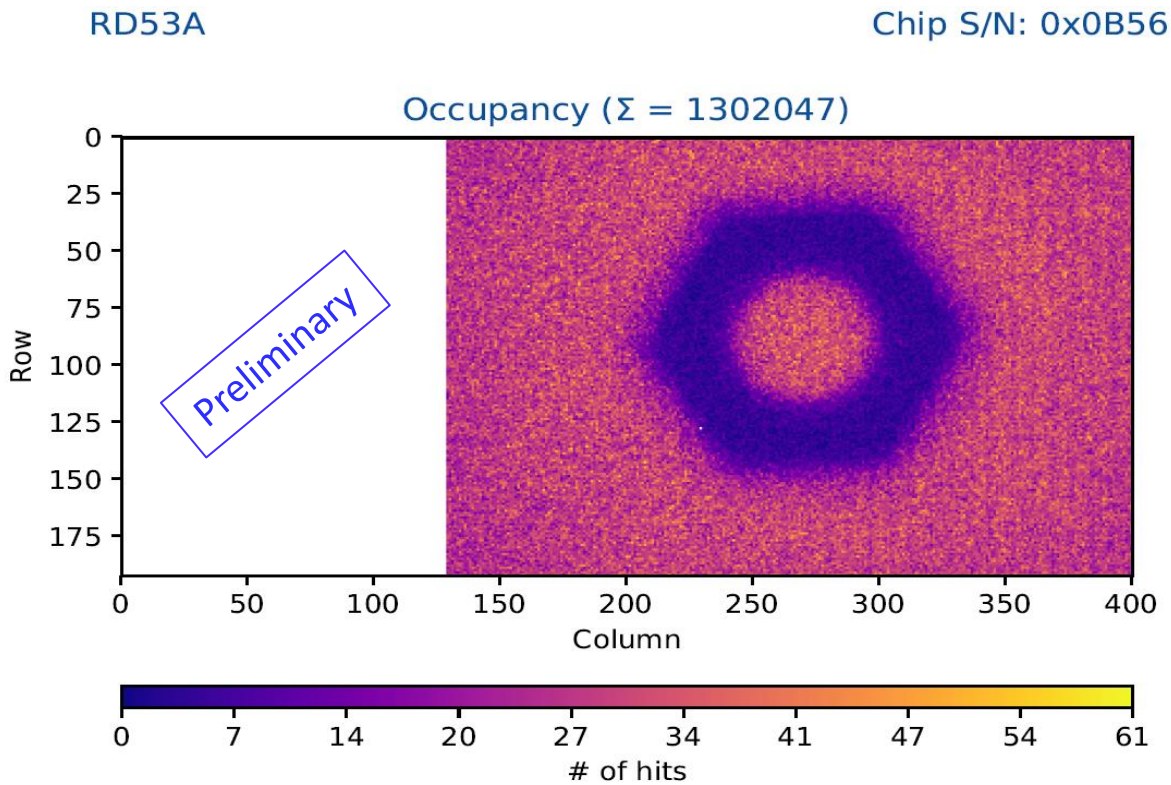






First signs of life of chip assembly

- 4 RD53A chips with sensor arrived in Bonn on 13 April 2018
- Image of a nut placed on the sensor backside, illuminated with Am241 source
- Hit-OR-trigger scan, LIN and DIFF FE, both set to 3 ke threshold, un-tuned
  - Need some more FW/SW development to implement auto-zero sequence for SYNC FE

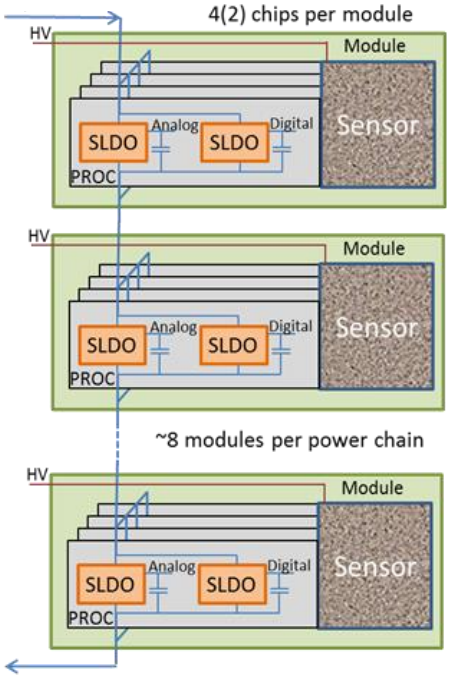


Sensor ID W8S7: 50x50 µm, 150 µm , n-in-p planar (MPP)

ShuntLDO

ShuntLDO

- RD53A is designed to operate with ***Serial Powering*** → constant current to power chips/modules in series (see dedicated talk by S. Orfanelli and poster by D. Koukola)
- Based on **ShuntLDO**
- Dimensioned for production chip

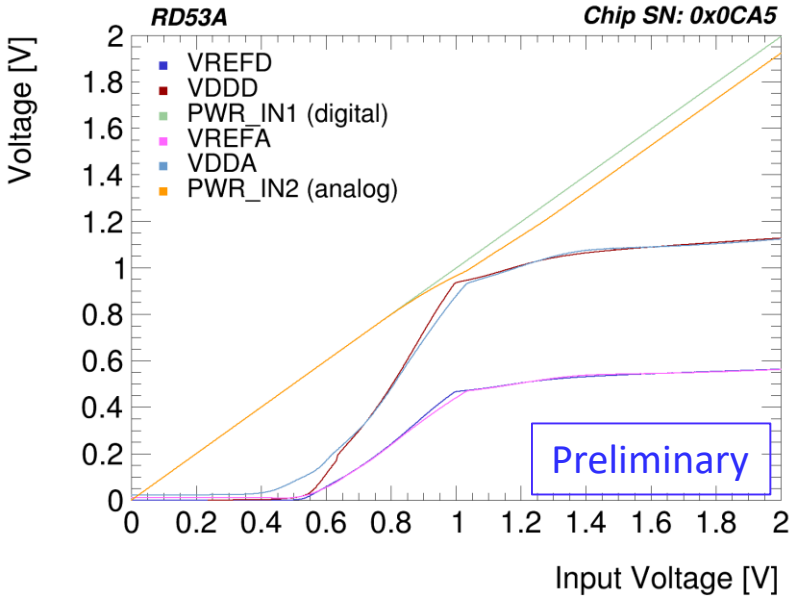


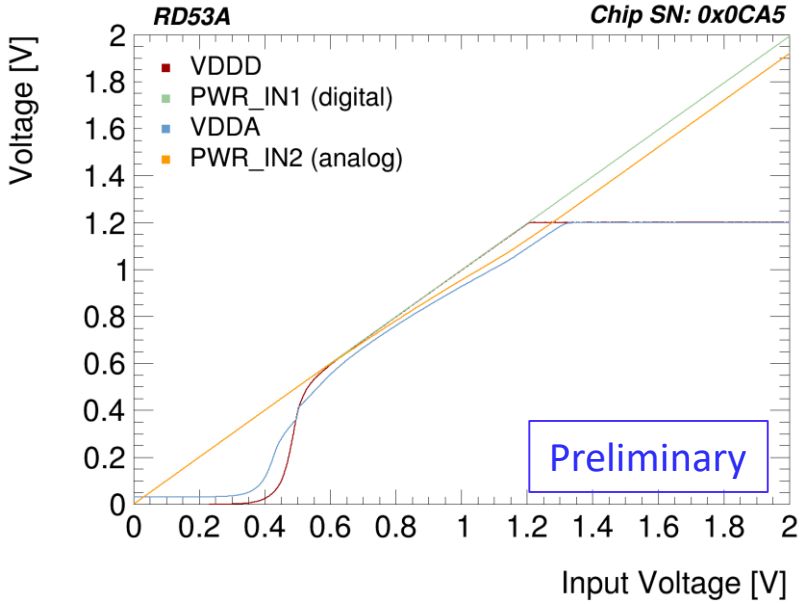
Three operation modes:

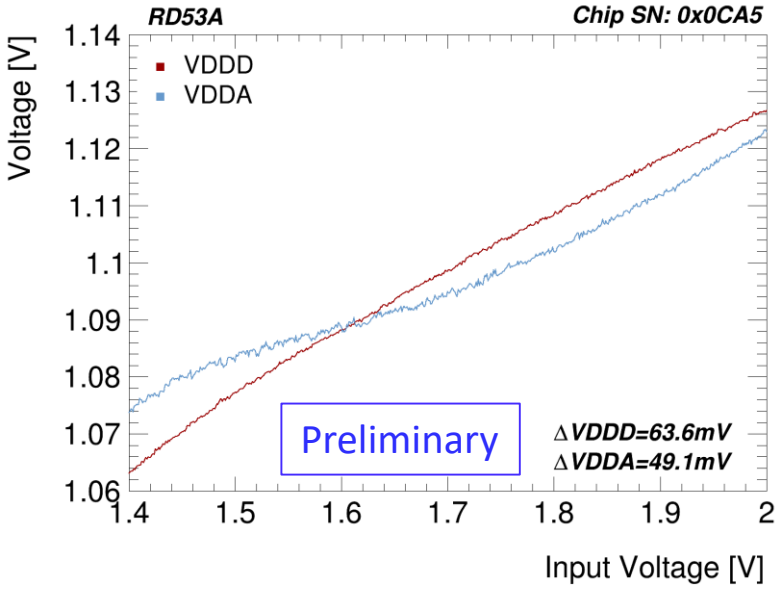
1. ShuntLDO: constant input current Iin → local regulated VDD
2. LDO (Shunt is OFF) : external un-regulated voltage → local regulated VDD
3. External regulated VDD (Shunt-LDO bypassed)

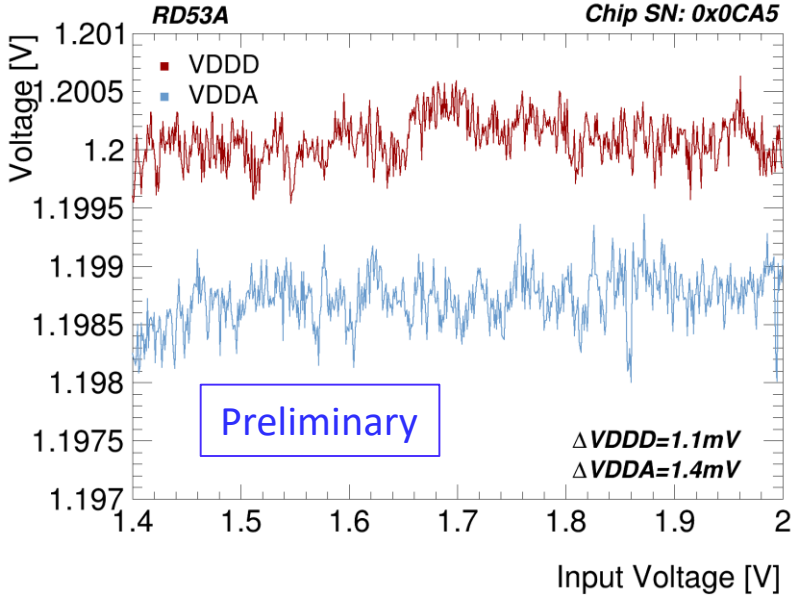
LDO - Line Regulation

(internal Vref from BGR) ⇔ (external Vref = 0.6 V)





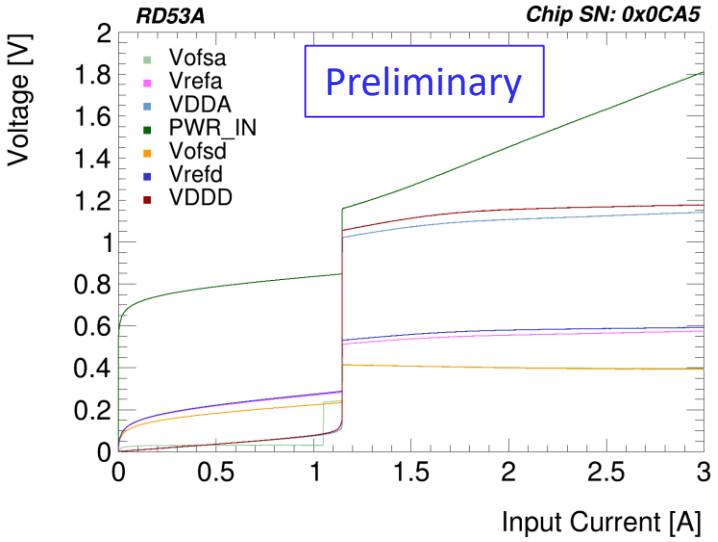


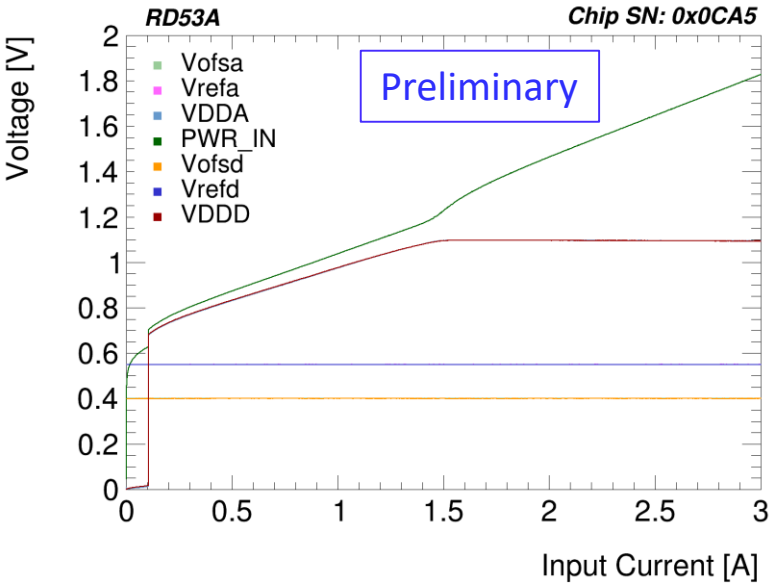


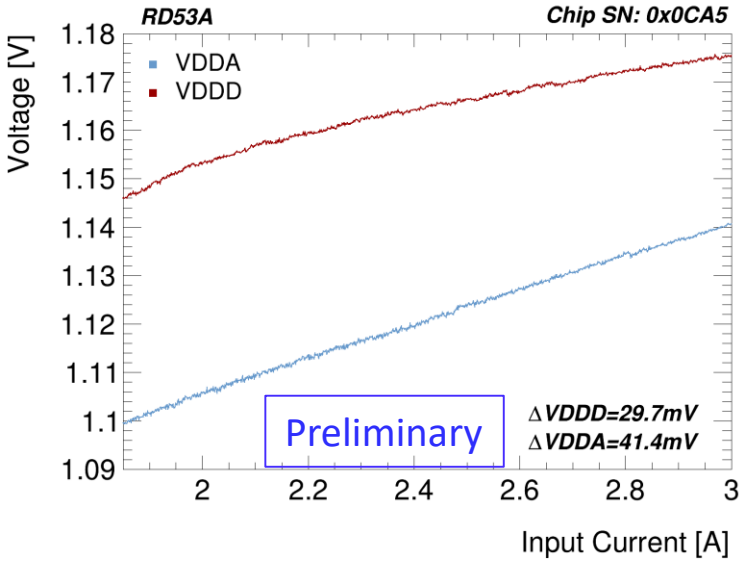
ShuntLDO - Line Regulation (parallel; Rint)

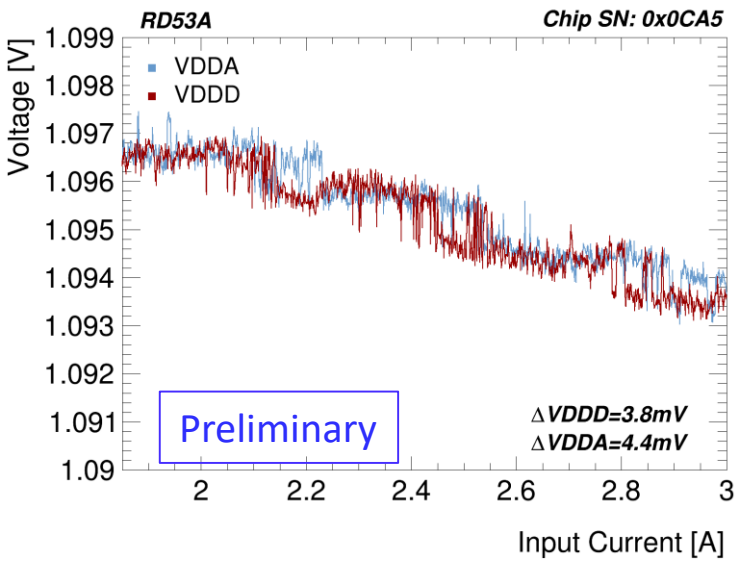
(internal Vref; internal Vofs) ⇔ (external Vref=0.55V; external Vofs=0.4V)

Note: here Vofs means 1/2 of effective ShLDO Voffset









Preliminary conclusions on ShLDO

- **The chip can be operated both in LDO and ShLDO mode**
- Lots of measurements are still on-going
- Line regulation behavior dominated by VREF (Bandgap) as expected by simulations → to be improved
- Load regulation is good
- New prototype submission in summer for:
  - New scheme to improve the line regulation
  - Low-power mode for module testing without cooling
  - Output current limitation
  - Over-voltage protection
  - Improve monitoring capability

RD53B development

RD53B design activity started → production chips

- Design team well defined: **~ 20 designers**
- All RD53A elements with bug fixes and technical improvements
- Small prototype submission in summer for some blocks requiring major changes
- Choice of AFE and digital architecture
- Known features left out of RD53A but needed for prod. Chips:
  - Bias of edge and top “long” pixels
  - Large pixels for outer layers?
  - 6 to 4 bit dual slope TOT mapping
  - 80 MHz TOT counting.
  - Design for test scan chains
  - SEU hardening
  - Serial power regulator updates
  - ATLAS 2-level trigger scheme
  - Optimal data formatting and compression
  - Date aggregation between pixel chips (CMS)
  - Co-simulation/verification with LPGBT
  - Cable driver optimization/verification with final cables
  - …

Conclusions

RD53A is alive and preliminary test results are very promising

- No major problems so far, but some “features” require proper Single Chip Card configuration and firmware/software optimizations
- First X-ray test at CERN done: some promising results but for next irradiation test we need to improve testing routines and setup (powering)
- On the way of defining default “Powering” option and how to operate the 3 different FE (threshold adjustment, calibration etc.)
- Test systems are being prepared and soon provided to institutes to test sensors with RD53A
- First production lot of 25 wafers submitted
- ATLAS/CMS plans to test different pixel sensors types (~10) and variants (2 - 4 for each type) with RD53A in the coming months (https://indico.cern.ch/event/721883/)
- Pixel modules (2x1 and 2x2) being designed with RD53A chip in both ATLAS and CMS pixel communities
- It is planned to integrated RD53A into CMS tracker readout system (FC7 based) after the summer
- Large scale serial powering tests being planned with RD53A based pixel modules