Overview of Outer Tracker ASIC development

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ACES 2018
25th April 2018

Introduction to Outer Trackers

Similarities and differences between ATLAS and CMS

Tracker Layout

ATLAS ITk Strip Detector

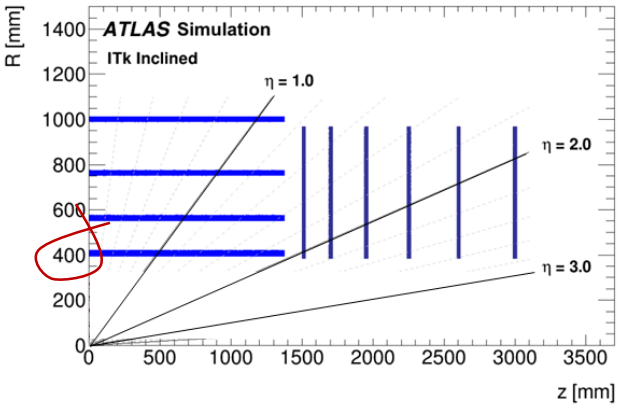
CMS Outer Tracker

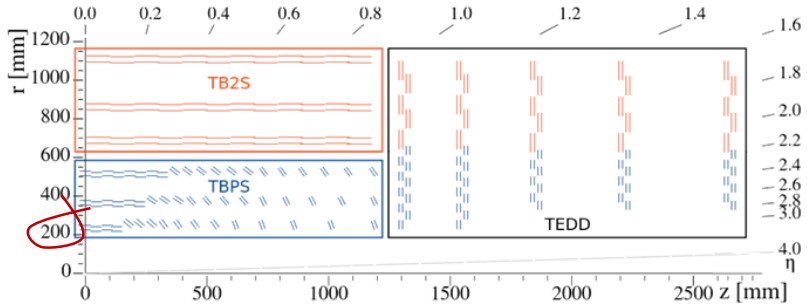
Common requirements for ASICs

Increase Radiation tolerance

Increase granularity

Participate L1 trigger





# of Modules = 17888

# of channels = 59.87 M strips

Silicon Area ~165 m^2

# of Modules = 13296

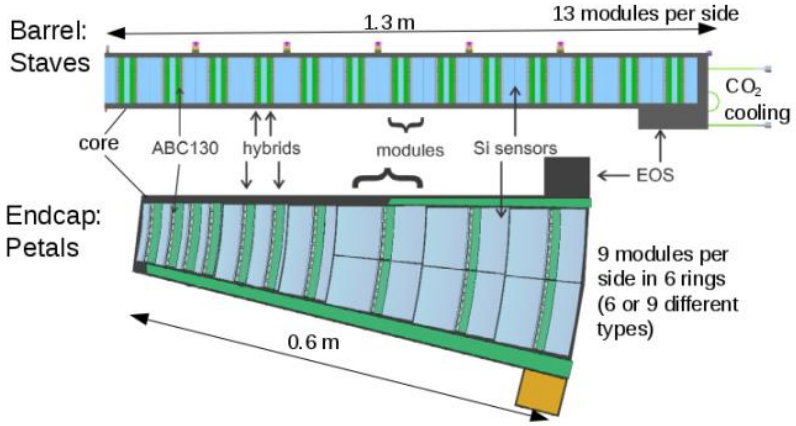
# of channels = 44 M strip + 174 M pixels

Silicon Area ~200 m^2

Modules

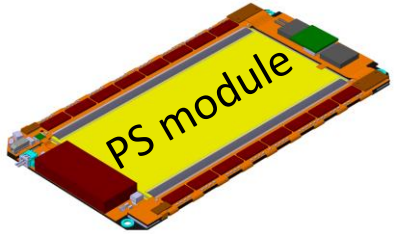
Hybrid and EoS modules

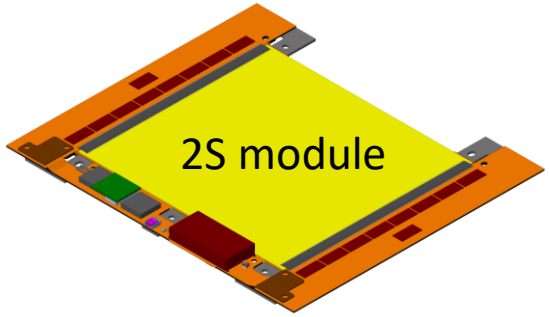
- Basic integration unit: Staves or Petals
- 2x Hybrid modules:
  Long or short strips (5 or 2.5 cm)
- **EoS** module: End of Structure



P_T (2S or PS) hybrid modules

- Basic integration unit: P_T (2S or PS) module
- 2S module: 2x Strip sensors (5 cm)
- PS module: **Pixel**-Strip sensors
  (**1.5 mm for pixel**, 2.5 for strip)





Data readout (1)

Multi-Triggered data flow

- Binary readout
- No continuous readout
- Multi-Triggered data flow
- Synchronous and Async. Triggers
- Zero-suppressed data output
- Electrical readout up to EoS
- Optical readout from EoS based on lpGBT and Versitile link

Stub Finding + Triggered data flow

- Binary readout
- High-p_T (stub) event-driven readout
- Triggered data flow
- Synchronous Triggers
- Zero-suppressed data output
- Electrical readout within modules
- Optical readout from modules based on lpGBT and Versitile link

Data readout (1)

Multi-Triggered data flow

- Binary readout
- No continuous readout
- Multi-
- readout up to EoS
- Optical readout from EoS based on lpGBT and Versitile link

Stub Finding +

- synchronous Triggers
- Zero-suppressed data output
- Electrical readout within modules
- Optical readout from modules based on lpGBT and Versitile link

lpGBT Status and Plans – Tuesday 24 April 2018 – S. Kulis
Versatile Plus Status and Plans – Tuesday 24 April 2018 – F. Vasey

Data readout (2)

Multi-Triggered data flow

- L0 (Level-0 trigger)
  - Synchronous to bunch crossing
  - Select data for readout
  - Global readout ***in single trigger mode***
- ***R3 (regional readout request)***
  - Asynchronous readout request with priority (PR) and low latency
  - Distributed to part of the detector to get tracking data participating to the L1 trigger
- L1 (Level-1 trigger)
  - Asynchronous readout request with low priority (LP)
  - Readout of the complete detector

Triggered data flow

- L1 (Level-1 trigger)
  - Synchronous to bunch crossing
  - Select data for readout
  - Global readout

Event-driven data flow

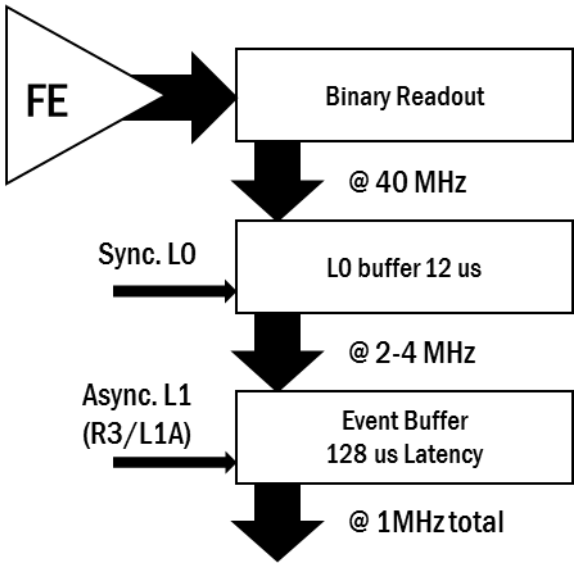
- ***Stub Finding***
  - Synchronous to bunch crossing
  - Continuous readout
  - Quick and on-chip data selection

Participate L1 trigger

Front-End ASICs

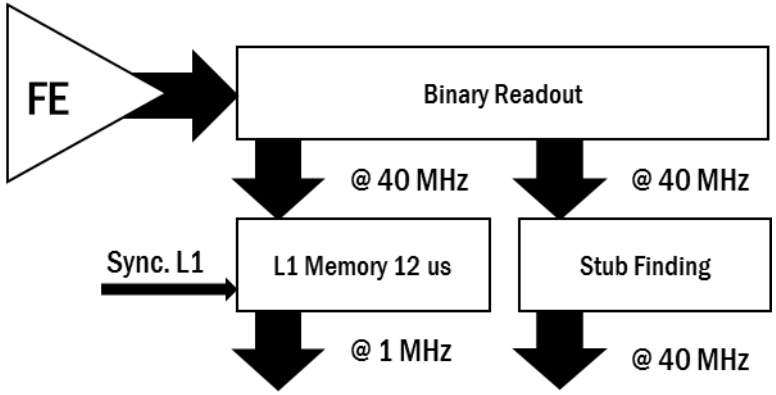
Multi-Triggered data flow

↳ ***+ Storage***



Stub Finding + Triggered data flow

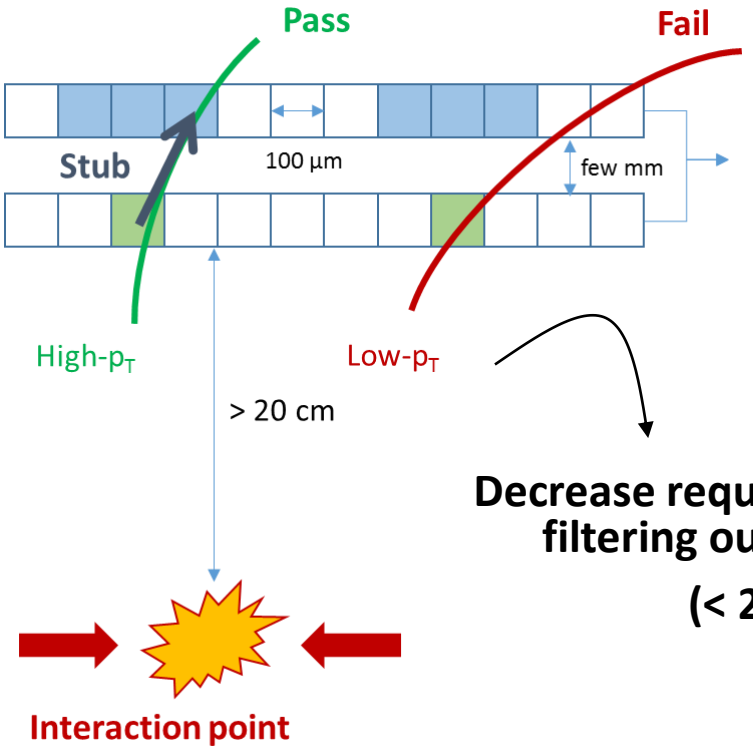
↳ ***+ Digital Signal Processing***



Front-End ASICs

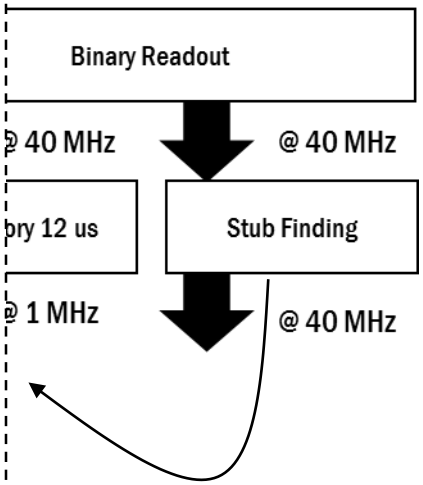
Multi-Triggered data flow

Stub Finding + Triggered data flow



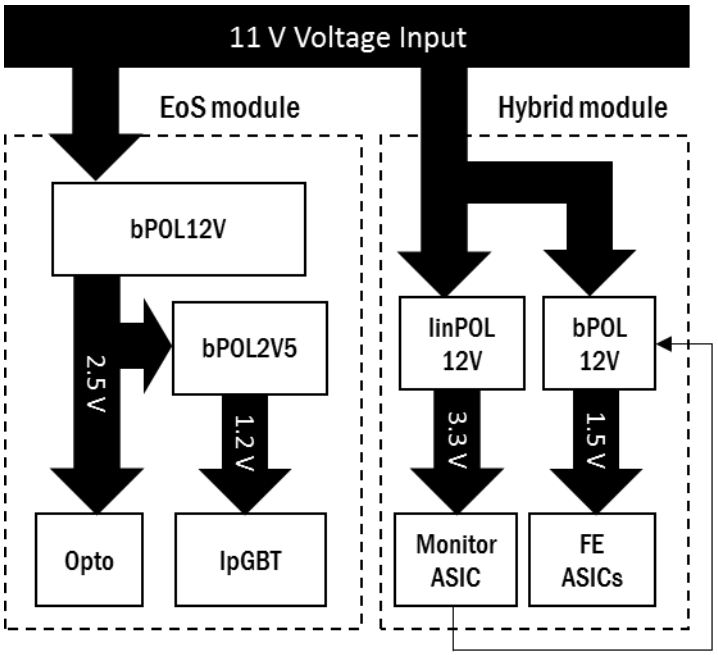
Decrease required bandwidth by filtering out low-pT tracks

(< 2 GeV/c)

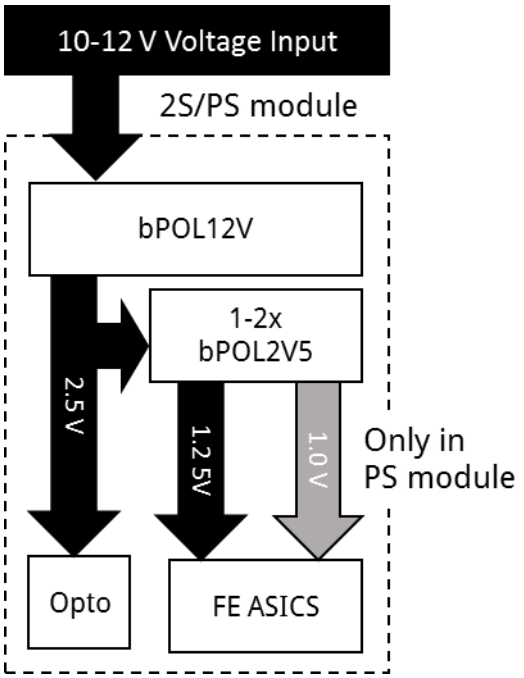


Powering scheme

DC/DC per module + DC/DC per EoS



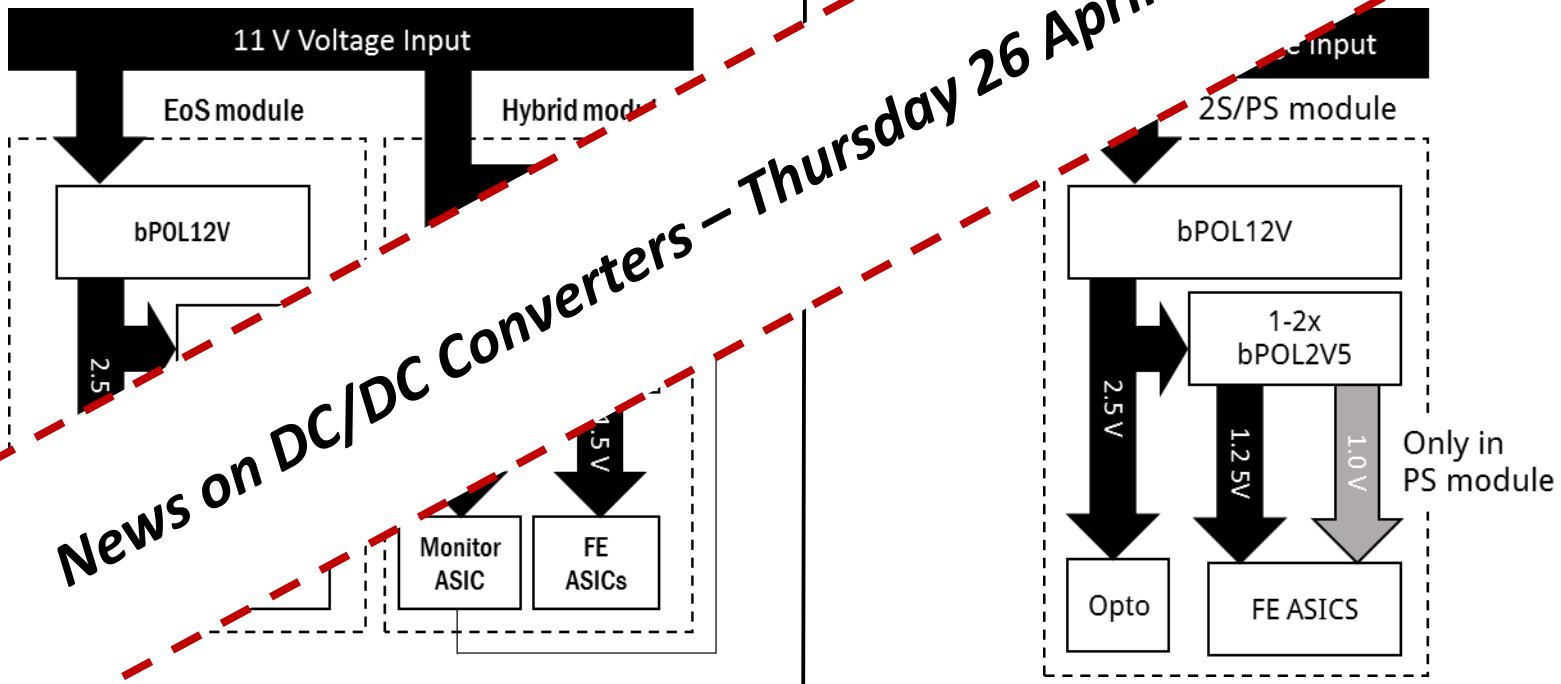
2/3 DC/DC per module



Powering scheme

DC/DC per module + DC/DC per EoS

2/3 [illegible]



News on DC/DC Converters – Thursday 26 April 2018 – F. Faccio

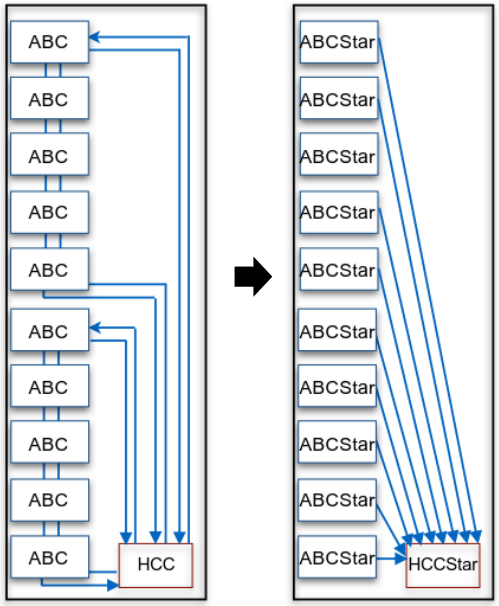
ATLAS ITk Strip Detector ASICs

ABC*, HCC* and AMAC design and results

Dedicated ASIC developments

- ABC: ATLAS binary chip
  - Strips readout ASIC
  - Production chip: ABCStar
  - Prototype: ABC130 (produced and tested)
- HCC: Hybrid Concentrator Chip
  - Interface between ABCStar chips and off-detector
  - Production chip: HCCStar
  - Prototype: HCC130 (produced and tested)
- AMAC: Monitoring & Control (produced and tested)

Reminder:



old new

- Wirebonded ASICs
- 130nm CMOS technology
- Common chip submission foreseen May 2018

Barrel module

ITK-strips
UK & US clusters

Available results from ASIC prototypes integrated in a barrel module

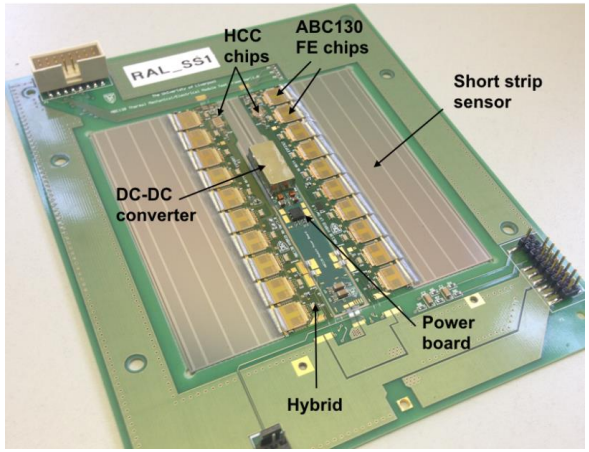


Table 3.1 Layout parameters for the ITk Strip Detector barrel.

Layer	Radius [mm]	Channels in ϕ	Strip Pitch [μm]	Strip Length [mm]
0	405	28×1280	75.5	24.1
1	562	40×1280	75.5	24.1
2	762	56×1280	75.5	48.2
3	1000	72×1280	75.5	48.2

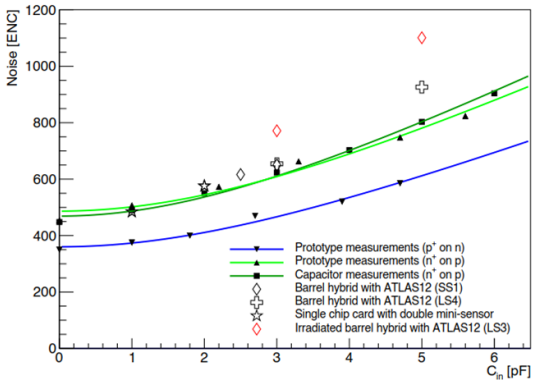


Figure 8.5: Measured noise as a function of input capacitance for a range of prototype devices.

Required Radiation tolerance:
< 35 Mrad (50 Mrad w/ 1.5x safety factor)

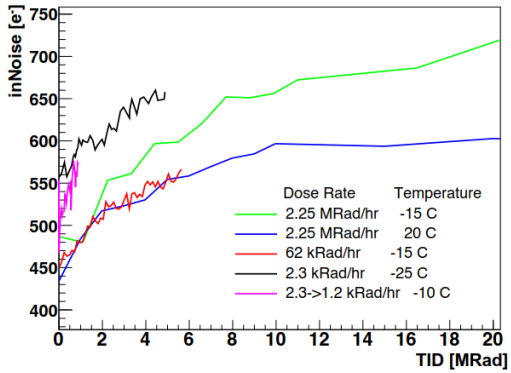


Figure 3.1 Increase of input noise in the ABC130 as a function of TID, for different does rates and temperatures

Results from **TDR for the ATLAS Inner Tracker Strip Detector** [cds.cern.ch/record/2257755]

ABC* Architecture

AGH Krakow
CERN
UCL (UK)
UCSC (Santa Cruz)
IHEP (Beijing)
Penn University
Oxford University

ABC* FE reuse ABC130 FE with improved noise operation with n+-in-p sensors before and after irradiation

Atlas Trigger options

Original trigger scheme:		
1 MHz L0	10% R3	400kHz L1
Single Trigger Scheme:		
1MHz L0		
Low Latency L0 Scheme:		
2-4 MHz L0	< 10% R3	600-800kHz L1

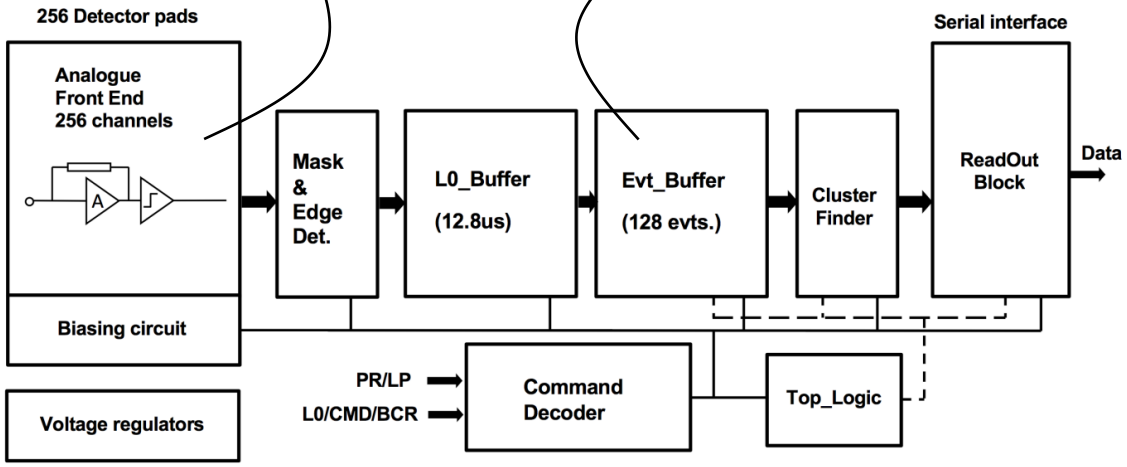


Table 17.1 Front-end power for the short (SS) and long (LS) strip

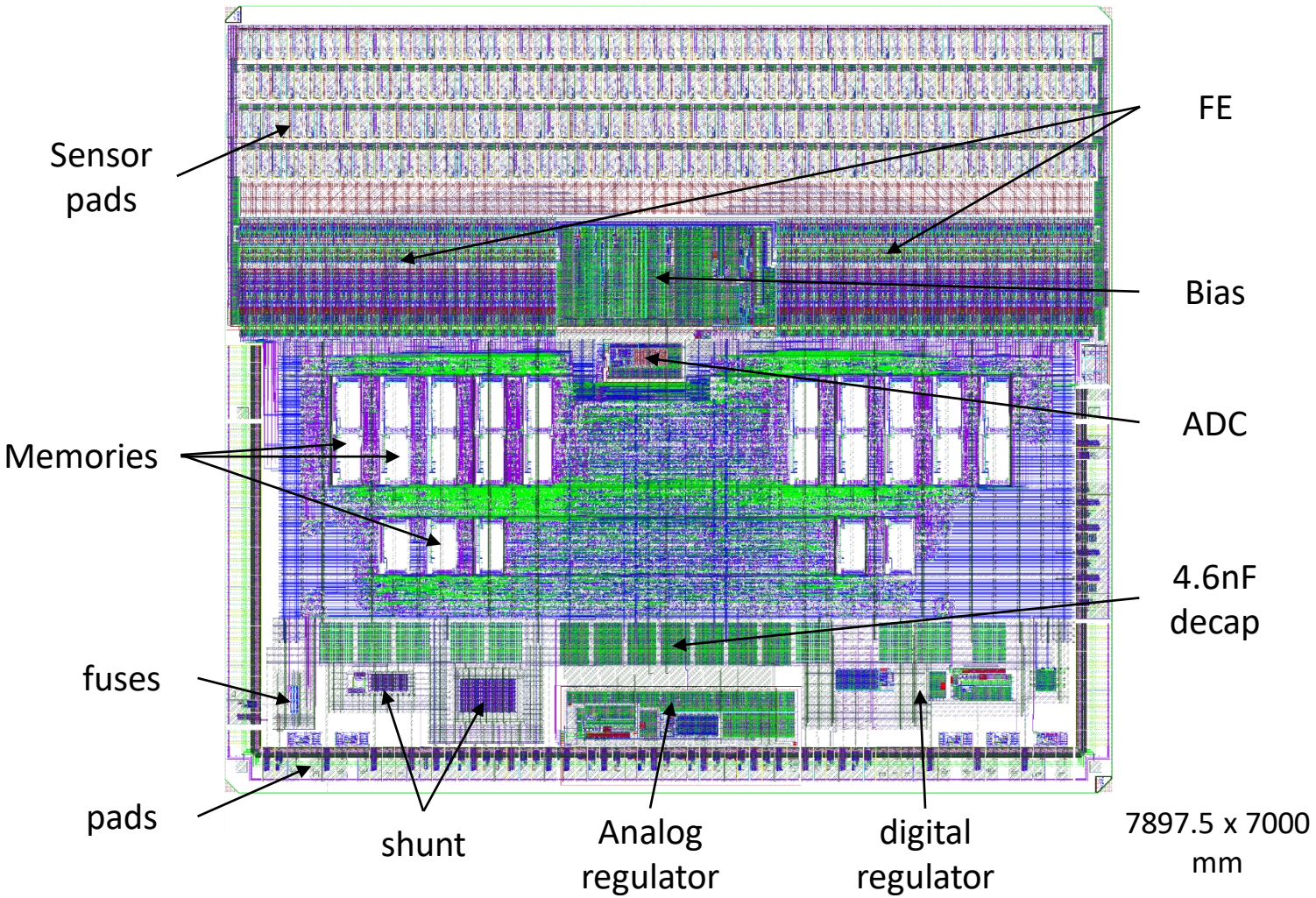
Power [W]	SS	LS
No TID	4.72	2.42
TID	5.64	2.88

Simulated ABC * Power consumption : < 170 mW

Scheme and table from **TDR for the ATLAS Inner Tracker Strip Detector** [cds.cern.ch/record/2257755]

ABC* layout

AGH Krakow
CERN
UCL (UK)
UCSC (Santa Cruz)
IHEP (Beijing)
Penn University
Oxford University

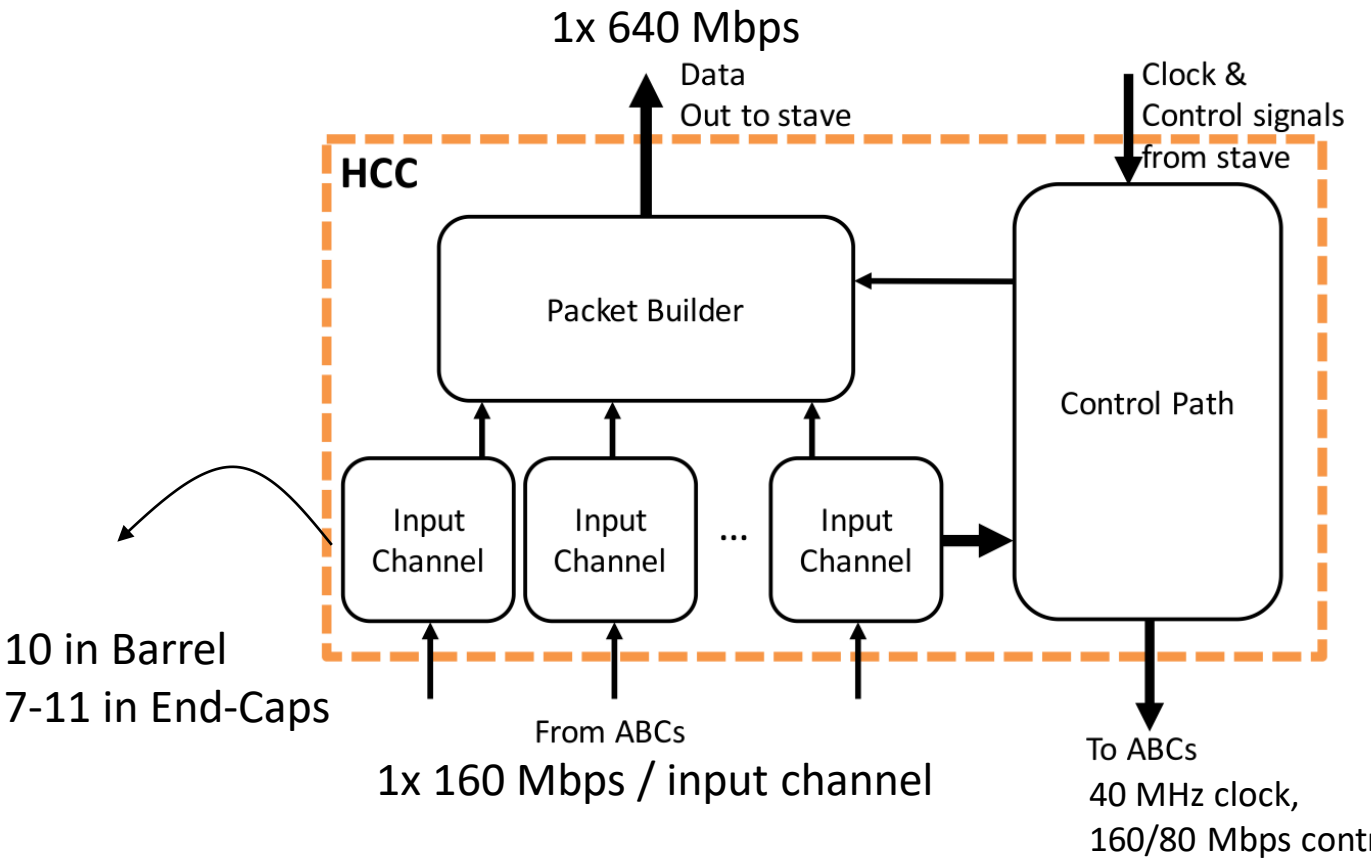


Couretesy of F. Anghinolfi and P. Leitao

Hybrid Concentrator Chip - HCC*

Penn University
UCL
CERN

The Hybrid Controller Chip (HCC) is the interface ASIC between the signalling on the stave and the analogue front-end ASICs (the ABCs) on the hybrid.



Data reduction factor: 1.75 - 3

Scheme from **TDR for the ATLAS Inner Tracker Strip Detector** [cds.cern.ch/record/2257755]

Design Verification

Single ABC* verification framework based on SystemVerilog

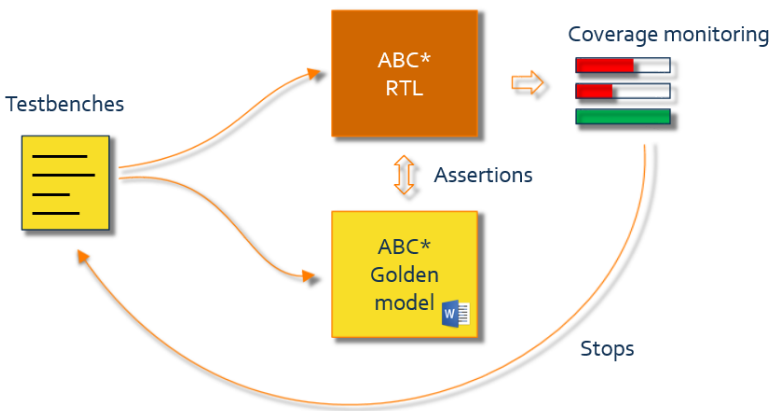


Figure by Hervé Grabas, UCSC

Module-level verification based on **CoCotb**
COroutine based *COsimulation TestBench* environment for verifying VHDL/Verilog RTL using Python.

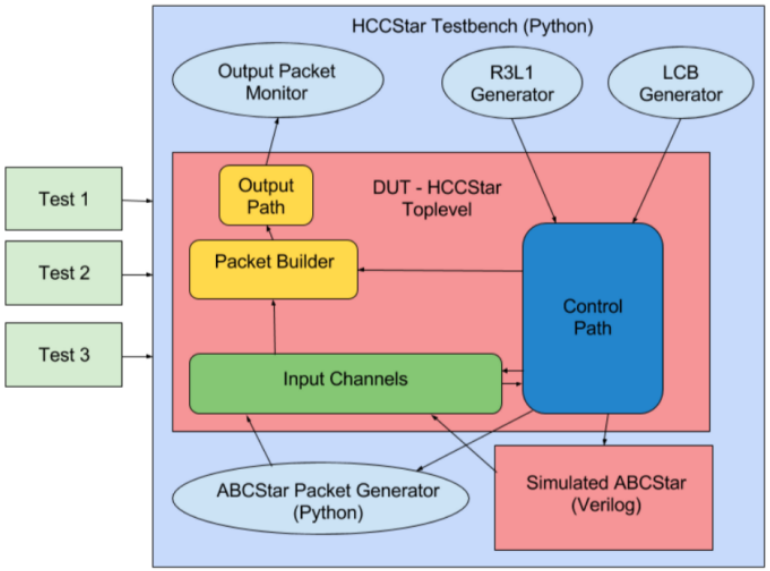


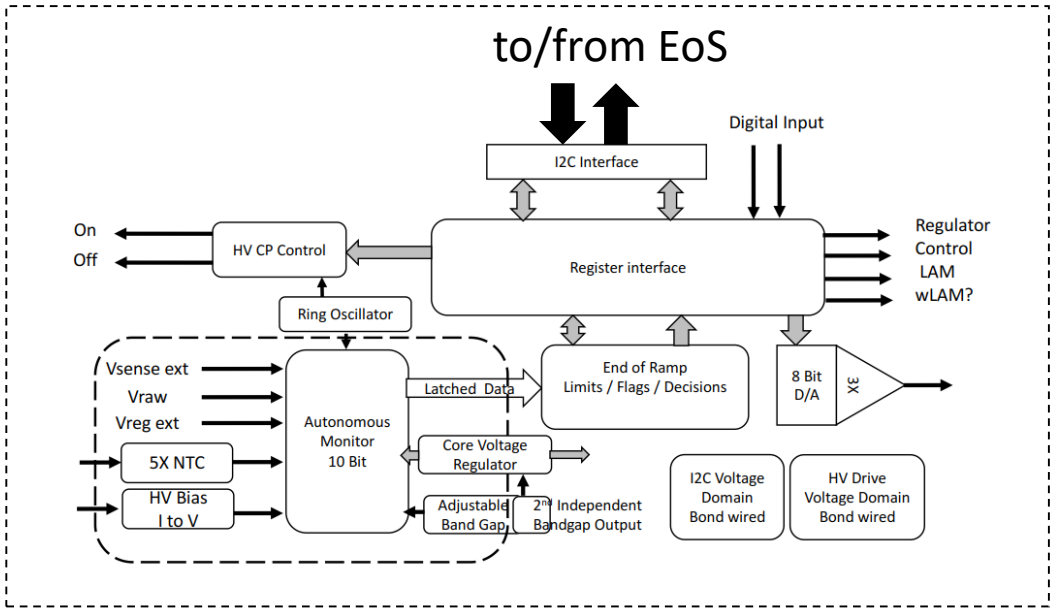
Figure by Jeff Dandoy, Penn University

Autonomous Monitor & Control Chip AMAC

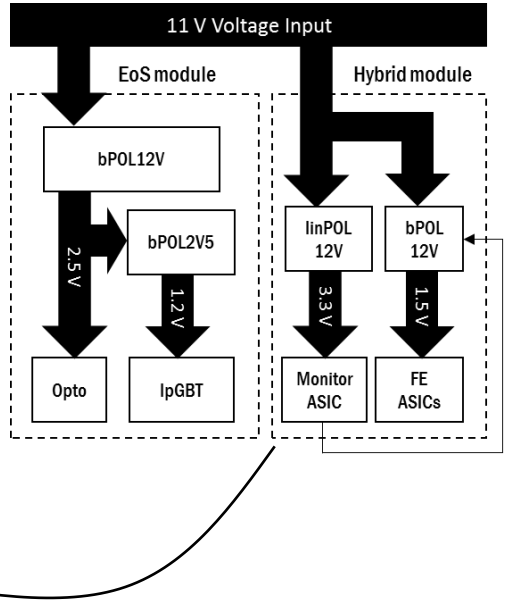
Penn University

Monitoring the temperature and voltage, controlling the HV switch and powering of the hybrids.

AMAC



Powering scheme reminder



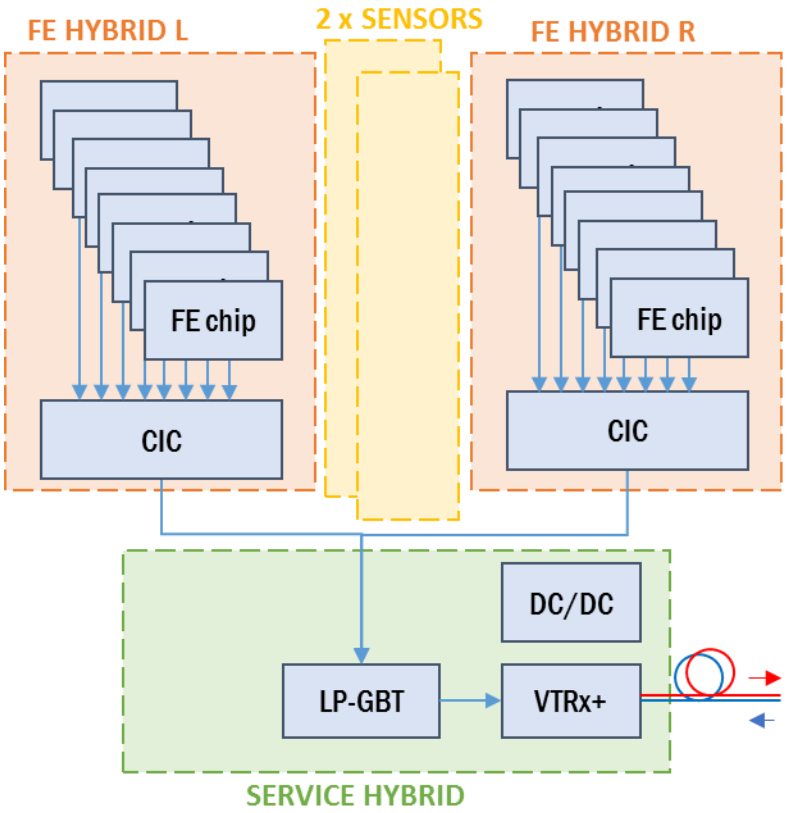
Scheme from **TDR for the ATLAS Inner Tracker Strip Detector** [cds.cern.ch/record/2257755]

CMS Outer Tracker ASICs

CBC, MPA, SSA and CIC designs and results

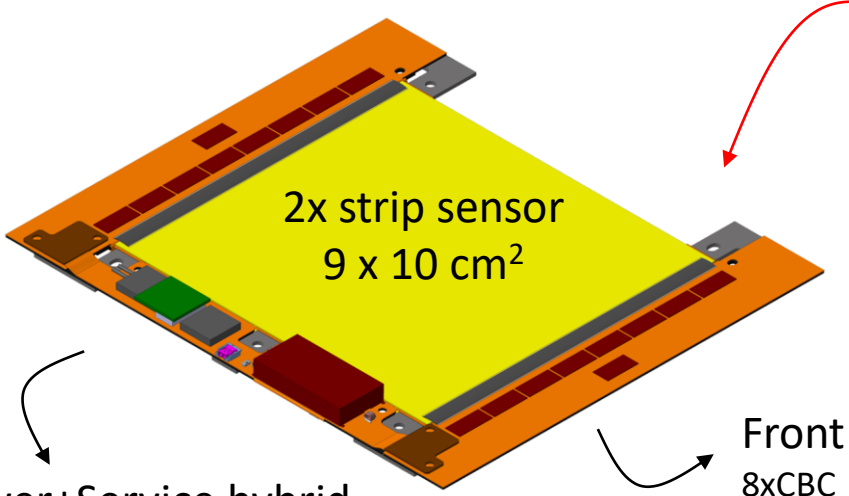
Dedicated ASIC developments

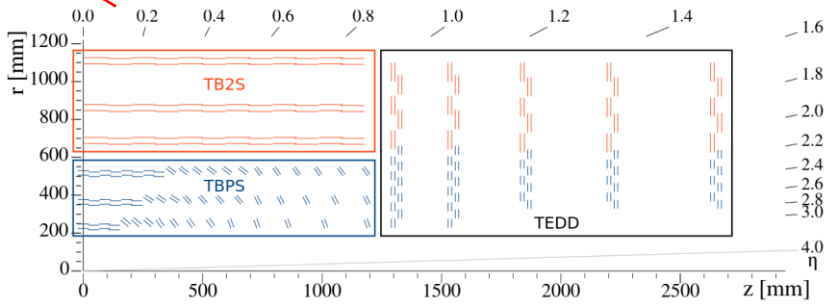
- FE ASICs: Converts sensor signal to binary hit information
  - CBC (*IC, RAL*): Strips readout 2S module
  - SSA (*CERN*): Strips readout PS module
  - MPA (*CERN*): Pixel readout PS module
- CIC - Concentrator IC (*INPL*)
  - Interface FE chips with off-detector
- Technology
  - 130 nm CMOS technology for CBC
  - 65 nm CMOS technology for the SSA, MPA and CIC



P_T module - 2 x Strip - 2S

< Z Resolution
< TID (9 Mrad)
< Power consumption



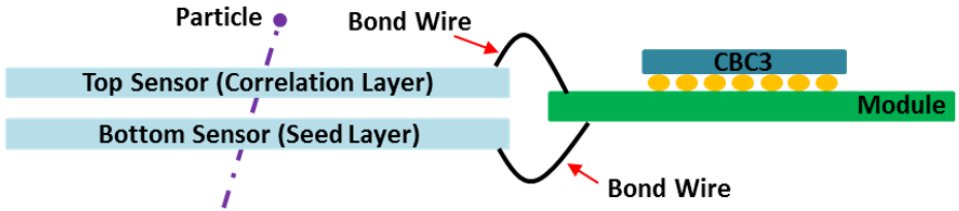


Power+Service hybrid

DC/DC
LpGBT
VTRX+

Front End hybrid

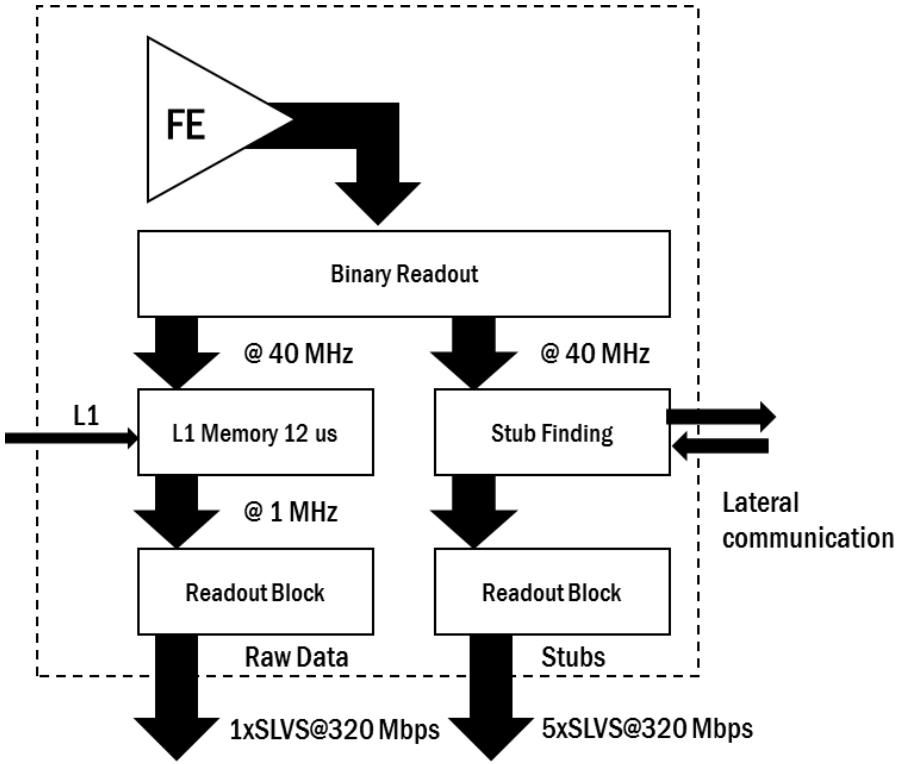
8xCBC
CIC

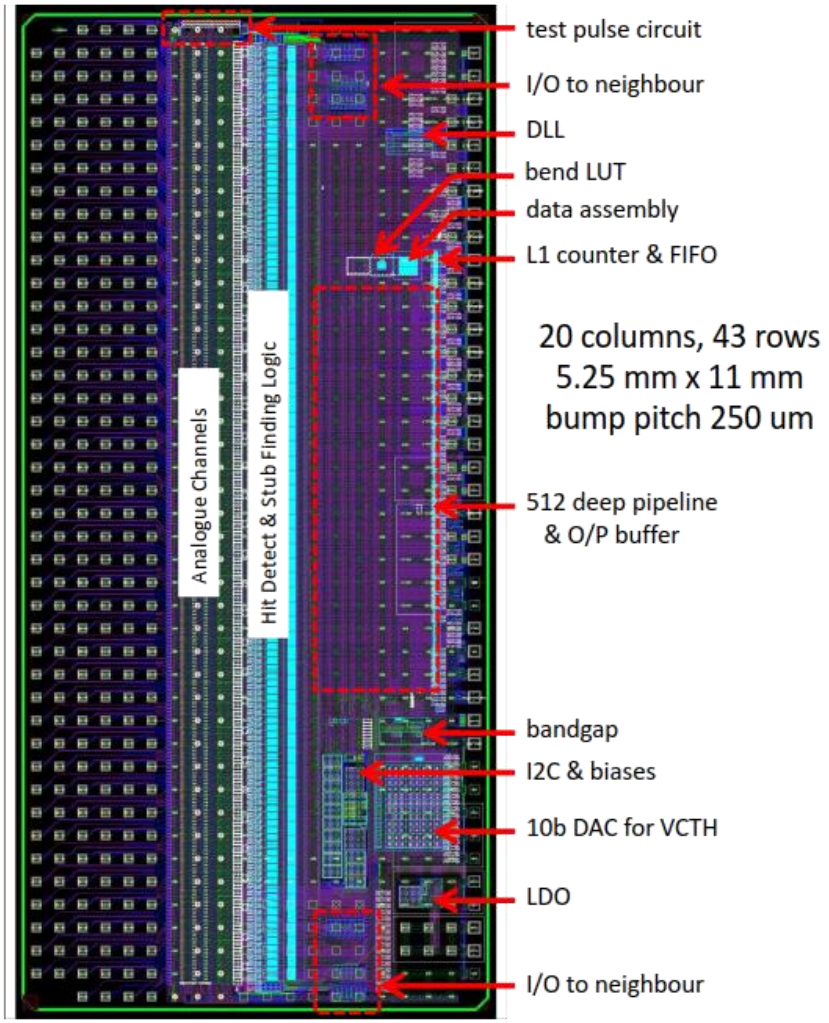


2S module
$\sim 2 \times 90$ cm^2 active area
2×1016 strips: ~ 5 cm $\times 90$ μm
2×1016 strips: ~ 5 cm $\times 90$ μm
Front-end power ~ 5 W
Sensor power ($-20\,^\circ$C) ~ 1.0 W

Table 3.1 from **The Phase-2 Upgrade of the CMS Tracker** [cds.cern.ch/record/2272264]

CBC3 architecture and layout





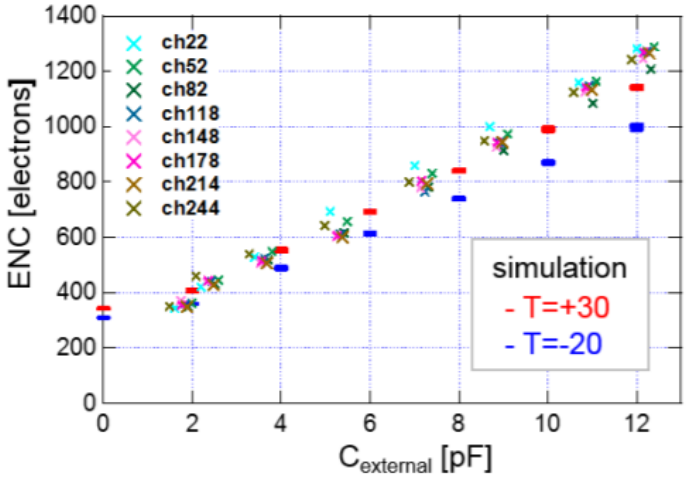
Layout from **CBC3 manual** [http://www.hep.ph.ic.ac.uk/ASIC/]

CBC3 results and plans

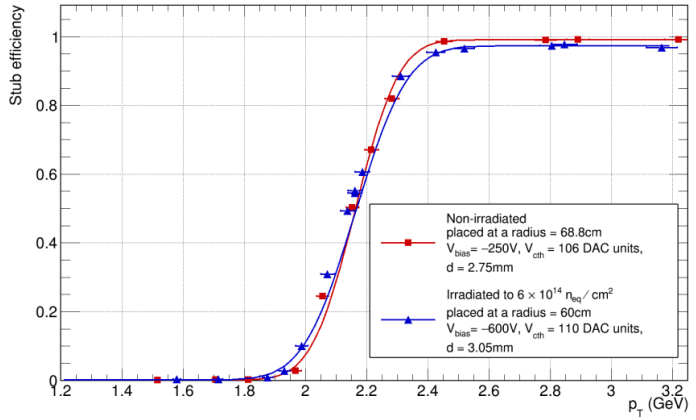
- CBC3 functional and analog testing completed
- Wafer probing carried out
- Irradiation test carried out
- CBC3.1 Production design submitted in Feb. 2018

Measured CBC3 Power consumption : < 140 mW

ENC vs external capacitance



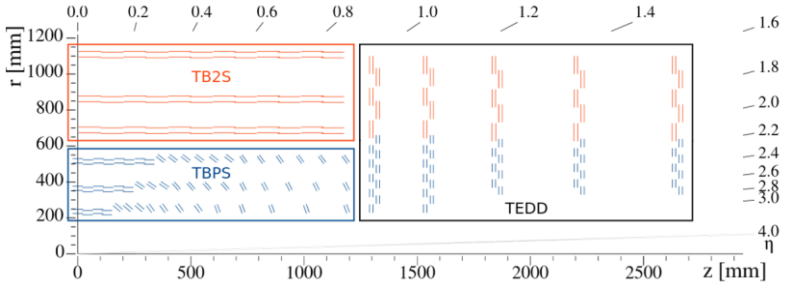
Stub Reconstruction efficiency 2S-mini module.



Results from **The CBC3 readout ASIC for CMS 2S-modules** [cds.cern.ch/record/2312215/]

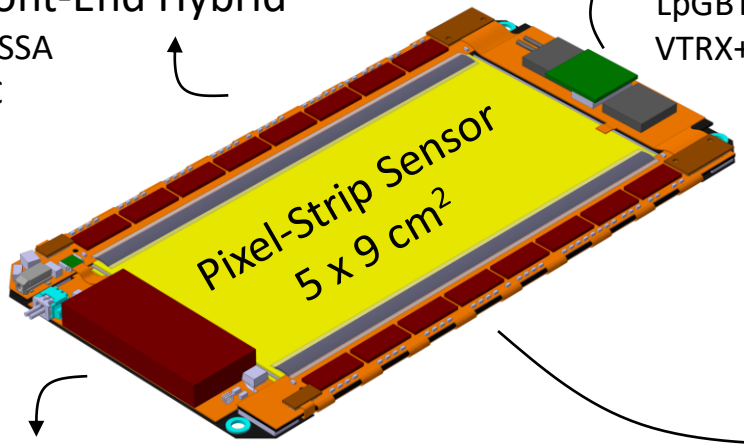
P_T module – Pixel-Strip - PS

> Z Resolution
> TID (56 Mrad)
> Power consumption



Front-End Hybrid
8x SSA
CIC

Service Hybrid
LpGBT
VTRX+

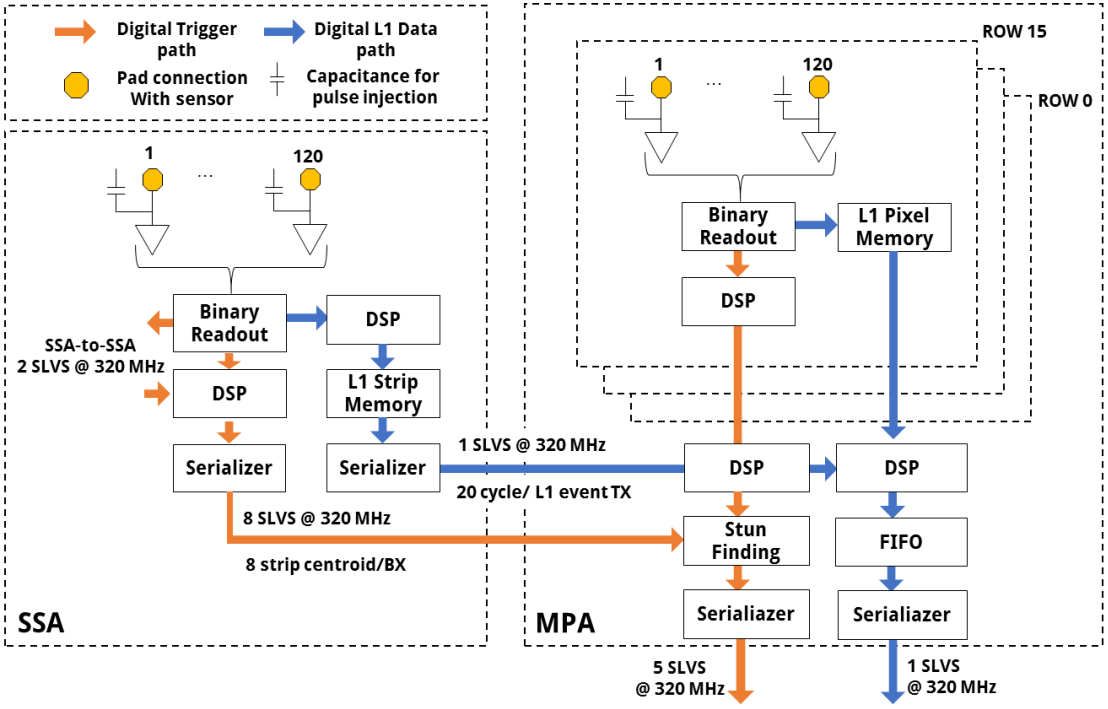


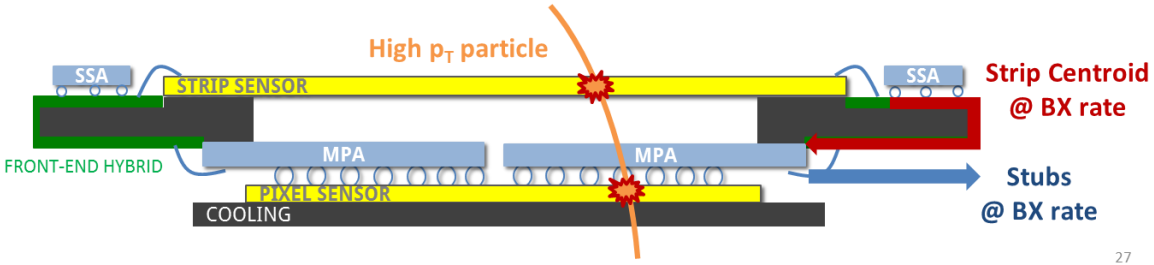
Power Hybrid
DC/DC

Table 3.1 from **The Phase-2 Upgrade of the CMS Tracker** [cds.cern.ch/record/2272264]

PS module
$\sim 2 \times 45$ cm^2 active area
2×960 strips: ~ 2.4 cm $\times$ 100 μm
32×960 macro-pixels: ~ 1.5 mm $\times$ 100 μm
Front-end power ~ 8 W
Sensor power ($-20\,^\circ$C) ~ 1.4 W

SSA-MPA architecture

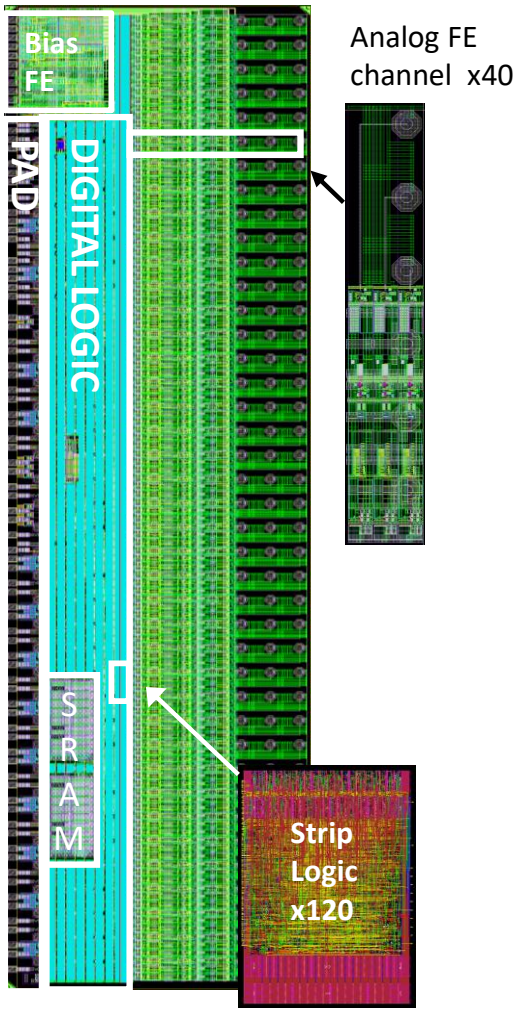


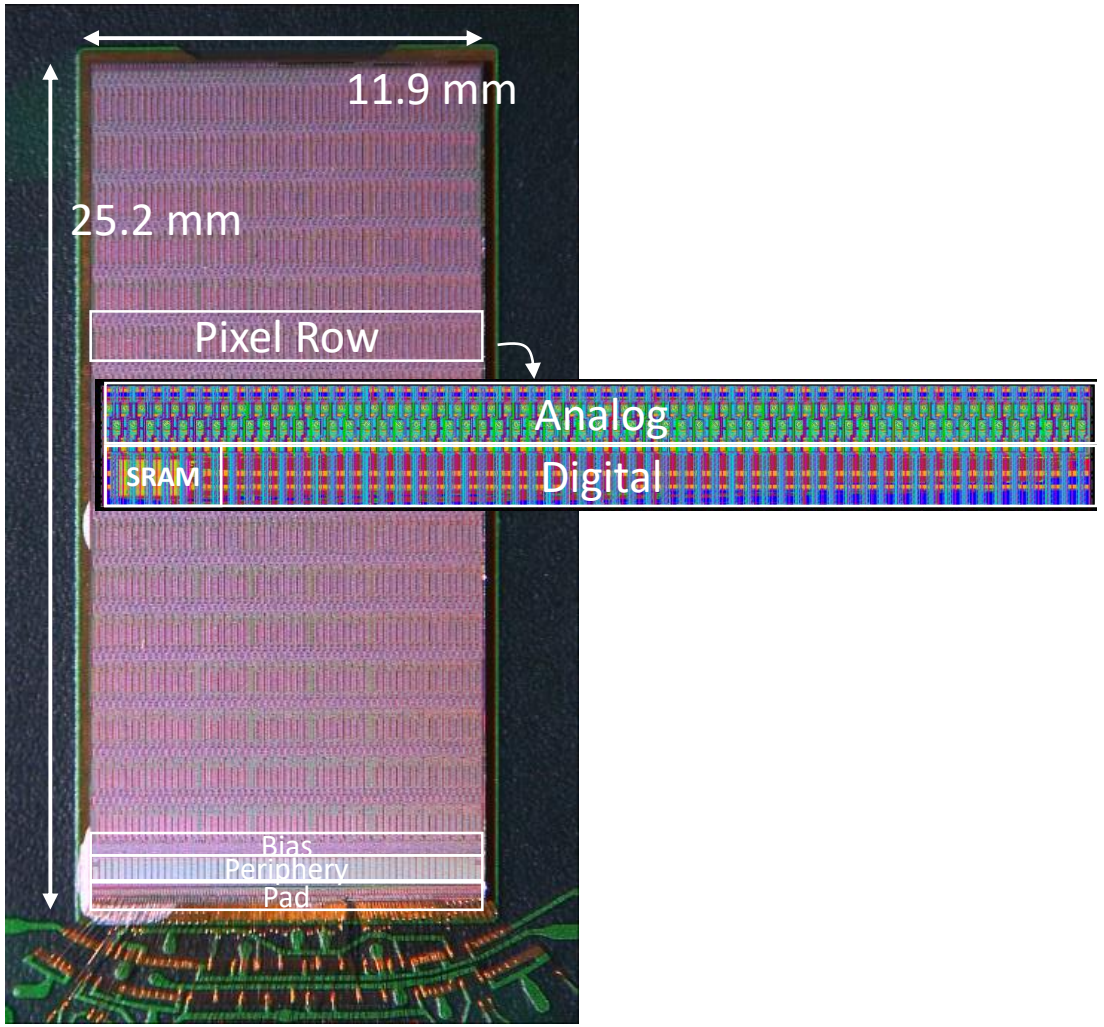


Simulated MPA+SSA power consumption : < 250 mW

Low power technique:
Low Digital supply
Clock gating
Memory gating
MultiV$_T$ Design

SSA - MPA floorplan

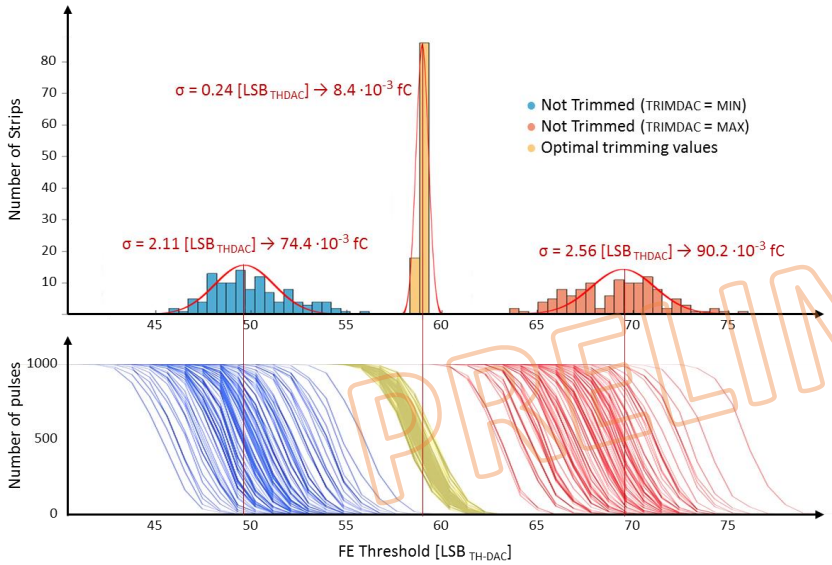




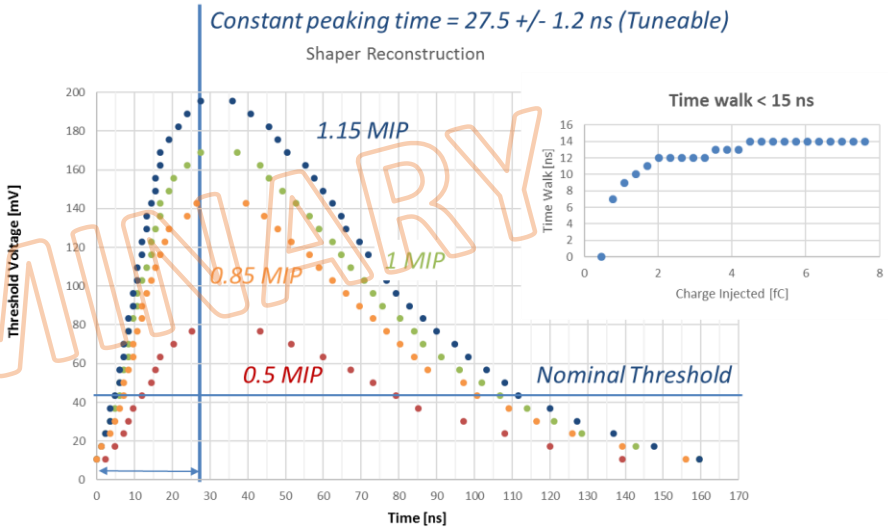
MPA/SSA **preliminary** results

- First full size prototype submitted in Sept. 2017
- Testing started end of Jan. 2018
- Basic functionalities verified
- On-going wafer probing, temperature test, radiation test
- Full-qualification expected in the coming months

SSA S-Curves Trimming procedure for 1 fC injected charge.



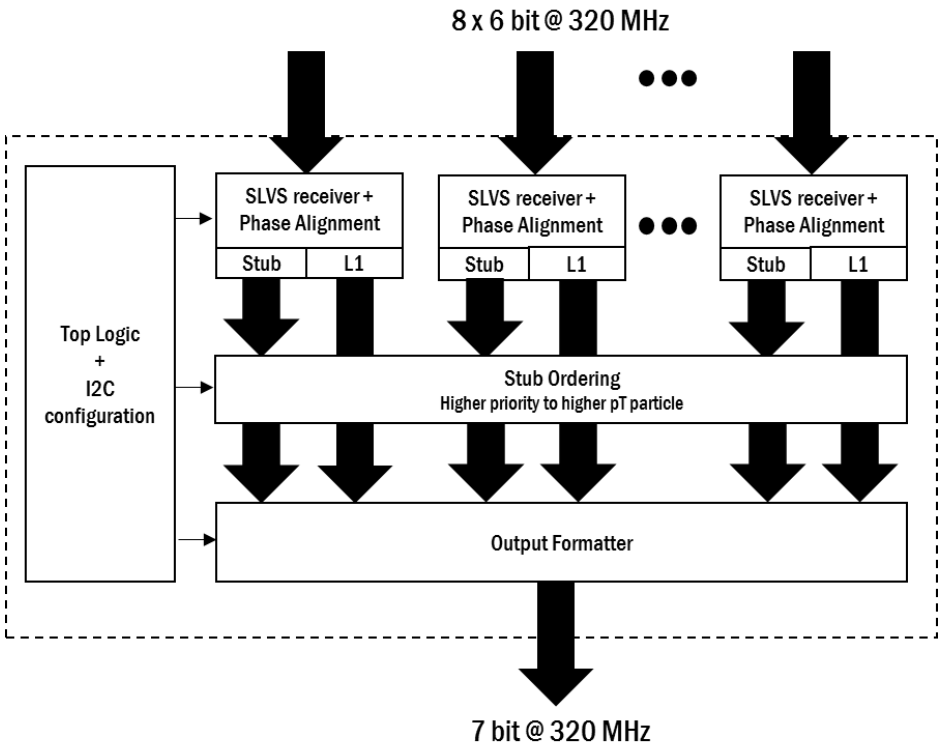
MPA Shaper and Timewalk measurement.



Concentrator IC

The Concentrator IC (CIC) is the interface ASIC between the FE ASICs on the modules and the LpGBT

Data reduction factor: 6.8



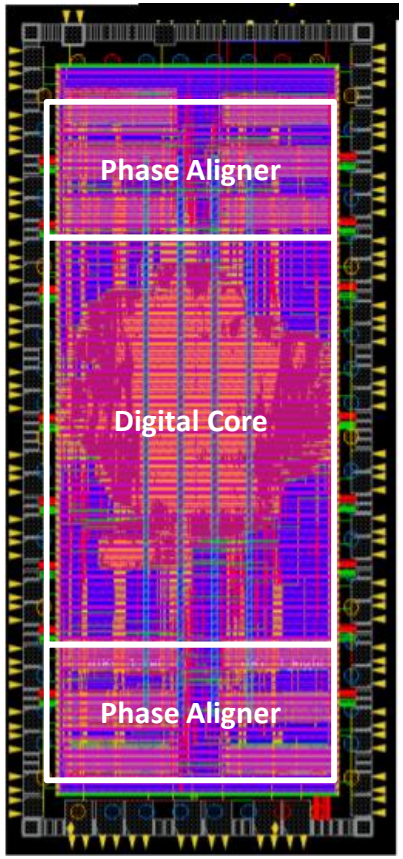


Figure by S. Viret, INPL

Module Level verification

A Verification framework based on the UVM allows single-chip and module verification
(UVM = Universal Verification Methodology for functional verification using SystemVerilog)

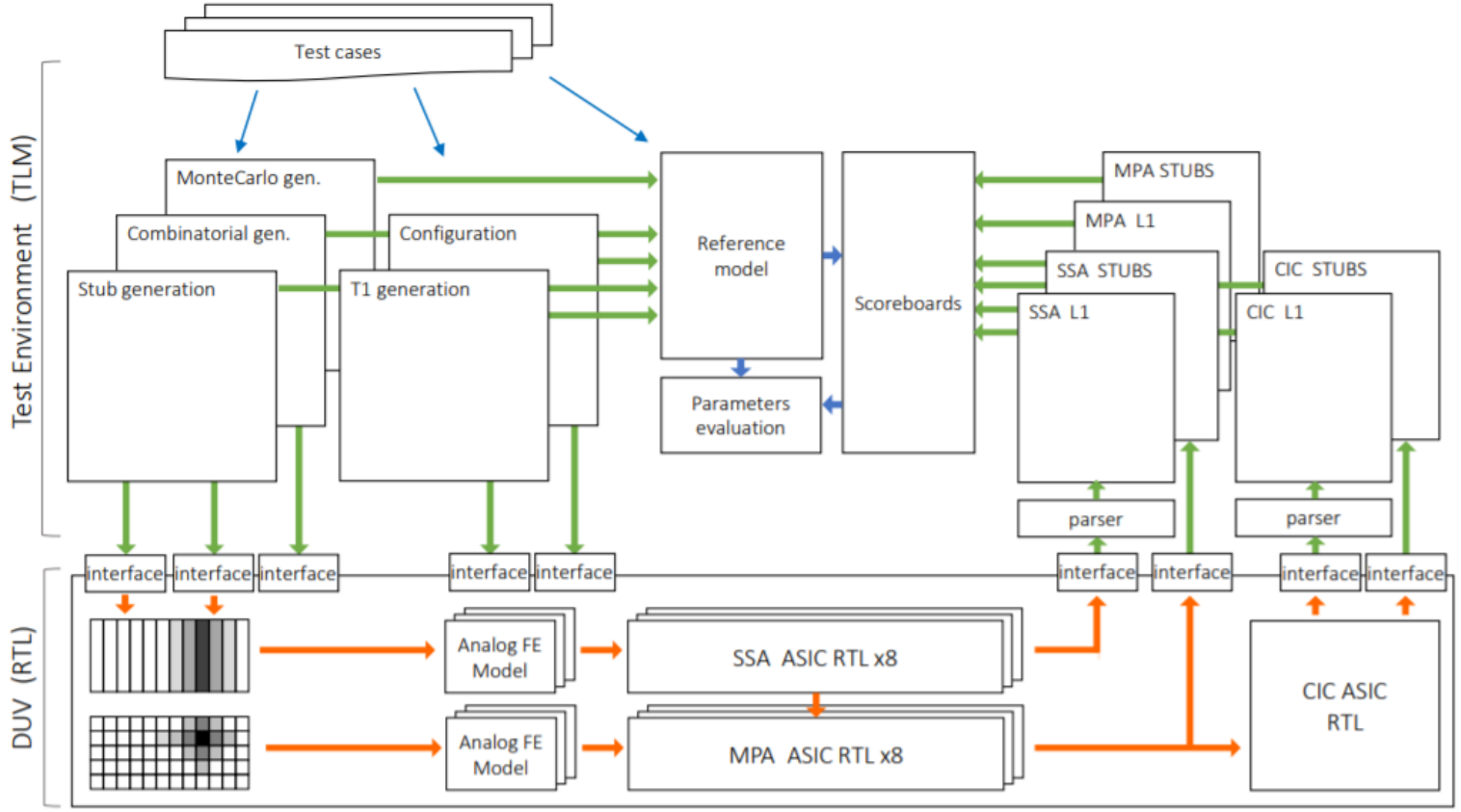


Figure by A. Caratelli, CERN

Summary

ATLAS ITk Strip Detector

- LpGBT & VL+ based readout
- DC/DC converter powering
- Binary Readout
- No continuous readout
- Multi-Triggered Flow
- Only Strip sensor
- Wirebonded bare dies
- 130nm CMOS technology

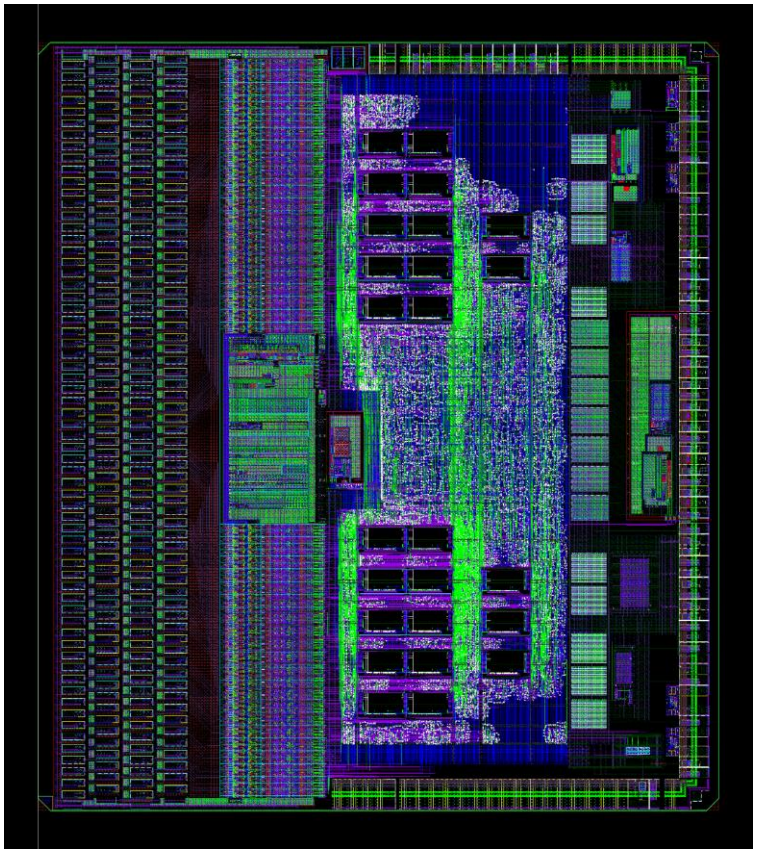
CMS Outer Tracker

- LpGBT & VL+ based readout
- DC/DC converter powering
- Binary Readout
- Stub continuous readout
- Single Triggered Flow
- Combine Pixel/Strip sensor
- Combine bump/wire bonding
- 65/130 nm CMOS technology

Spare slides

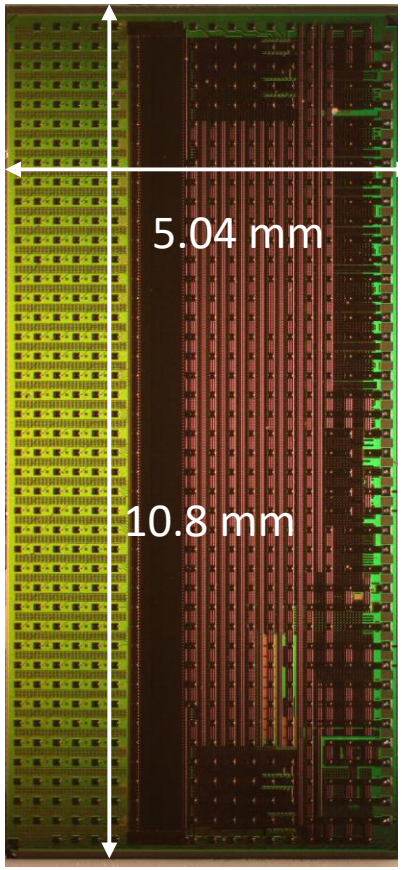
ATLAS Binary Chip - ABC*

Strip Number	256 strips
Strip Size Barrel	75.5 um x 19-60.1 mm
Strip Size End-Cap	69-84 um x 19-60.1 mm
Acquisition Type	Continuous @ BX rate (40 MHz)
Occupancy	< 1%
Readout types	1) Multi-triggered
Acquisition Mode	Binary readout
L0-Trigger latency	< 12.8 us
L0-Trigger rate	2-4 MHz Synchronous
L1-Trigger latency	< 128 us
L1-Trigger rate	1 MHz (R3+L1)
Output data types	1) Strip cluster
Data storage	Strip frame for L0 Latency (~256 x 512w)
Output data port	1 x Custom-sLVS @ 160 Mbps
Power budget	~170 mW
Radiation Tolerance	< 35 Mrad (50 Mrad w/ 1.5x safety factor)
Technology	130 nm GF



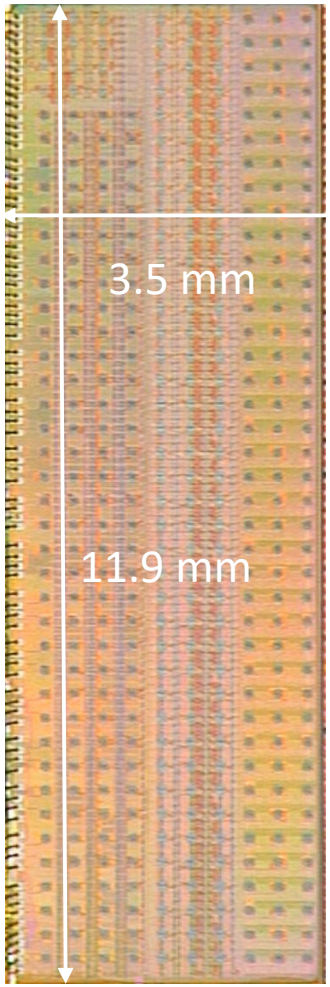
CBC3 specifications

Strip Number Arrangement	254 strip (on two layers)
Strip Size	90 um x 5 cm
Sensor Area	10 cm x 10 cm (16 x CBC)
Acquisition Type	Continuous @ BX rate (40 MHz)
Occupancy	< 1%
Readout types	1) Triggered for full frame (L1-Trigger) 2) Continuous for high-pT information
Acquisition Mode	Binary readout
L1-Trigger latency	< 12.8 us
L1-Trigger rate	<750 kHz
Output data types	1) Raw strip image 2) Stubs
Trigger data storage	Strip frame for L1 Latency (~254 x 512w)
Output data port	6 x Custom-sLVS @ 320 Mbps = 2.88 Gbps
Power budget	~ 120 mW
Radiation Tolerance	9 Mrad (No safety factor)
Technology	130 nm



Short Strip ASIC

Strip Number Arrangement	120 strip
Strip Size	100 um x 2.5 cm
Sensor Area	5 cm x 10 cm (16 x SSA)
Acquisition Type	Continuous @ BX rate (40 MHz)
Hit Rate (Pixel hit Occupancy)	53 MHz / cm^2
Readout types	1) Triggered for full frame (L1-Trigger) 2) Continuous for high-pT information
Acquisition Mode	Binary readout
L1-Trigger latency	< 12.8 us
L1-Trigger rate	<750 kHz
Output data types	1) Raw strip image 2) Strip cluster
Trigger data storage	Strip frame for L1 Latency (~128 x 512w)
Output data port	9 x Custom-sLVS @ 320 Mbps = 2.88 Gbps
Power budget	< 90 mW/cm^2
Radiation Tolerance	56 Mrad (No safety factor)
Technology	65 nm with 1p7m (4x1z1u + RDL)



Macro Pixel ASIC

Pixel Arrangement	118 x 16 = 1888 pixels
Macro Pixel Size	100 um x 1446 um
Sensor Area	5 cm x 10 cm (16 x MPA)
Acquisition Type	Continuous @ BX rate (40 MHz)
Hit Rate (Pixel hit Occupancy)	53 MHz / cm^2
Readout types	1) Triggered for full frame (L1-Trigger) 2) Continuous for high-pT information
Acquisition Mode	Binary readout
L1-Trigger latency	< 12.8 us
L1-Trigger rate	<750 kHz
Input data types	1) Raw strip data 2) Strip clusters
Output data types	1) Pixel and strip clusters 2) Stubs
Trigger data storage	Pixel frame for L1 Latency (~2048b x 512w)
Input data port	9 x Custom-sLVS @ 320 Mbps = 2.88 Gbps
Output data port	6 x Custom-sLVS @ 320 Mbps = 1.92 Gbps
Power budget	< 90 mW/cm^2
Radiation Tolerance	56 Mrad (No safety factor)
Technology	65 nm