FPGAs in radiation environments

(in High-Energy Physics)

ACES workshop, April 2018

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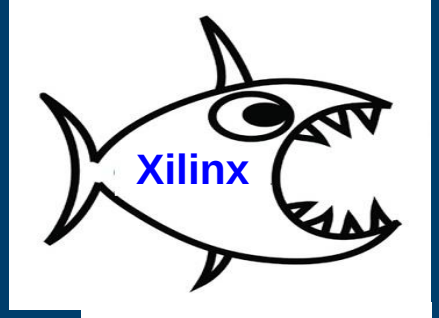
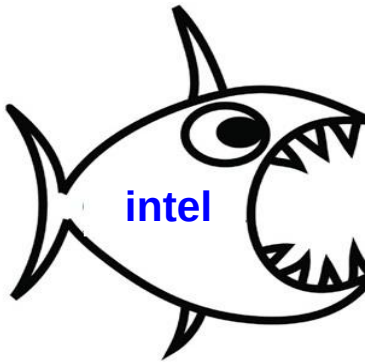
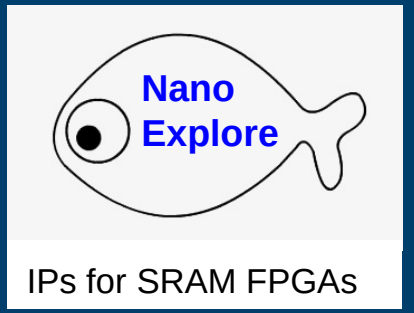
FPGA market

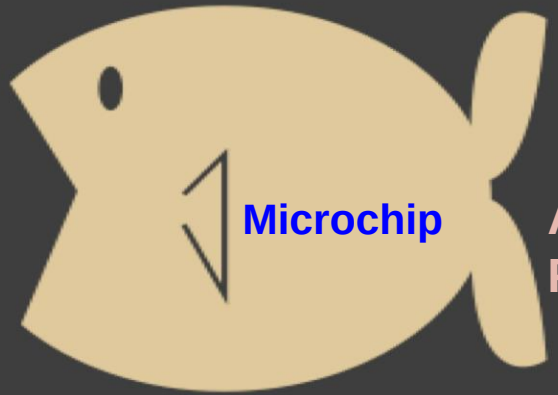


SRAM-based





IPs for SRAM FPGAs



Anti-fuse and Flash-based

Commercial-grade versus Rad-tol grade

Commercial-grade FPGAs are not specifically developed to tolerate radiation.

Some vendors also offer FPGAs specifically developed for radiation environments. These FPGAs can cost about 100 times more than commercial-grade FPGAs. They are targeted to space systems, where very small quantities of FPGAs are used per system.

HEP systems often uses many 100's FPGAs, and they cannot afford to buy the radiation-tolerant grade

→ **this presentation will focus on commercial-grade.**

Radiation effects on commercial-grade FPGAs (list not exhaustive)

	Destructive events (SEL, etc)	SET	SEU on configuration	TID
SRAM [12, 13]	No	Yes	Yes	
Anti-fuse [12]	No	Yes	No	
Flash [8]	No	Yes	No	

SEE are mostly caused by hadrons above 20 MeV (= HEH = High Energy Hadrons).
SEU-sensitivity on the user logic depend on the design, but it is similar for all commercial-grade FPGAs.
There are more effects, often family-specific. For example on PLLs, internal voltage regulators, etc.

SRAM-based FPGAs: pros and cons

- Re-programmable
  - Can add features after installation , allow to try more complex logic
- Fastest FPGAs
  - Latest silicon processes (example: 16 nm for Xilinx UltraScale+)
  - LVDS ports: 1.6 Gbps. SERDES: 32 Gbps.
- Best TID tolerance
  - At least 5 kGy (some parts much more)
- Drawbacks
  - Worst power consumption
  - SEUs in the Configuration: for example a connection or a logic-gate can be modified
  - Need scrubbing (requires even more power) [11]

Antifuse FPGAs: pros and cons

- Reliability:
  - No SEU on configuration
- Drawbacks:
  - Limited resources
  - Non-reprogrammable
  - Speed : 700 Mbps LVDS ports
  - TID tolerance : 800 Gy

→ Not much interest for new projects

Flash-based FPGAs : pros and cons

- Re-programmable
  - Can add features after installation , allow to try more complex logic
- Reliability:
  - No SEU on configuration
- intermediated density and speed:
  - LVDS port: 1.25 Gbps. SERDES 12.7 Gbps (on PolarFire)
- Drawbacks
  - TID tolerance : ~700 Gy (on igloo2, SmartFusion2)
  - ability to reprogram fails at much lower TID
  - design tools not as mature as for SRAM FPGAs

Use cases at CERN

	Present	Plans for next generation
nanoFIP (accelerators)	ProASIC3. [1]	investigating Smartfusion2 and nanoXplore FPGA [2]
LHC SciFi , Cal, and Muons	Antifuse AX , ProASIC	Igloo2
LHCb RICH	Antifuse AX , ProASIC	Xilinx Kintex7 [4]
ALICE ITS [7]	no FPGAs	Xilinx ultraScale(+) , ProASIC3L (scrubber).
ALICE TOF	ProASIC	Igloo2
ALICE TPC	SmartFusion2	
ATLAS muon RPC	Xilinx	Xilinx
ATLAS TGC Muon	Antifuse AX	Plan A : Xilinx Kintex-7 Plan B : PolarFire
CMS RPC Muon	Xilinx SPARTAN3; Actel ProASIC+ as blind scrubber, every 10 minutes.	Plan A : Xilinx Kintex7 and SmartFusion2. Plan B : PolarFire
CMS DT Muon	no FPGAs	PolarFire
CMS HCAL [10]	ProASIC3L, igloo2	

Design techniques (1/3)

Techniques to mitigate SEUs : TMR, fault-tolerant FSMs, EDAC codes, watchdogs, scrubbing. Each of this technique can be implemented in a number of different ways…

There are two commercial synthesisers that can help with this:

1. Synplify Pro® (cannot do TMR on IP blocks)
2. Precision® Hi-Rel (can do TMR on IP blocks). The US government has recently removed the export limitation on this item.

Do not blindly trust these tools, they had bugs in the past. It is better to understand what they do and occasionally double-check.
Synplify Pro® has a directive named "syn_safe_case" , for FSM synthesis. In 2016, a support person Synopsys verbally advised NOT to use it because it is not safe !!

Design techniques (2/3)

There are also SEU-mitigation tools developped by academia and research lab.

- Tools from the HEP community
  - **do they have long-term support, in order to work with new FPGAs ?**
- Tools from the space community
  - **do they remain available once they have good funding and results ?**

Design techniques (3/3)

- **incorrect implementation can increase errors !!!**
- **no strategy is 100% fail-safe**

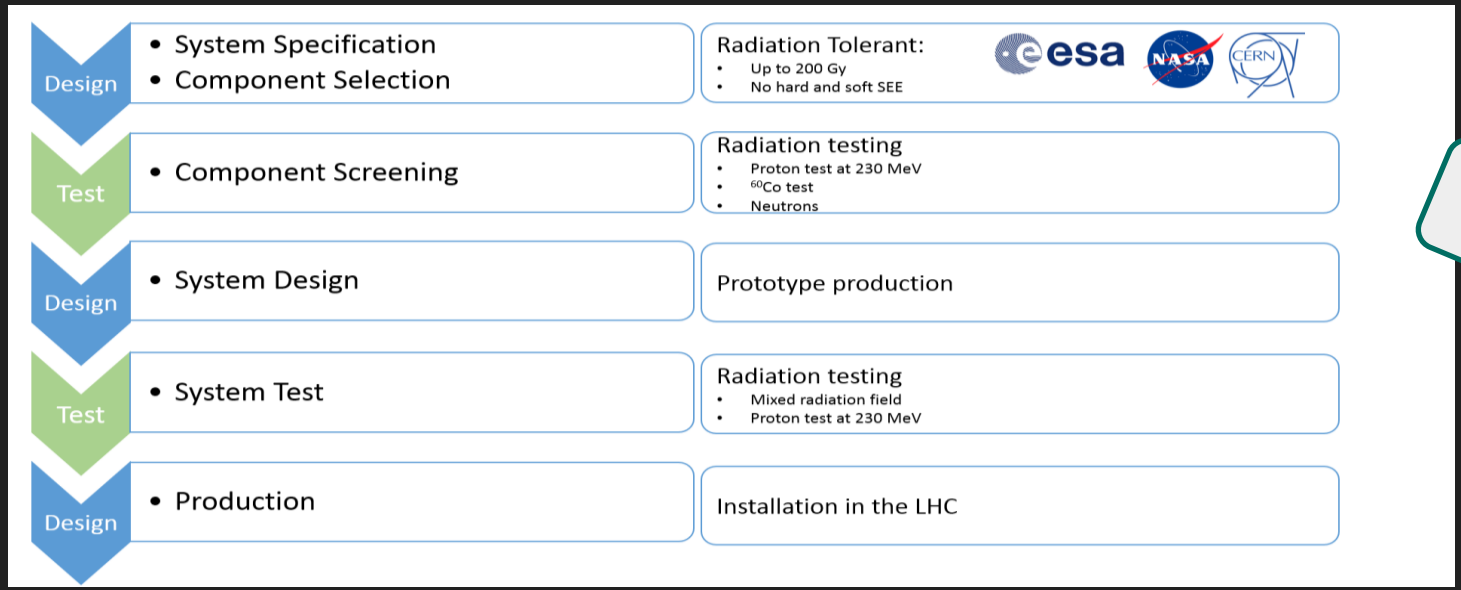
Warning

Do not mitigate failure mechanisms that have insignificant contribution to the overall failure rate. This:

- adds risk
- slows down system
- can provide a false sense of protection.

Testing FPGAs in a radiation environment

- Typical CERN process for quality assurance of COTS can be applied also to FPGAs (it can be simplified for certain FPGAs)
- Initial radiation tests can be done with gamma or x-rays
- Main radiation test usually done in proton beam
- Once a prototype system is ready, it should be tested: **where?**



Courtesy of S. Danzeca

CHARM: a radiation facility for system testing

Courtesy of S. Danzeca

CHARM = Cern High Energy AcceleRator Mixed-Field Facility

Main purpose

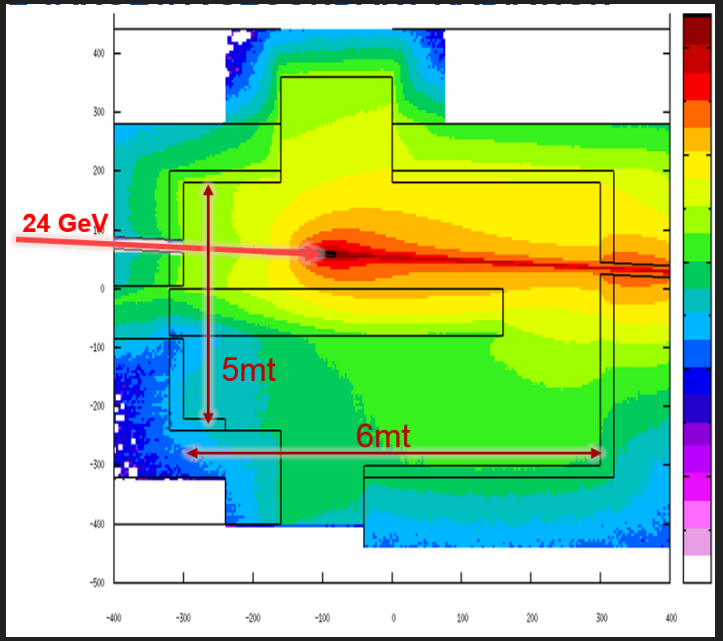
Radiation tests of electronic equipment and components in a radiation environment similar to the one of the accelerator

Large dimension of the irradiation room

- Large volumes electronic equipment
- High number of components
- Full systems

Numerous representative radiation fields

- Mixed-Particle-Energy: Tunnel and Shielded areas, atmospheric and space environments
- Direct beam exposure (proton beam 24 GeV)



Collaboration within HEP

In the last few years there have been cases of technical collaboration and sharing of results, also thanks to previous ACES workshops. This has been very useful. Note that this is based on individual initiative.

There is not much collaboration about dealing with vendors. It could be useful to organize that. Many Cern projects make purchases of the order of 100 k$ and do not have much leverage with vendors.
A customer making a purchase > 1 M$ would be taken much more seriously, and could have more access to internal details and maybe to product decisions.

More documentation:
https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/InformationOfInterest

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