Serial Powering for Pixel Detectors

Special thanks to Matthias Hamer for providing ATLAS material.

Outline

- **Introduction**
  - Collaborating institutes
  - Next generation pixel detectors & chip
  - Serial powering concept
- **Shunt-LDO regulator**
  - RD53A Shunt-LDO
  - Simulations
  - Testing results
  - Future plans
- **System aspects & experiments**
  - Thermal aspects & Failures
  - ATLAS & CMS layout & power chains
  - Other SP activities
- **Summary**

RD53 Institutes involved in serial powering

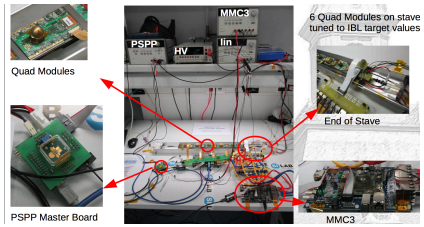
Dortmund

RD53
Shunt-LDO DESIGN

INFN Istituto Nazionale di Fisica Nucleare Sezione Pavia

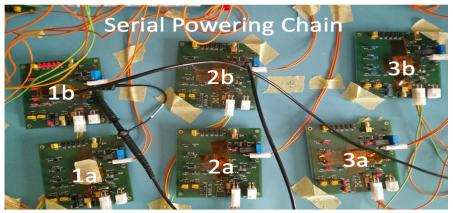
RD53
Bandgap DESIGN

bonn



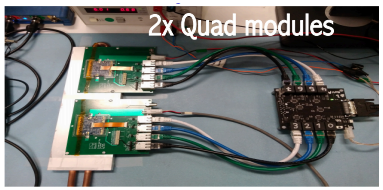
ATLAS System tests
RD53 SLDO padframe
BDAQ53 support

CERN



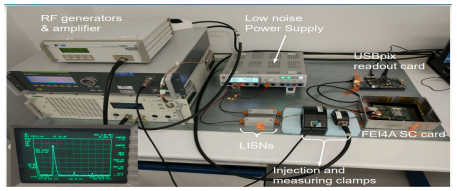
RD53 SLDO design verification & validation
CMS System Tests
ATLAS Demonstrator Tests

BERKELEY LAB



ATLAS System tests

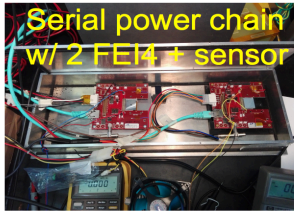
ITA INNOVA



RD53 SLDO design verification & validation
CMS EMC tests

More CMS & ATLAS institutes involved in SP

INFN Istituto Nazionale di Fisica Nucleare

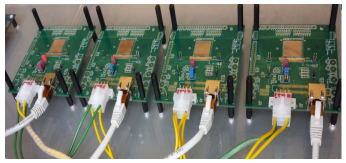


CMS System tests
CMS Power system

Bergische Universität Wuppertal · 1972

ATLAS PSPP chip
ATLAS system tests

ETH



CMS System tests
CMS Module design

ATLAS System tests
Previous involvement
SP for ATLAS strips

University of Liverpool

ATLAS System tests
ATLAS Power system

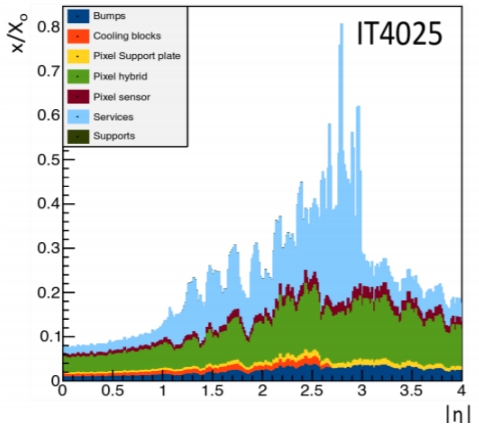
Oklahoma State University

Next generation pixel detectors & chip

Pixel detectors' environment:

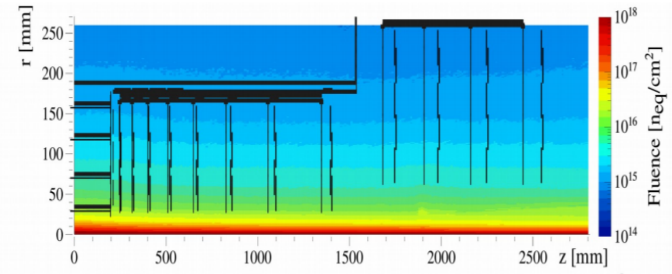
- **Radiation levels**
  - CMS Innermost layers: $2x10^{16}$ n_{eq}/cm^2, 1 Grad TID
  - CMS Outer layer and Service cylinder (R~20cm) : $1x10^{15}$ n_{eq}/cm^2, 100 Mrad TID
- **Material budget**
  - Service cylinder in the tracking region
- **Space**
  - Stringent physical constraints in the services channels
  - Minimize mass of services and auxiliary electronics

ACES 2018 Overview of the pixel upgrades talk (T.Heim):
https://indico.cern.ch/event/681247/contributions/2929051



RD53 pixel readout chip:

- 65nm CMOS technology for high density logic and low power
- Large chip (~2x2 cm^2, ~10^9 transistors)
- Pixel supply voltages: Analog 1.2V, Digital 1.2V
- Requires current levels of 8 uA/pixel (4 uA/analog, 4 uA/digital).
- For a full size pixel chip (~150k pixels), after adding periphery, **total current needed ~1.3 A under normal operating conditions.**
- **INTEGRATED SHUNT-LDO** allows for serial powering operation
- **AC-coupling** (Aurora for data/DC balanced protocol for commands)



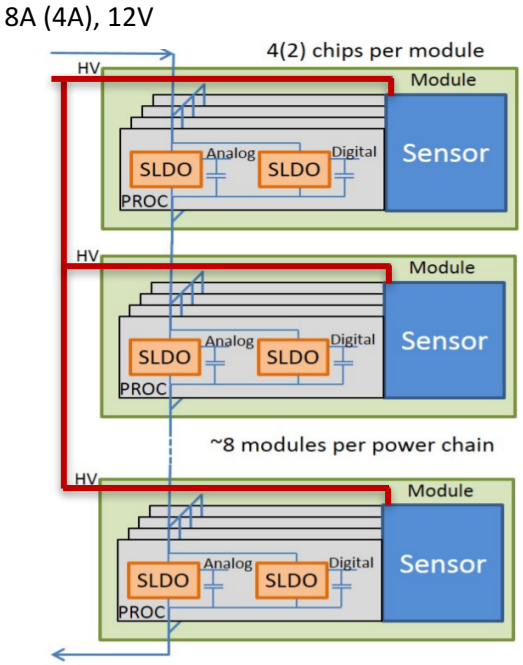
ACES 2018 RD53A talk (F.Loddo):
https://indico.cern.ch/event/681247/contributions/2929050

Serial Powering Concept

Serial powering has been identified as the baseline choice for powering the CMS and ATLAS HL-LHC pixel detectors.

It is a based on a shunt-Low Drop Out regulator design:

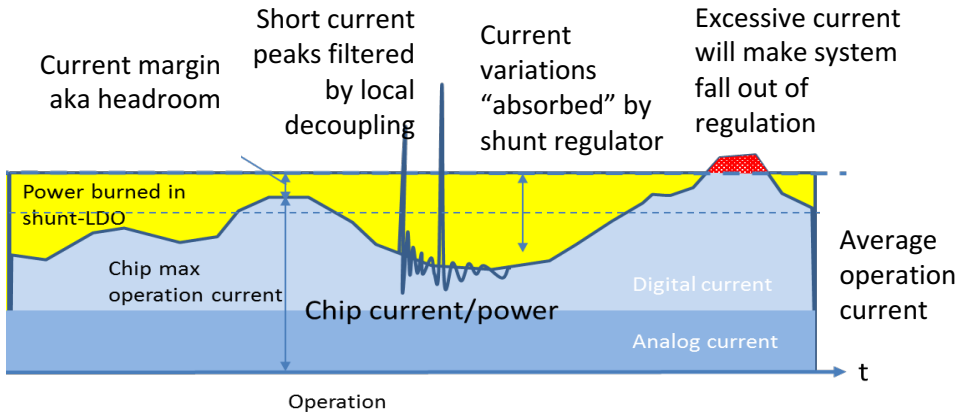
- ✓ Low mass
  - ✓ power cabling reduction ∝ length of chain
- ✓ On-chip integrated solution
- ✓ Radiation hard
- ✓ Not sensitive to voltage drops
- ✓ Smooth Operation with low noise independent of load variations



Across-module serial powering:

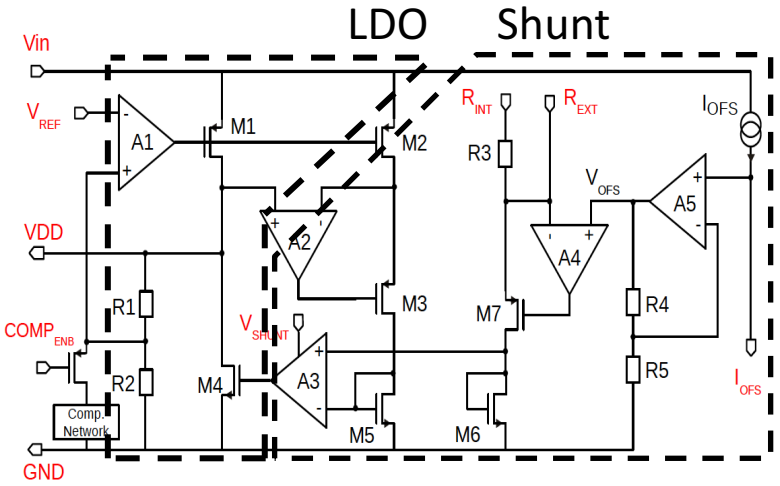
- •Pixel detector modules serially powered.
- •Up to four chips per module powered in parallel.
- •Modules/ sensors grounds differ inside a chain.

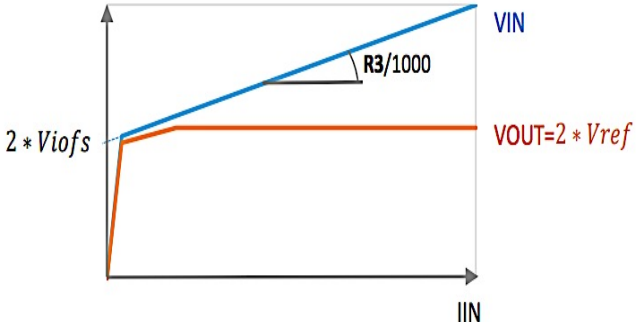
- •**Iin** "re-used" among multiple loads in series
- •Enough current injected to satisfy the highest possible load current.
- •**Total current constant- independent of load** at the cost of extra power burnt in the shunt, known as **headroom**.



RD53A Shunt-LDO regulator Designed by M. Karagounis

- **65 nm for Iin= 2A, Vin =2A** (FE-I4 version was 0.5A)
- **Configurable Resistive behavior** allows for well-defined current sharing, determined by their effective resistance.
- **Configurable Offset voltage**, allows for an optimization of the power consumption.
- Improved control loop for **capacitive load**.
- **Off-chip decoupling capacitors** (uF) for LDO stability at the input and the output of the circuit.
- The reference and offset voltages are provided by **on-chip integrated BANDGAPs** (2/Shunt-LDO)
  - Vref value can be trimmed using trimbits.





$$VIN = 2 * Viofs + \frac{R3}{1000} * IIN$$

$$Viofs = 2\mu A * Riofs$$

For an introduction to the Shunt-LDO circuitry see M.Karagounis paper:
https://indico.cern.ch/event/72160/attachments/1036621/1477145/Shunt-LDO_Regulator.pdf

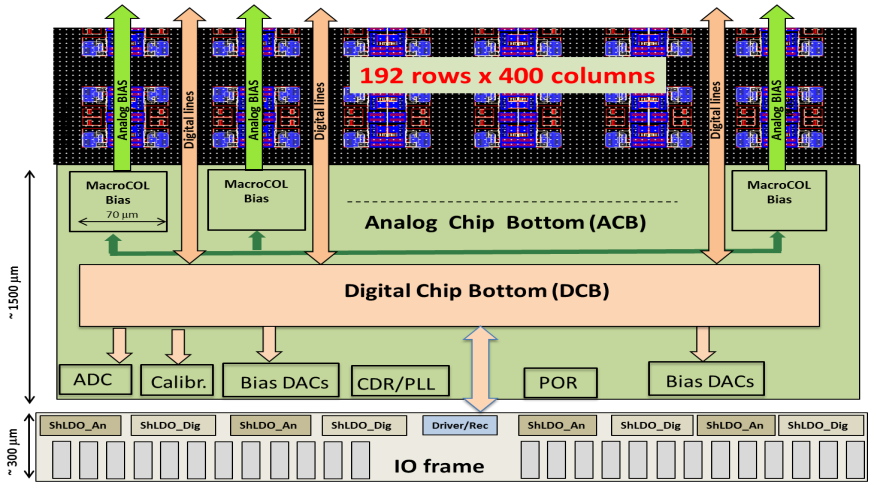
Shunt-LDO integration

- A specialized local **Shunt-LDO of 2.0 A per power domain designed and integrated as in the final chip**
  - Almost 100% current margin could be burnt by the Shunts
  - Split in 4*0.5A blocks for heat distribution and reliability
  - Absolute max power: < 4W (1W/cm^2 for final chip)

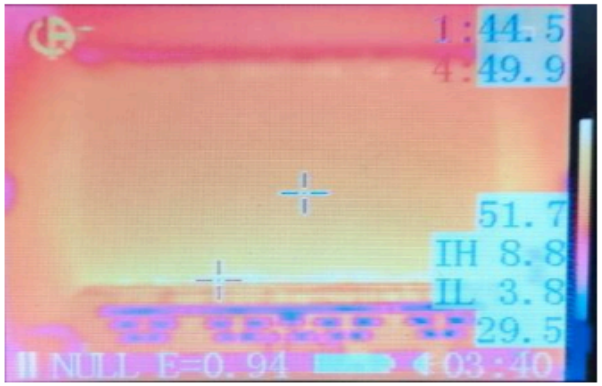
- Analog and digital circuitry in separated **deep N-wells** for maximum possible substrate isolation.
  - Analog (VDDA, GNDA) & Digital (VDDD, GNDD)

- **Decoupling capacitance**
  - from digital logic ~300 nF for full size pixel chip & analog FE ~70 nF.

RD53A functional floorplan



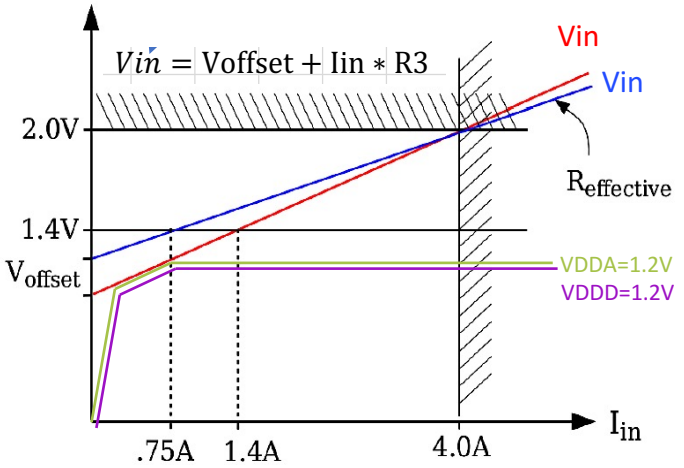
Picture with thermal camera for Iin=2.0A, Vin =1.45V (2.9W)



RD53A Shunt-LDO Resistive model

Shunt-LDO makes power load look like resistor with voltage offset.

- **Critical for appropriate current sharing and stable operation.**
- Power consumption variations inside chip not “visible” from outside.
- Shunt current dynamically regulated to keep chip current constant.

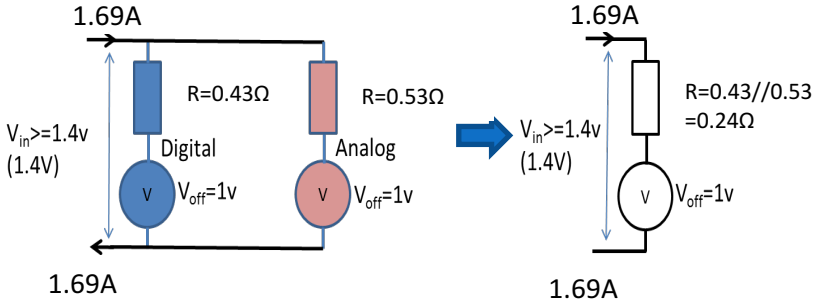


Shunt-LDO Parameters:

- Drop-out voltage (min 0.2V)
- Effective resistance
- Configurable offset
- Extra headroom is user’s choice (10%, 20%, etc.)

Nominal operation of full size chip (400x328 pixels):

- Drop-out voltage of ~0.2V => **Vin=1.4V**
- **Voffset=1V**
- Current headroom **~25%** (will be less in the final)
- R3 adapted such that Vin(4A/chip)=2.0V
  - R_{digi} = (1.4V – 1.0V) / (0.75A *125%) = 0.43Ω
  - R_{ana} = (1.4V – 1.0V) / (0.6A *125%) = 0.53Ω
  - Total chip Req = 0.24Ω

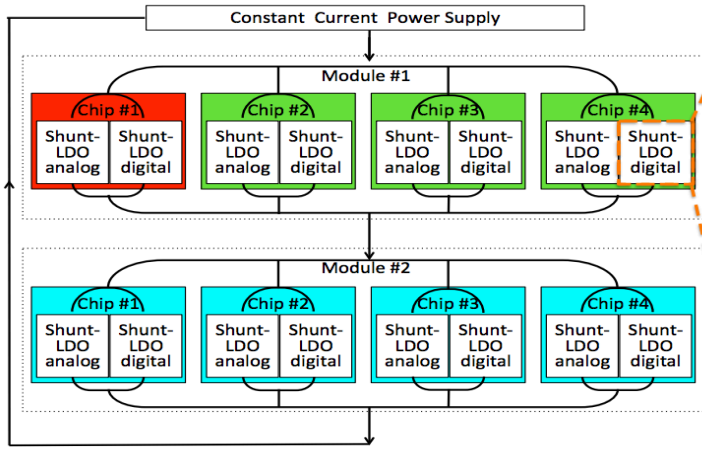


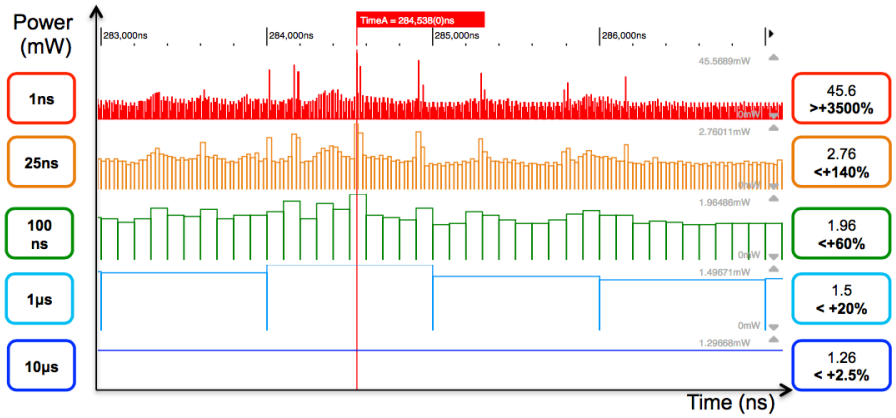
System Simulations with power profiles

System simulations (Cadence Virtuoso) with Shunt-LDO detailed design, serially powered pixel modules and parasitic elements.

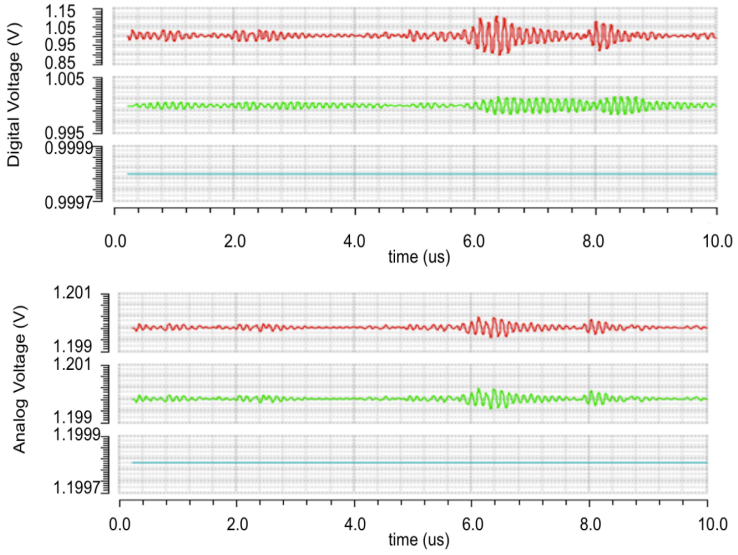
Dynamic profiling of both digital and analog power

Noise coupling has been found to been within acceptable limits (Vout ripple 100mV for digital, <10mV for analog).





Power profiles at different time-scales with Monte Carlo hits (3GHz/cm^2), triggers (1MHz) from detailed gate level simulations after place and route and with circuit parasitics for 64x4 pixels



S.Marconi (CERN)

More details: http://iopscience.iop.org/article/10.1088/1748-0221/12/02/C02017/pdf

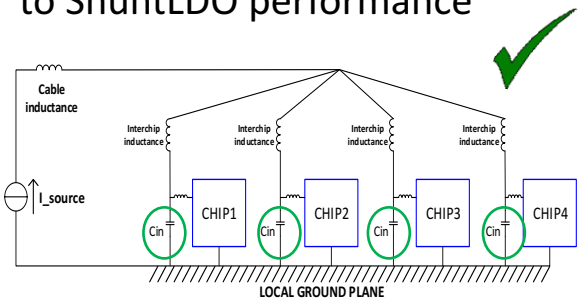
More Shunt-LDO simulations

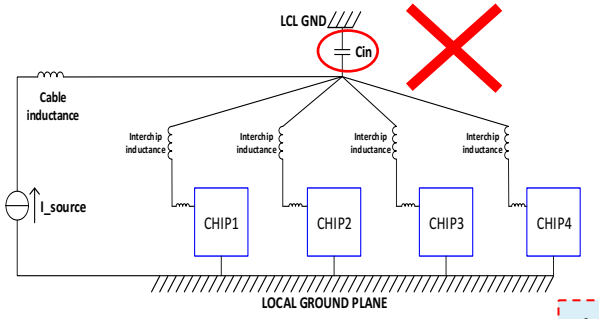
1. Verification of any improved features and validation of SLDO from designer team:
   - Input current
   - Process and mismatch variations
   - Different loads
   - Temperatures: -50°, 27°, 120°
   - Voltage sources as replacement for bandgap
   - With internal/ external resistor

Checking:
- ✓ Voltage Limits
- ✓ Transient response
- ✓ Line Regulation
- ✓ Load Regulation
- ✓ Startup
- ✓ Stability Analysis
- ✓ Sweep of external Resistance
- ✓ Monte Carlo Simulation

Michael Karagounis (Dortmund)
Andreas Stiller (Dortmund)
Jeremias Kampkötter (Dortmund)

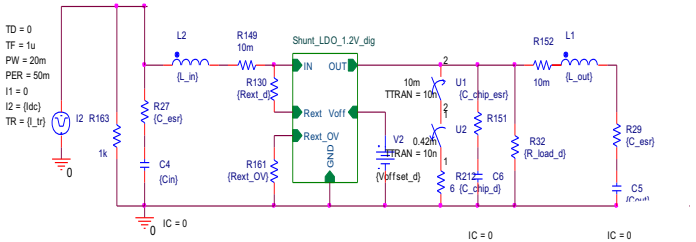
2. Module-level simulations for study of the impact of HDI parasitics to ShuntLDO performance





A.Luengo (ITAINOVA)

3. Spice simplified model



RD53A Single Chip Card: Shunt-LDO options

Power (PWR) configuration options:

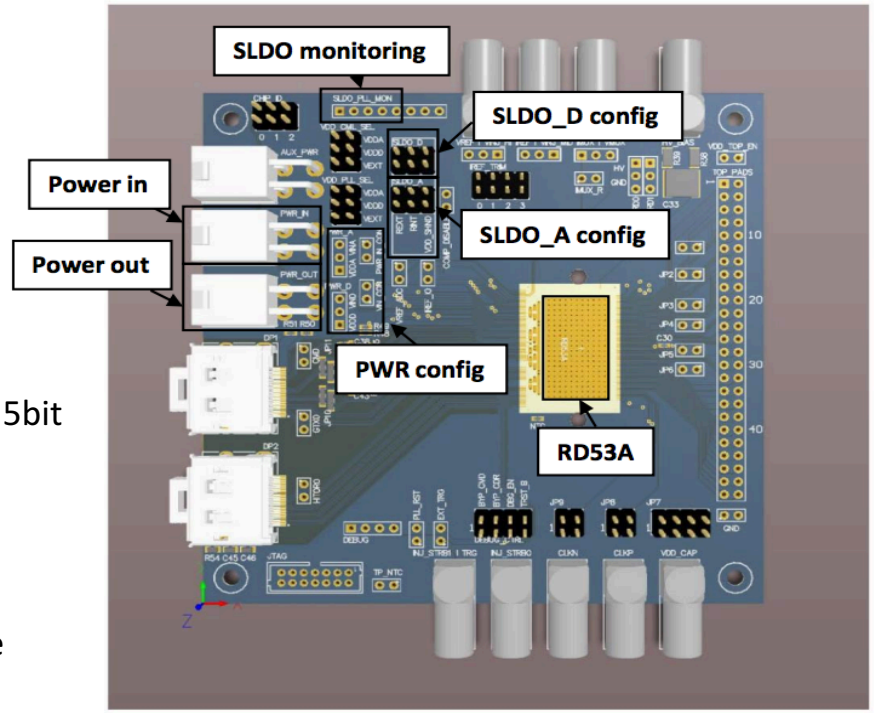
- Serial or single chip operation
- SLDO or Direct powering (bypassing SLDO)
- Parallel or separately

Shunt-LDO_A/D configuration options:

- Internal (~600Ω) or external R3
- LDO or ShuntLDO-mode
- Monitoring signals: Viofs, Vref for both SLDOs
- Output voltage configurable digitally (1.0V-1.48V) via 5bit
- Overwriting of Vref, Viofs possible

External resistors for each ShuntLDO:

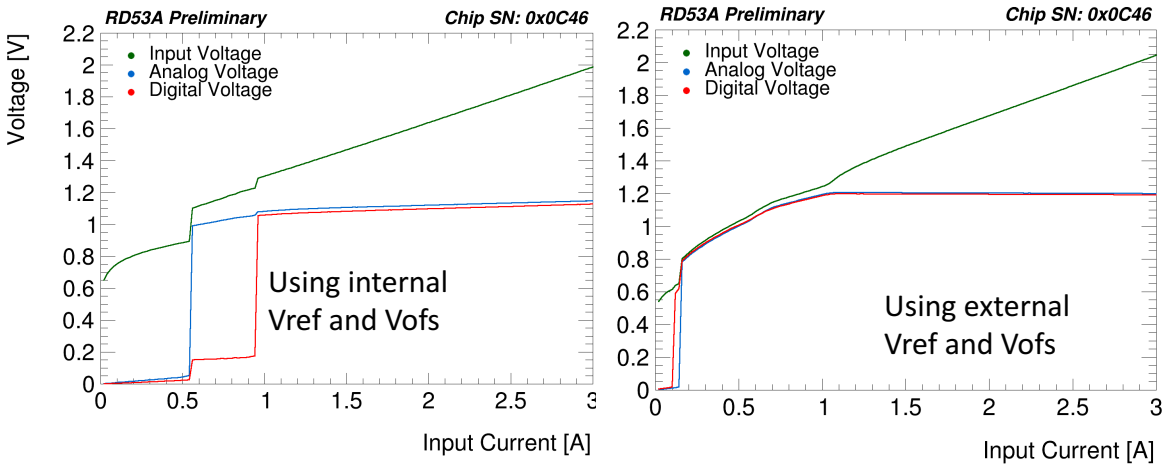
- Resistor for Offset Voltage (RIOFSA, RIOFSD) has to be mounted for Shunt-LDO mode
- External R3 (REXTA, REXTD), alternatively RINT (~600Ω) can be used



First results of RD53A testing: Shunt-LDO

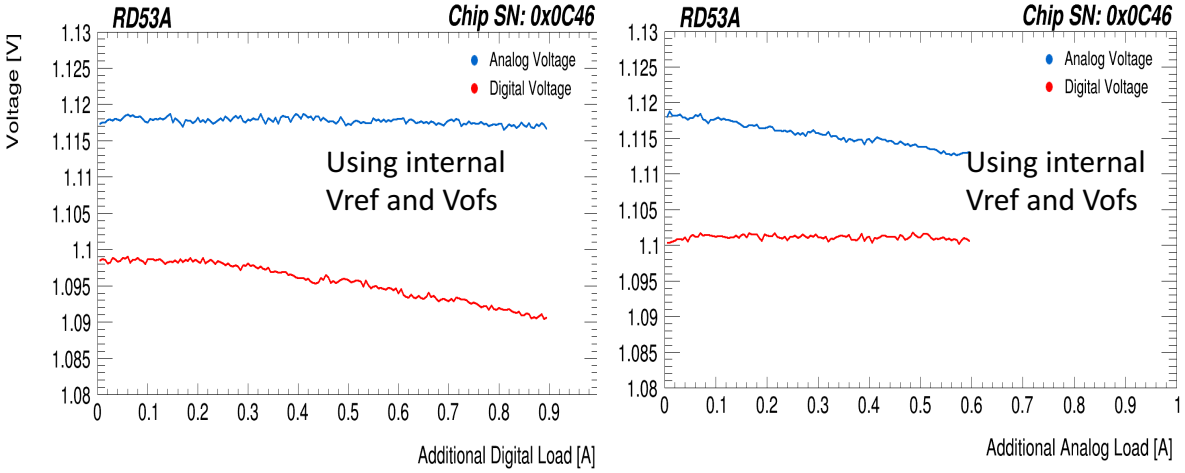
Line regulation:

- Bandgaps need a minimum V to start & difference in analog and digital bandgaps.
  - **New bandgap design (mini-asic)**
- Slope is higher than expected ≈0.37Ω instead of 0.3Ω & offset is lower than expected ≈0.9V instead of 1.0V
  - **Parasitics under investigation**



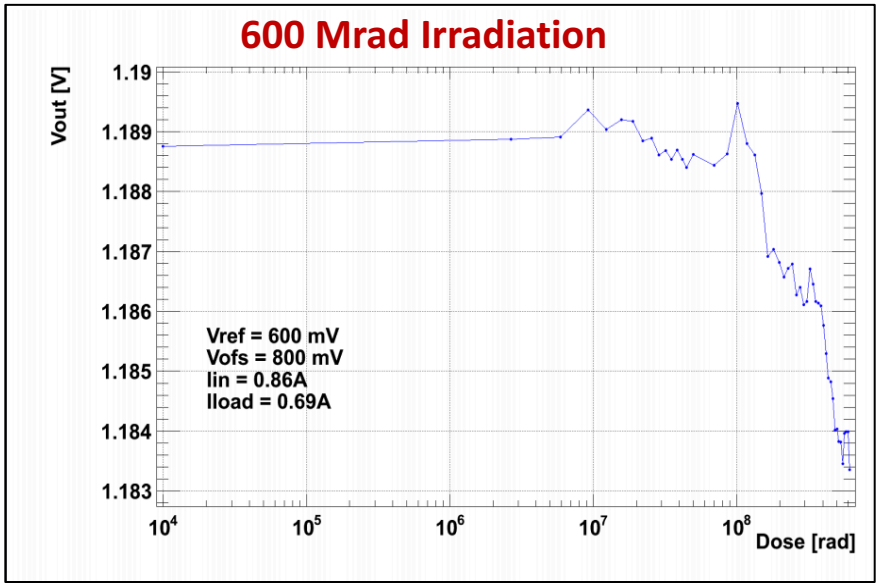
Load regulation:

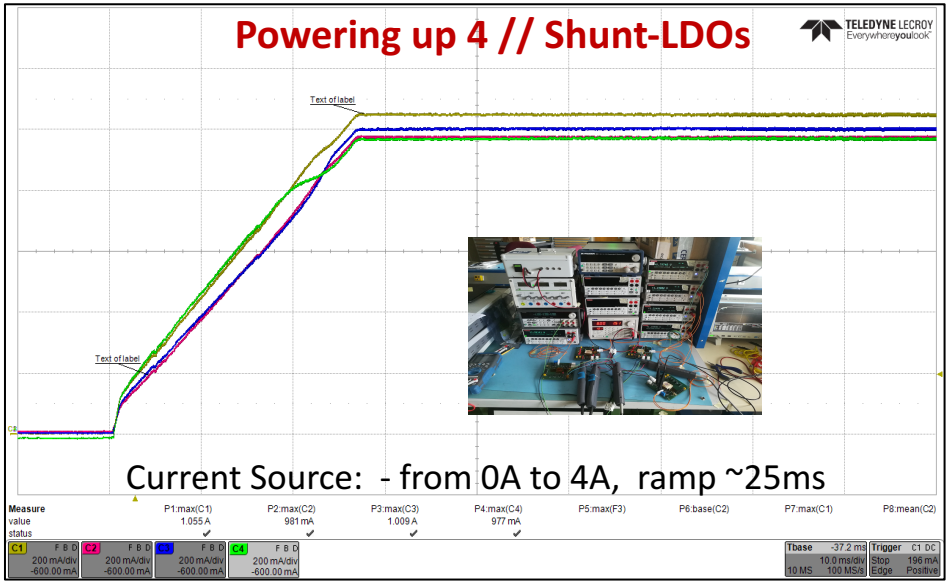
- After power-up 100mA digital load (no clk) and 400 mA analog load (matching simulations). Additional load was drawn from the Shunt-LDOs.
- VDDD decreases over load ~8mV/0.9A
- VDDA decreases over load ~5mV/0.6A

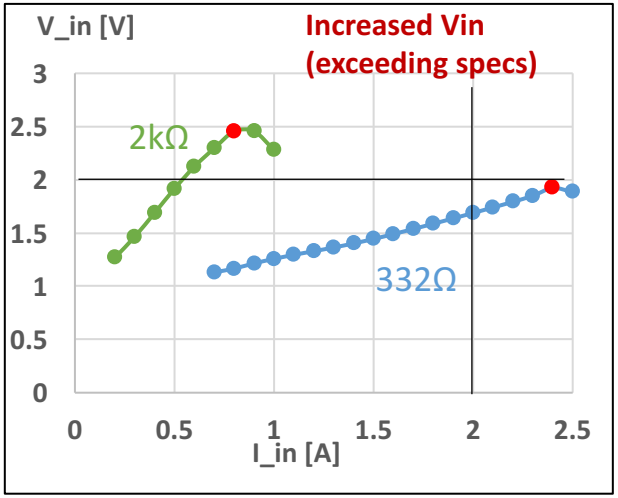


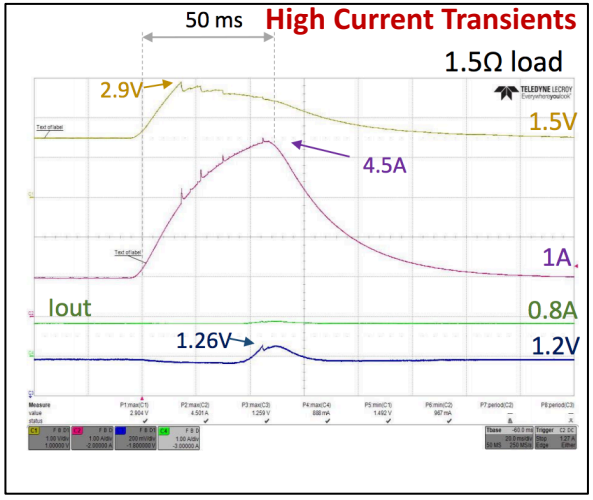
D. Koukola, CERN

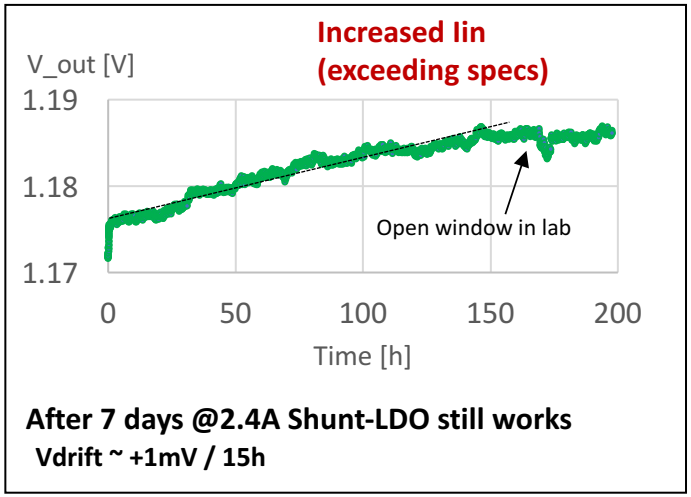
2.0A Shunt-LDO test-chip: Extensive testing







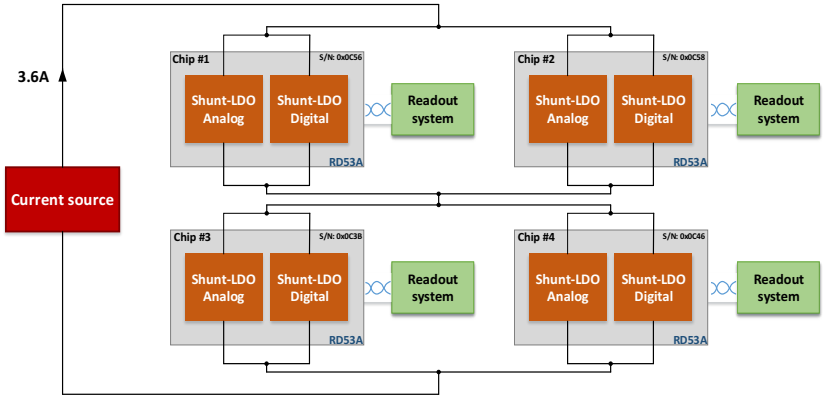




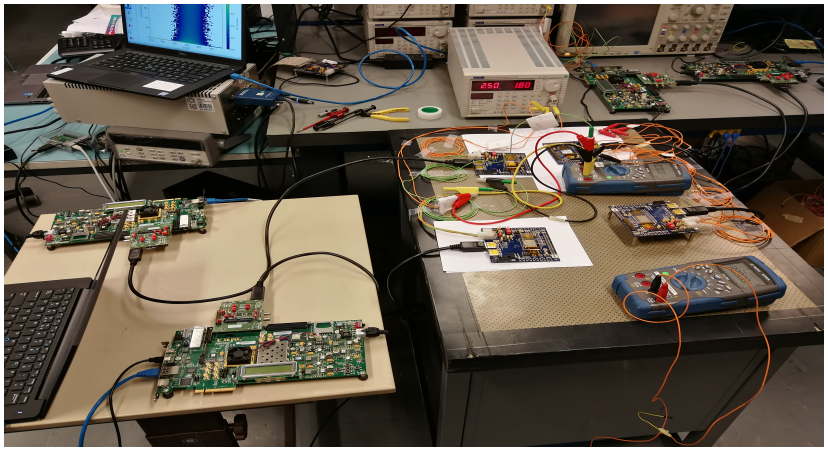
Matthias Hamer (University of Bonn (DE)), Florian Hinterkeuser (University of Bonn (DE)), Stella Orfanelli (CERN), Daniele Ruini (ETHZ), D.Koukola (CERN)

Future of RD53A serial powering

- **Shunt-LDO and system tests:**
  - Climatic chamber and radiation tests
  - Provide a nominal configuration for power up to users
  - Scale readout systems to support SP activity
  - Study impact of serial powering to threshold/noise
  - Transient/Noise/Failure propagation studies
  - Decide on configurability of bandgaps
  - Decide on optimal Voff, R values per ShuntLDO
  - Investigate protection schemes, HV distribution
  - System tests using current source, long cables and chains of pixel modules
  - Study SP chains with planar & 3D sensors



- **Mini-asic to be submitted in summer**
  - New scheme for generation of voltages (ref, offs)
  - Current monitoring
  - Under investigation:
    - low-power mode to test the chip without cooling, disabled with wirebonds
    - Output current limitation
    - Overvoltage protection



See more RD53A ShuntLDO RESULTS:
D. Koukola poster: https://indico.cern.ch/event/681247/contributions/2961205/

Thermal aspects

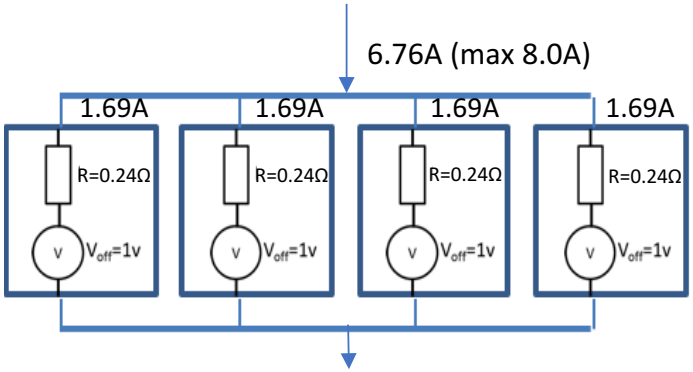
Normal operation:

- Pixel array: 2cm x ~2cm: ~uniform analog & digital power: < 1 W/cm^2
  - Temperature gradient across pixel arrays must be small
  - Analog FE and sensor temperature sensitive
  - Radiation hardness of chips relies on being operated cold.

1.5x Nominal power & no pixel array power consumption:

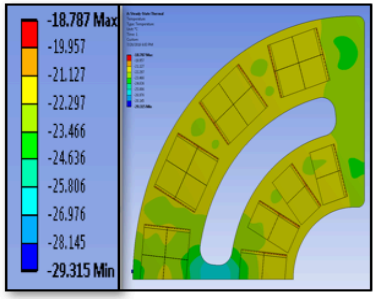
  - At power-up or if mis-configured
  - Pixel chip does not need to be operational.
  - Preliminary FEA simulations have shown that the chip won't melt.

=> Cooling pipes have to pass close to the Shunt-LDO hotspot!!!!



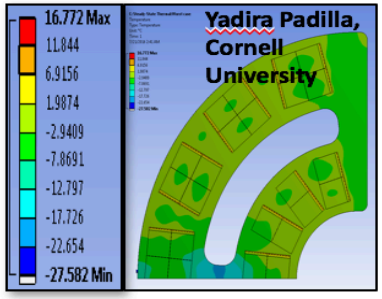
Injected current: 4x1.69A (max 2.0A)= 6.76A (max 8.0A)
Voltage: 1V+6.76A*1/4*0.24Ω=1.4V (max 1.48V)
Chip power: 6.76A/4*1.4V=2.3W (max 2.96W)
Total power for a quad module: 6.76A*1.4V =9.1W (max 11.84W)

Normal operation

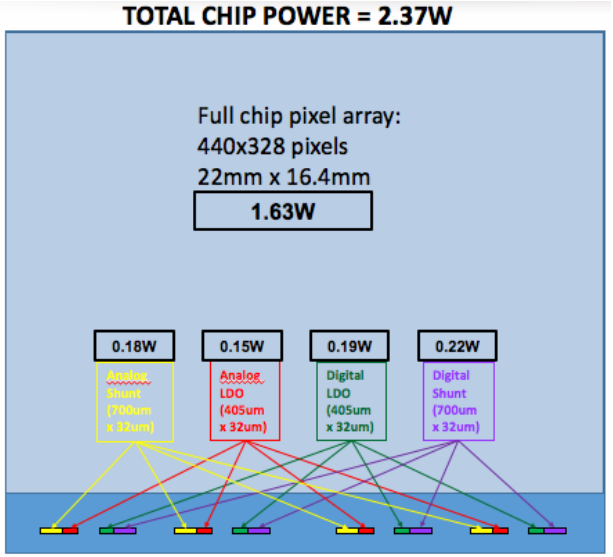


Location	ΔT [ºC]
Quarter of an endcap disk structure	10.5
ROC Pixel area	2.5
LDO, Shunt, Periphery	3.7

Pixel arrays shut-down



Location	ΔT [ºC]
Quarter of an endcap disk structure	44.4
ROC Pixel area	5.1
LDO, Shunt, Periphery	26.0



Failures & protection

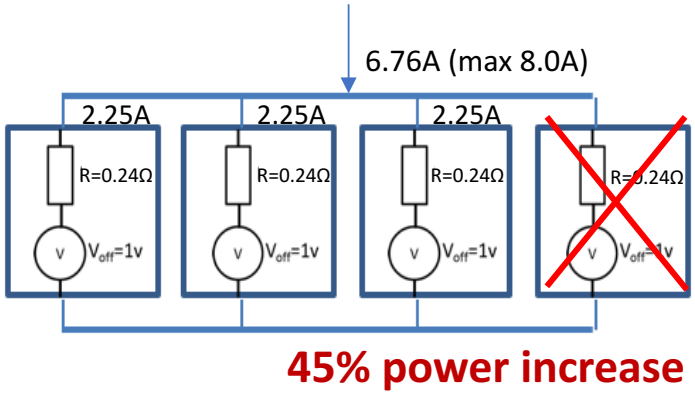
Open circuit:

Collapse due to load or fast start-up

⇒ current transients & power increase for remaining chips

⇒ over-voltage transients at Vin

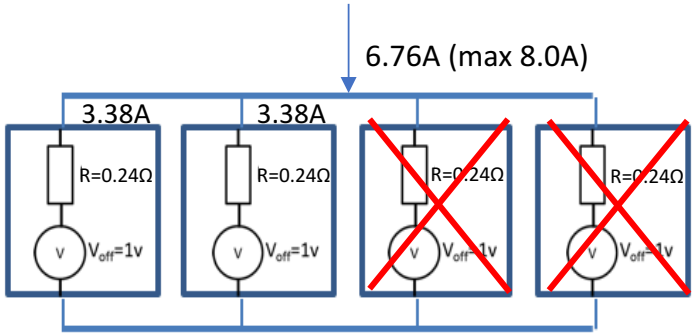
⇒ power increase for the remaining



45% power increase

Potential protection mechanisms:

- Voltage clamp (under study)
- Connect modules in parallel (if geometry permits)
- Use of PSPP chip in ATLAS to bypass modules



150% power increase

Overload / Short circuit:

Physical short or overload due to failure/misconfiguration:

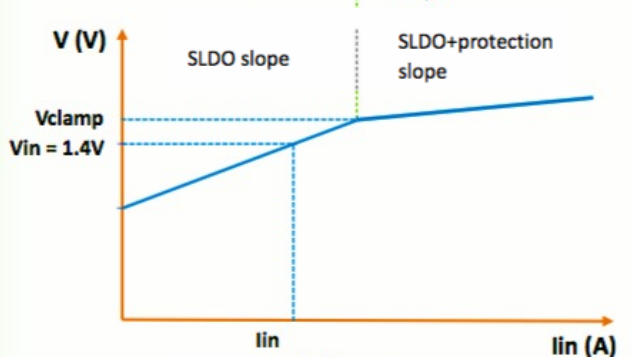
⇒ shorted Shunt-LDO takes most of the module current

⇒ input voltage decreases (1.1V) but not collapsing fully

⇒ rest of the chips underpowered

Potential protection mechanisms:

- Passive or active fuse
- Overcurrent protection (under study)
- Use of PSPP chip in ATLAS to bypass modules

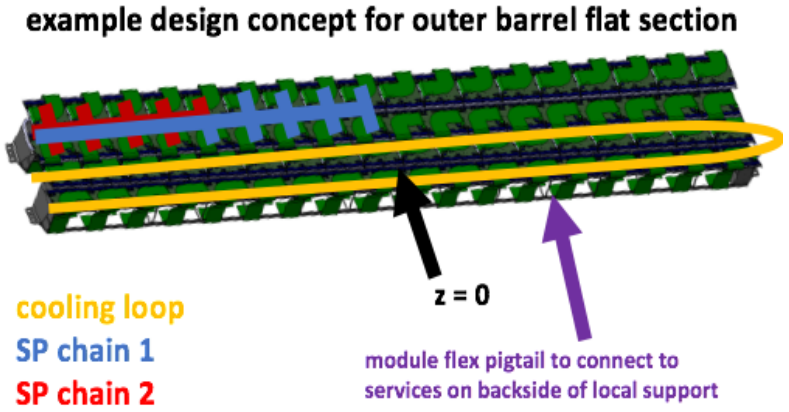


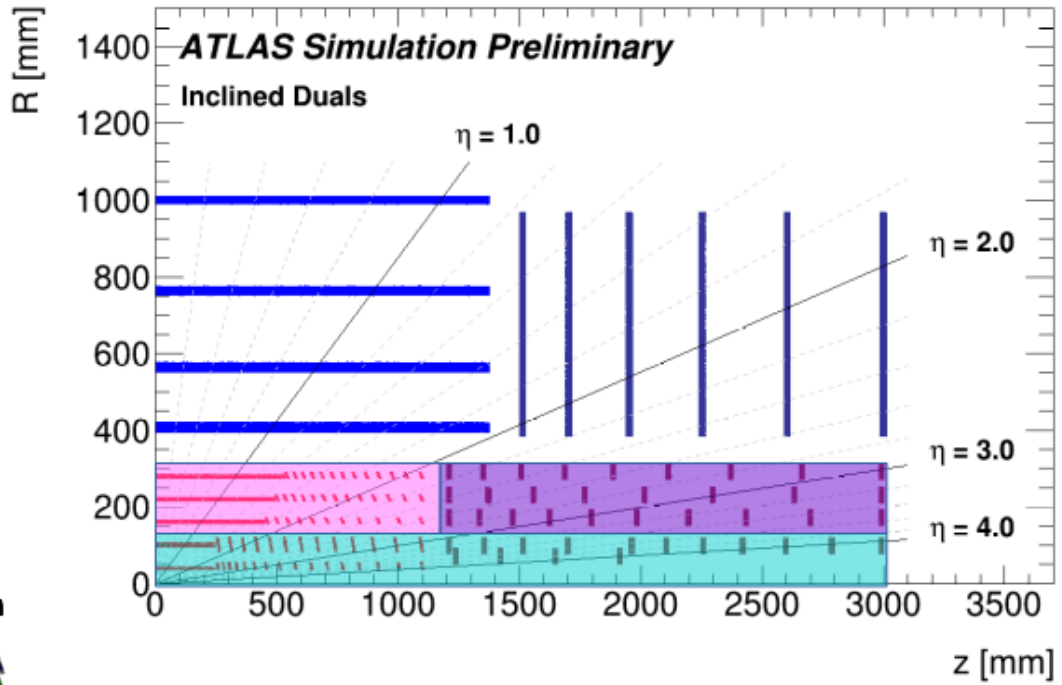
ATLAS layout & SP chains

ATLAS ITk Pixel detector layout:

- 3 subsystems
- Serial powering chains built
  - In z for barrel sections & in ϕ rings
- Powering unit: Always 4 chips in parallel.
  - One quad module
  - Two double chip modules
  - Four single chip modules

- in total, ~ 1000 SP chains for 8.000 modules
- Planar sensors & 3D sensors.



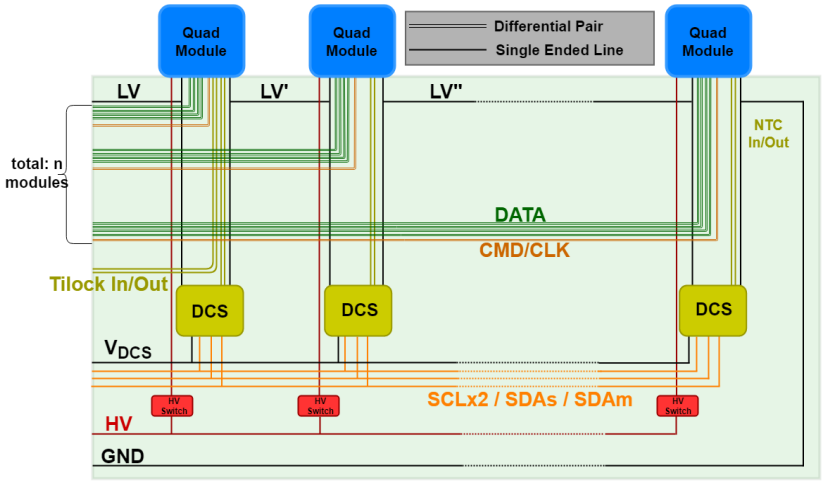


outer barrel	inner system	endcaps
3 layers	2 layers	3 layers
flat + inclined section	flat section + rings	rings
planar sensors	3D and planar sensors	planar sensors

ATLAS serial powering & PSPP chip

Serial power chains in ATLAS:

- Up to 14 modules per serial powering chain
- Up to 4 serial powering chains/same local support



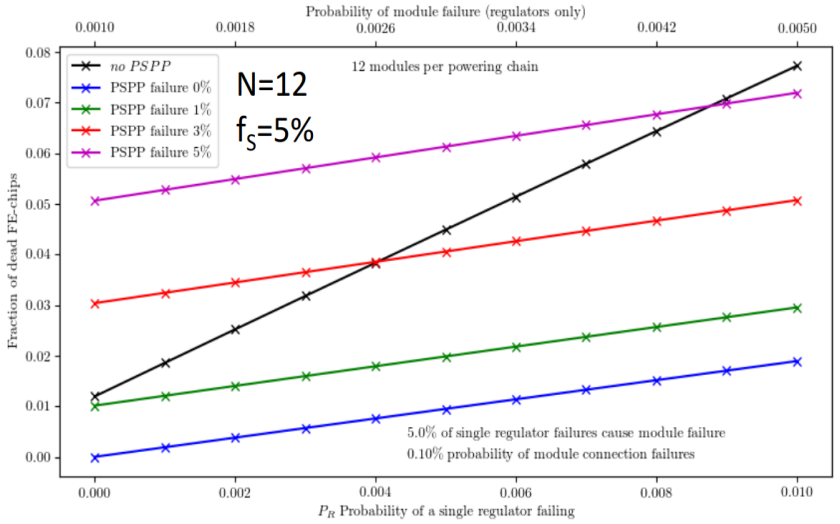
On-detector control system chip in parallel to each module

- measures module temperature
- measures voltage drop over module
- can bypass the module in the SP chain
- automated OT/OV protection
- power hungry bias resistors required
- risk analysis and final decision about implementation require tests with final FE chip

One NTC/SP chain hardwired interlock system

HV fuses/switches under discussion (difficult to implement)

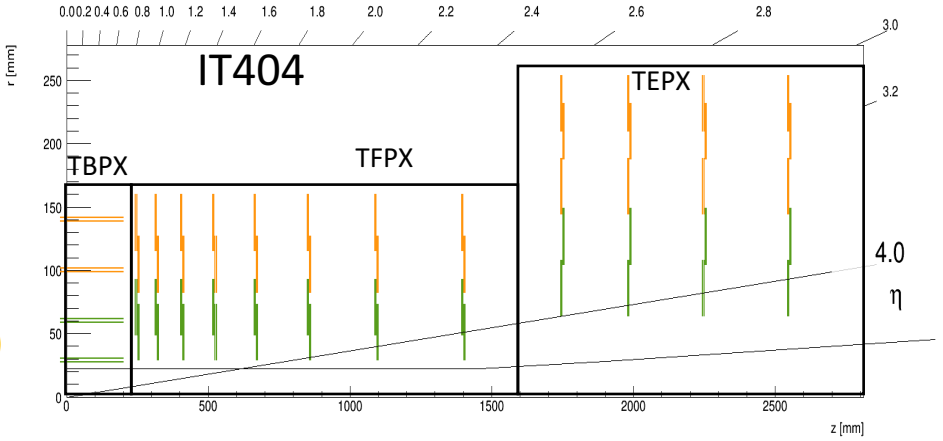
HV modularity (>1 HV line per SP chain) follows serial power chains. Extra return lines for HV under discussion

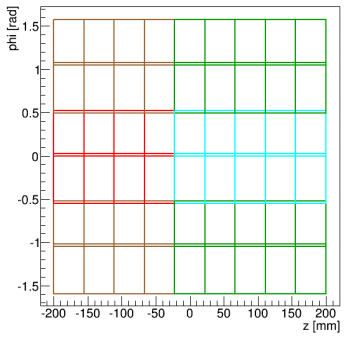


CMS layout & SP chains

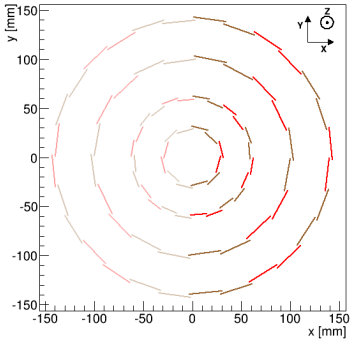
CMS Inner Tracker (pixel) detector layout:

- 3 subsystems
- Accessible & replaceable system
- Split mechanics in z and ϕ (built in quarters)
- Serial powering chains built
  - In z for barrel sections & in ϕ for rings
- Powering unit: Modules always in series
  - 2-chip modules TBPX L1, L2 & R1, R2 (4A chains)
  - 4-chip modules TBPX L3, L4 & R3, R4, R5 (8A chains)
- in total, ~ 564 SP chains for ~4244 modules
- Planar sensors. 3D are considered for inner layers/rings.

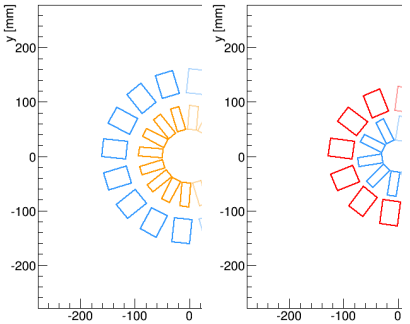




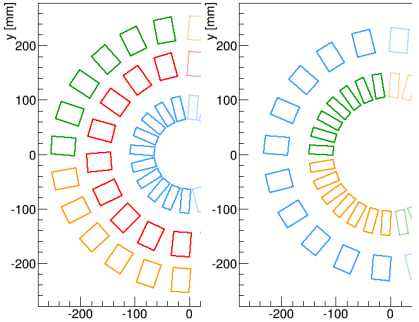
TBPX L1



TBPX



TFPX R1,R3 TFPX R2,R4



TEPX R1,R3,R5 TEPX R2,R4

Serial power chains in TBPX:

- 1 serial power chain for 2 consecutive rods in φ.
- Modules at Z=0: connect to the same end (alternation by layer)

Serial power chains in TFPX/TEPX:

- Up to 4 chains per (X) side /(Z) side of a ring.
- Chains do not connect front/back side for easiness of mechanics.

CMS serial powering, no aux electronics

Serial power chains in CMS:

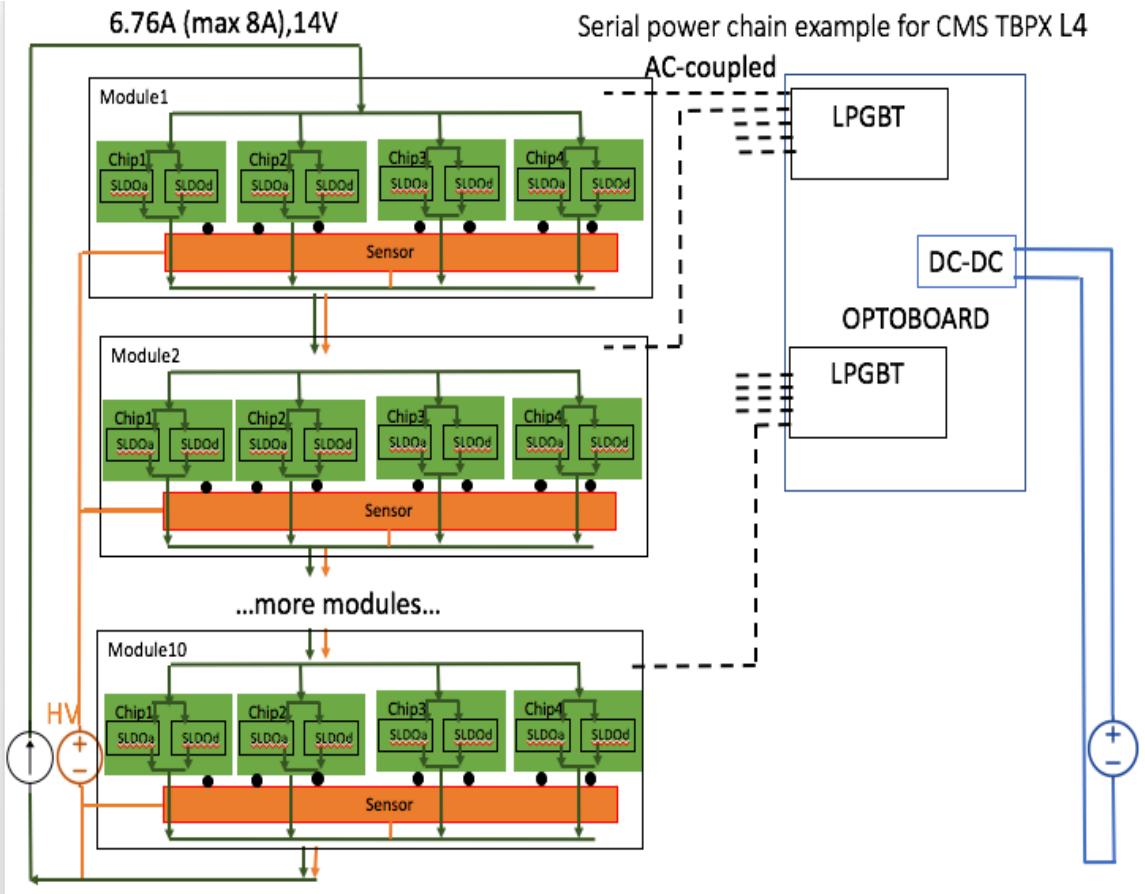
- Up to 10 modules per chain
- 1 serial power chain /2 rods in φ.
- No parallel modules.

Under study “simple” on-chip integrated protection mechanisms

Always reading/controlling with an optoboard modules that belong to the same chain.

One NTC/SP chain hardwired interlock system

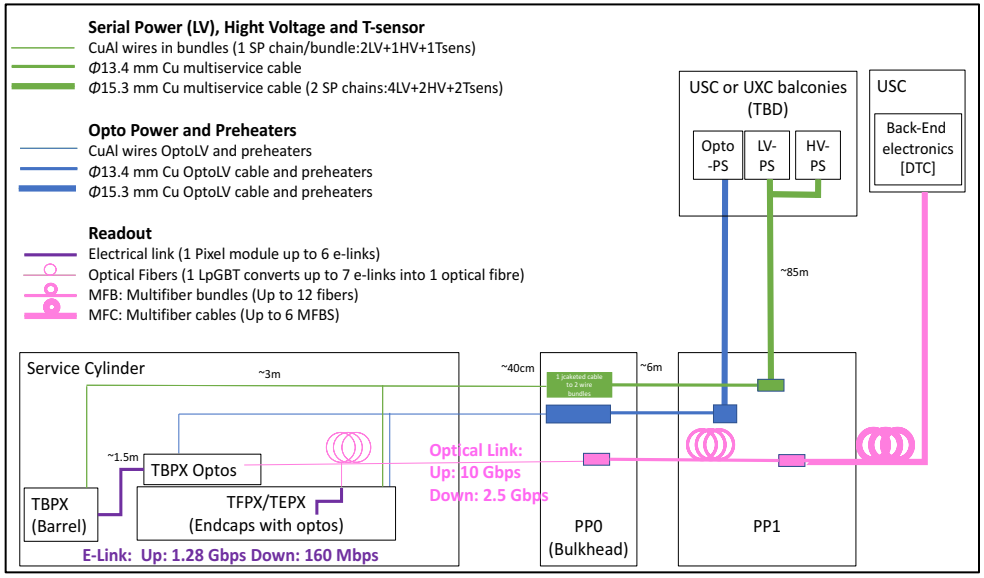
HV modularity (>1 HV line per SP HV modularity (>1 HV line per SP chain) follows serial power chains. Extra return lines for HV under discussion.

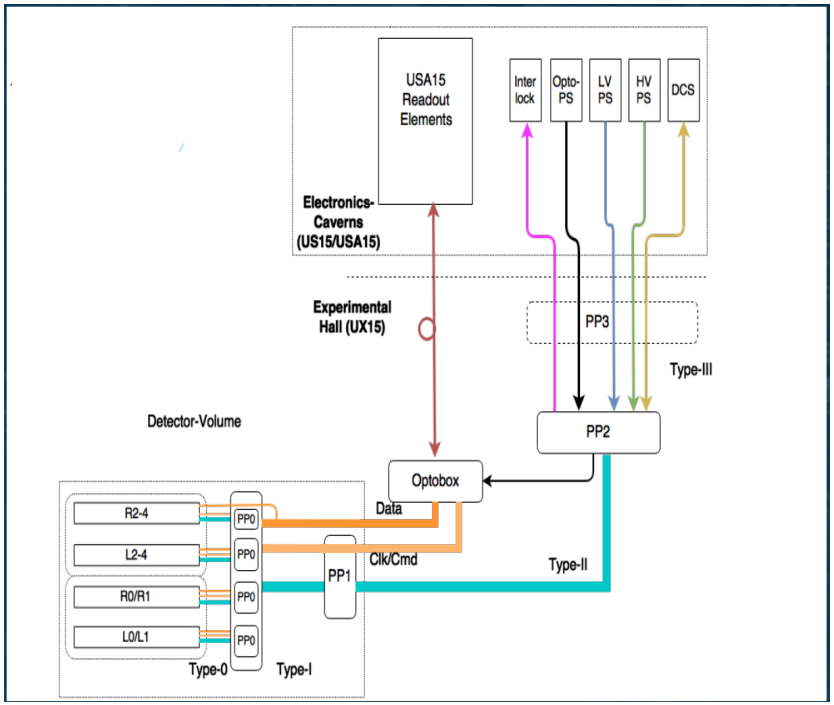


Services: cables & supplies

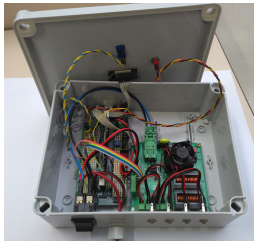
- CMS will use new multiservice cables, each one serving 2 SP chains off detector and CuAl on-detector.
- Location of PS has not been decided.
- Current sources needed? Preliminary simulations show that a commercial in current limit mode could be sufficient.

- ATLAS would like to reuse existing cables
- More patch panels in the system
- All power supplies in service cavern.
- In communication with WIENER to design commercial PS.





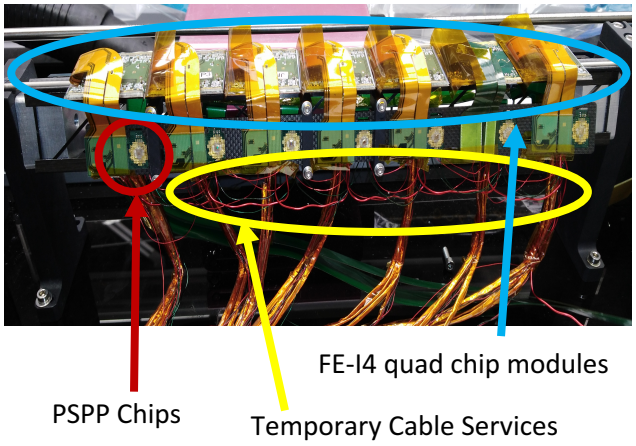
ITAINNOVA
Current source prototype:

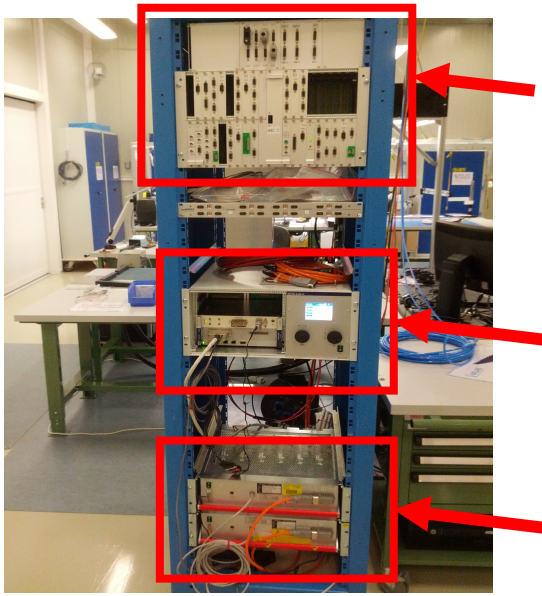


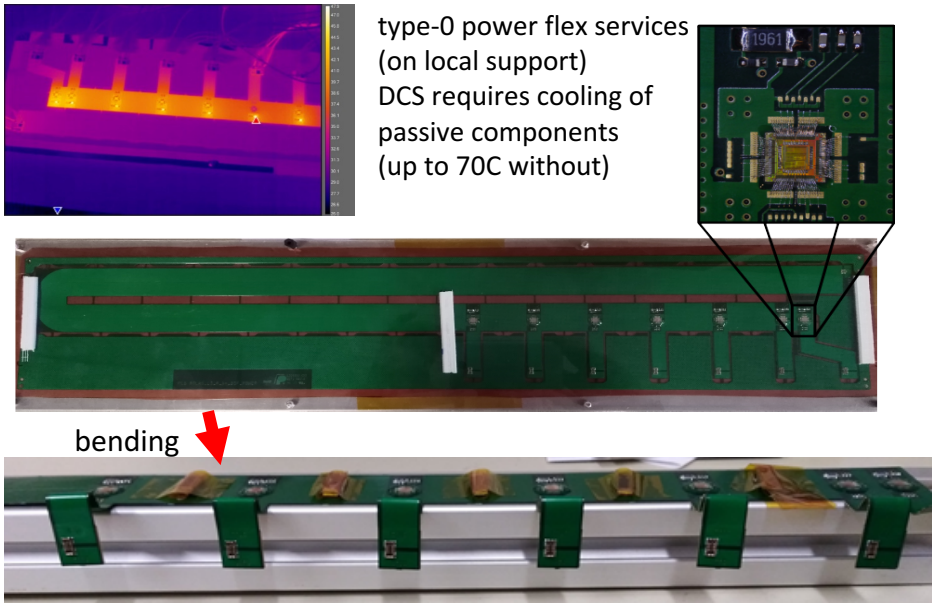
INFN Firenze/CAEN
Current source prototype:

ATLAS system tests with FEi4s

- Long SP chain with 13 FE-I4 quad modules being tested in Liverpool
- Full scale demonstrator project with thermal and electrical prototypes for the outer barrel started end of 2016 using:
  - FE-I4 modules, PSPP prototype chips, type-0 services prototypes, realistic power supplies, DCS, interlock, long cables
- Short electrical prototype commissioned in 2018, full scale SP chain with 7 B-class modules running
- Qualification of ATLAS SP chain design with a long chain (16 modules) and multiple chains on single local support ongoing







Summary

- ✓Serial powering effort based on large collaborative effort!
- ✓Low noise system at the cost of operating at maximum current to absorb load variations

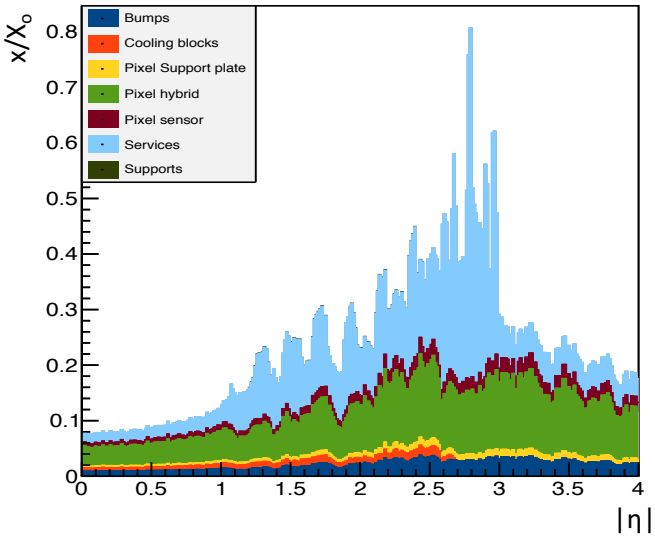
- ✓Enhanced Shunt-LDO for RD53A
  - ✓65nm CMOS technology & operational range up to 2.0A,2.0V
  - ✓Independent Shunt-LDOs per power domain
  - ✓Additional features for optimization of power efficiency and stability
- ✓Extensive simulations at chip, module, system level
- ✓Testing of RD53A Shunt-LDOs has shown very promising performance so far. Test-chip was hard to die.
- ✓New mini-ASIC will be submitted with improved features, bandgap scheme and protection.

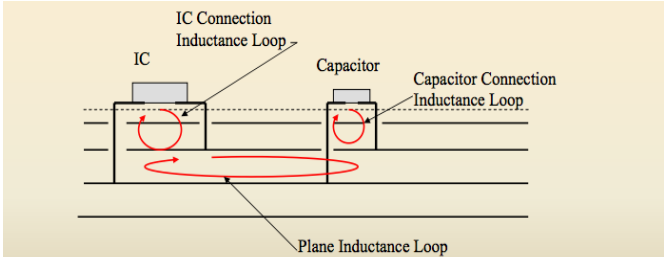
- ✓CMS and ATLAS have same very similar approaches to system aspects, except for
  - ✓the presence of the PSPP chip
  - ✓putting in parallel modules choice
  - ✓CMS pixel detector is accessible & repairable
- ✓Long list of system tests to come now that chips and assemblies will be available.

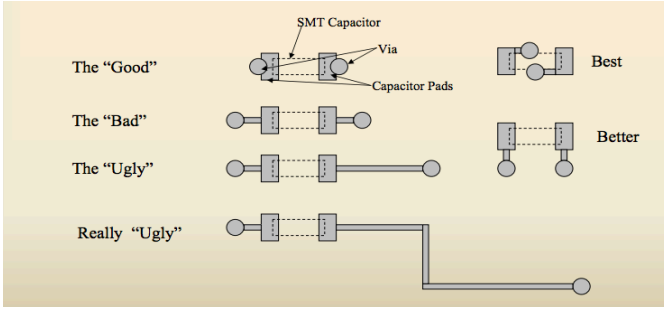
CMS IT module material budget &SLDO

- Material budget: the hybrids should be optimised.
- **Copper** planes dominating the hybrid weight BUT it is crucial for an efficient placement of the decoupling capacitors with small inductance loops.
  - Ground plane should be used from decoupling capacitors
  - Vias should be optimized
- **Capacitors** play an important role in the material budget of the module but cannot live w/o them..

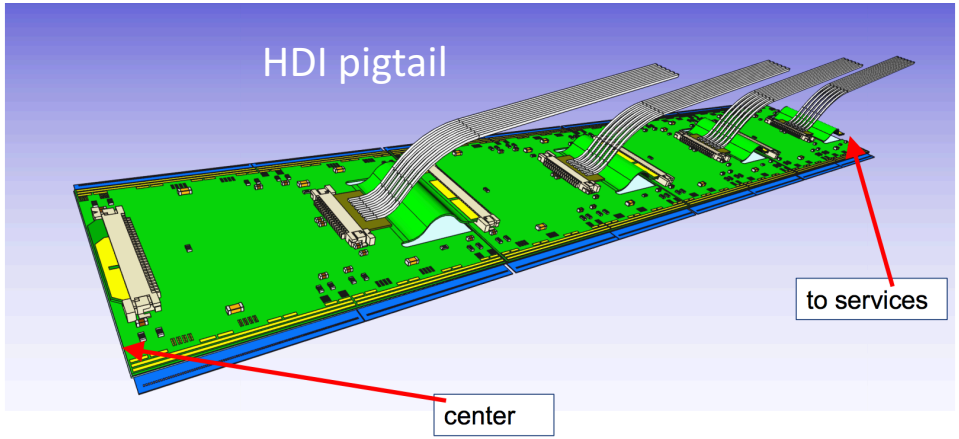
  SMD capacitors placement close to the pixel chip
  - **Input capacitor**: 6uF per module => more efficient when splitted into 4x 1.5uF (one per chip)
  - **Output capacitor**: 2.2uF per chip MANDATORY for stable SLDO operation (R & D on cap-less design ongoing)
  - **Resistors** for offset/reference voltage: better integrated with e-fuses
  - **HV filtering**: to be defined after RD53A module tests

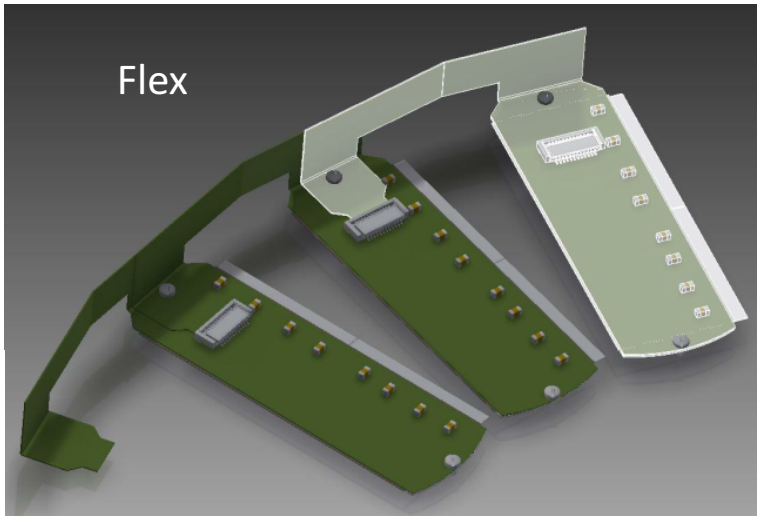


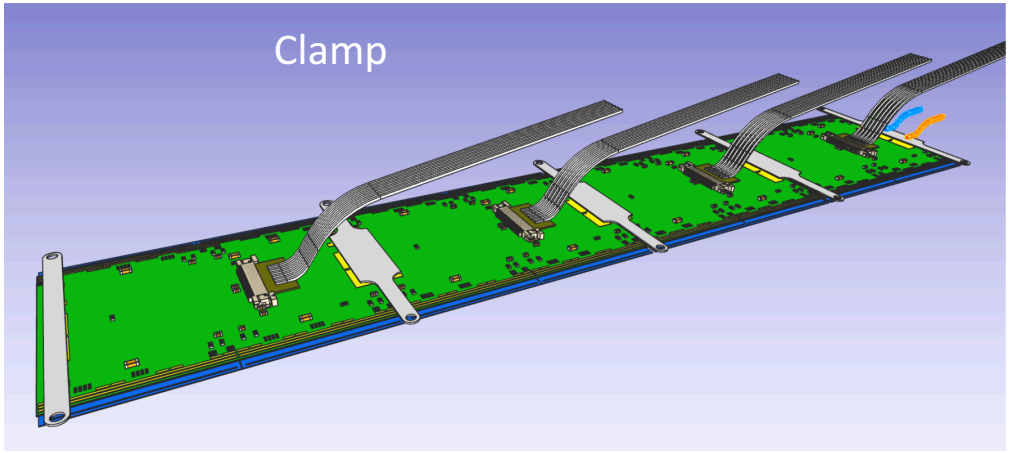




CMS IT serial powering connectors

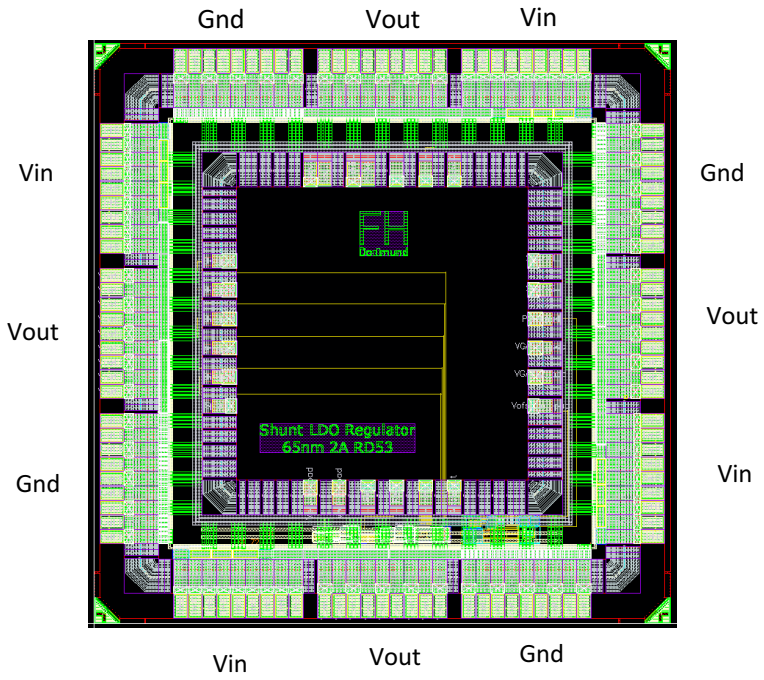






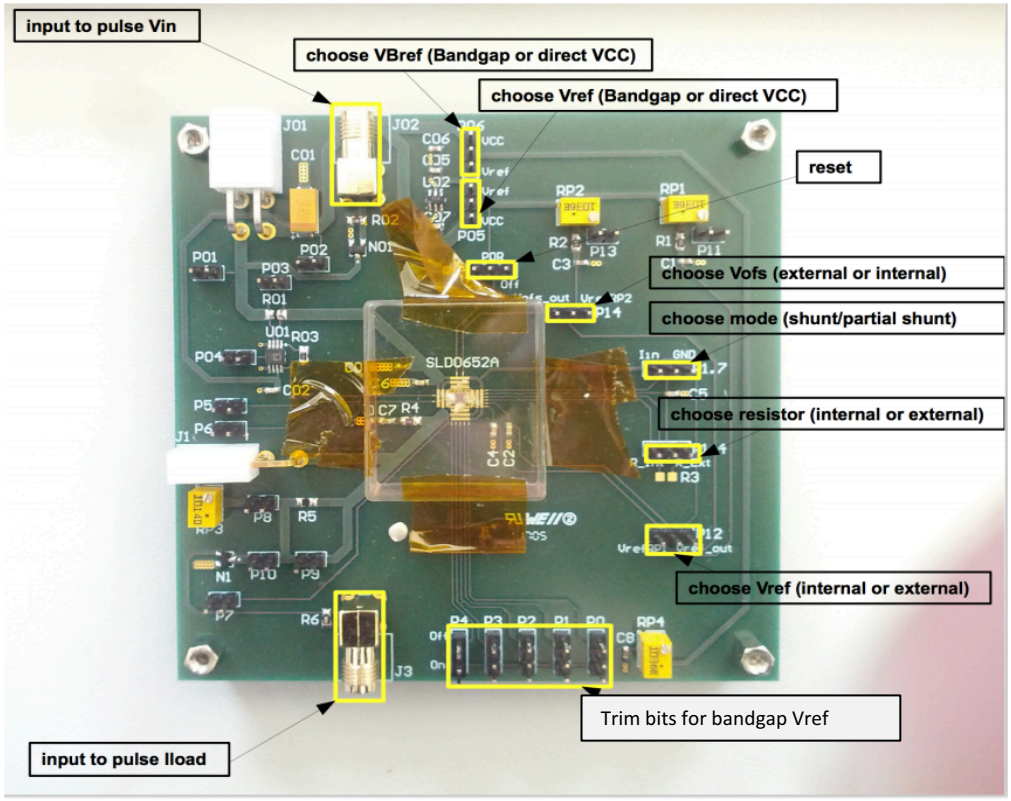
Shunt LDO 2.0A test-chip

- A 2.0A Shunt-LDO prototype chip has been tested in Shunt-LDO mode, where its characteristics have been investigated e.g. the effective resistance, the use of the configurable voltage and the coupling of the noise of chips operated in parallel and in series.



2A Prototype single regulator
Submitted October 19th 2016.

- Definable Offset Voltage
- Bandgap Integrated
- Trimmbits connected to analog pads
- Bandgap to SLDO connection established off chip
- Vout, Gnd Sense Pads



2.0A test-chip Shunt-LDO: 600 Mrad X-ray irradiation