# Serial powering testing with the 2.0A Shunt-LDO regulator of the RD53A pixel readout chip

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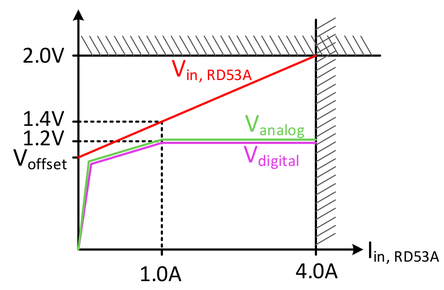
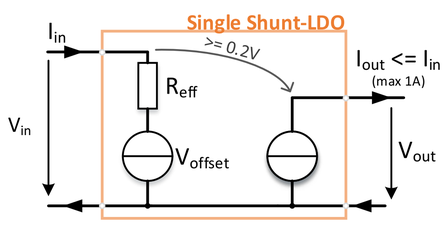
## 1. Introduction

- The HL-LHC ATLAS and CMS pixel detectors will be powered using a serial powering scheme.
- Constant current will be provided to a chain of pixel modules powered in series, whereas chips within a module will be powered in parallel.
- This scheme is based on the design of a Shunt-LDO regulator [1] that has been integrated on the new RD53A [2] prototype pixel readout chip.
- This poster shows first results of serial powering tests with the RD53A powered using the on-chip Shunt-LDO regulators and without sensors.

### RD53A

- 65 nm CMOS technology integrated circuit.
- Demonstrator for suitability of the RD53 pixel chip for HL-LHC pixel detectors' requirements.
- Large format, ~ half-size of the final pixel chip.
- Two independent on-chip integrated Shunt-LDO regulators provide the analog and digital supply voltages using a reference voltage and shunt any extra provided current.
- Each Shunt-LDO is dimensioned and integrated as in the full size pixel chip. It can take up to 2A and 2V.
- A dropout voltage of 0.2V is required for stable operation of the LDO. For an output voltage of 1.2V, a input voltage of 1.4V is required.

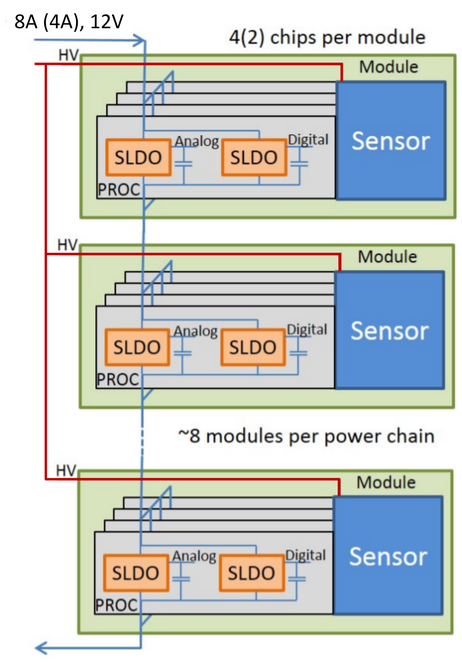



$V_{in} = R_{eff} * I_{in} + V_{offset}$
$V_{out} = 2 * V_{ref}$

### Shunt-LDO regulator parameters

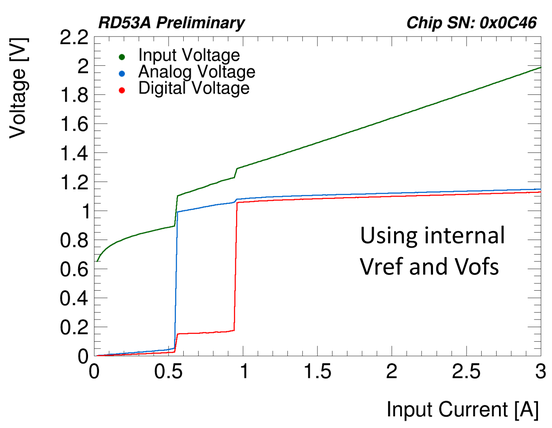
- The Shunt-LDO can be modeled as a resistor in series to a voltage source. This resistive behavior is critical for appropriate current sharing among parallel chips.
- The effective impedance is set by a resistor which together with the offset voltage defines the working point of the Shunt-LDO.
- The constant current provided must include a safety margin, referred to as headroom, to comply with power consumption variations.
- The reference and offset voltages are configurable and provided by on-chip integrated bandgaps. Overwriting with external voltages is possible.
- External decoupling capacitors (uF) are mandatory for LDO stability.

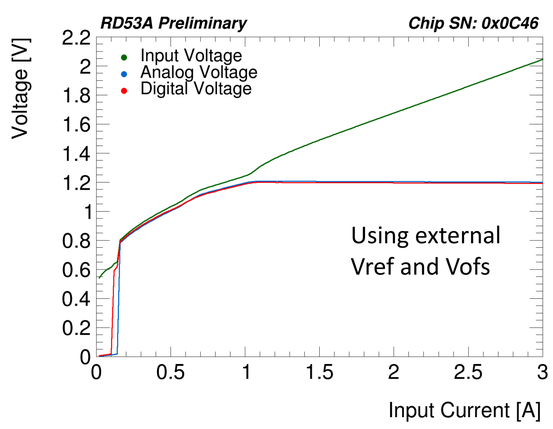



## 2. Single RD53A chip tests

### a) Line regulation

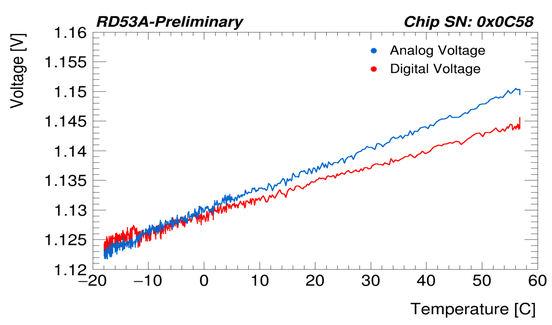
- The slope of the Vin is equivalent to the input impedance. Parasitic resistance can effect the input impedance: A slope offset of ~200mΩ was measured.
- Line regulation measurements were performed using the internal bandgaps for the offset and reference voltages (left plot) and when providing them externally (right plot).
- The line regulation behavior is dominated by the interaction of Shunt-LDO with the bandgap voltages.



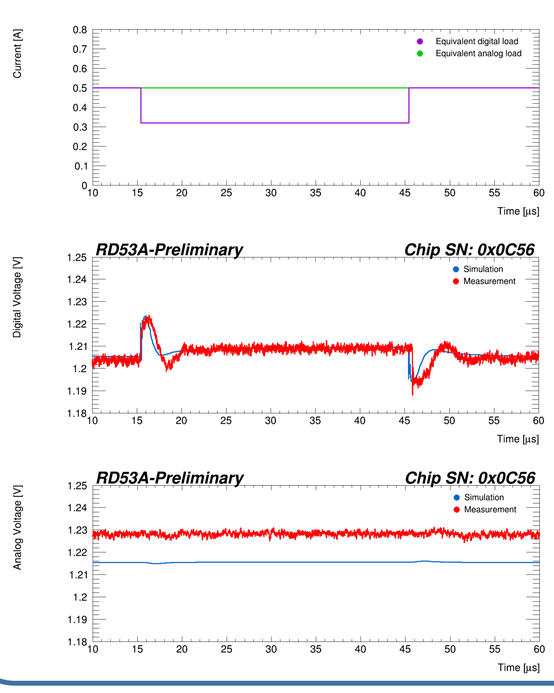

### b) Climatic chamber test

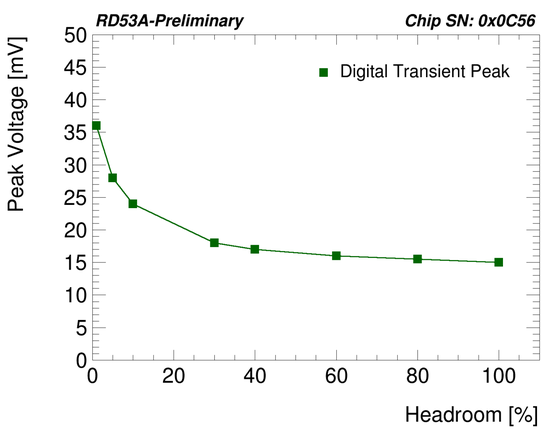
- Chip was tested in a climatic chamber, operated in Shunt-LDO mode with Iin = 2.2A and using internal bandgaps.
- The temperature was measured using NTC on carrier card.
- The Shunt-LDO output voltages change by ~20-25mV/80°C.




### c) Transient measurement

- Both digital and analog domains were configured to have ~0.5A consumption.
- Digital load transient was done by turning off/on the clock of a part of the pixel matrix.
- Impact of the transient to analog voltage is almost not visible (as expected by simulation).
- Decoupling capacitors used: Shared input Cin=20uF, per regulator output Cout=2.2uF.



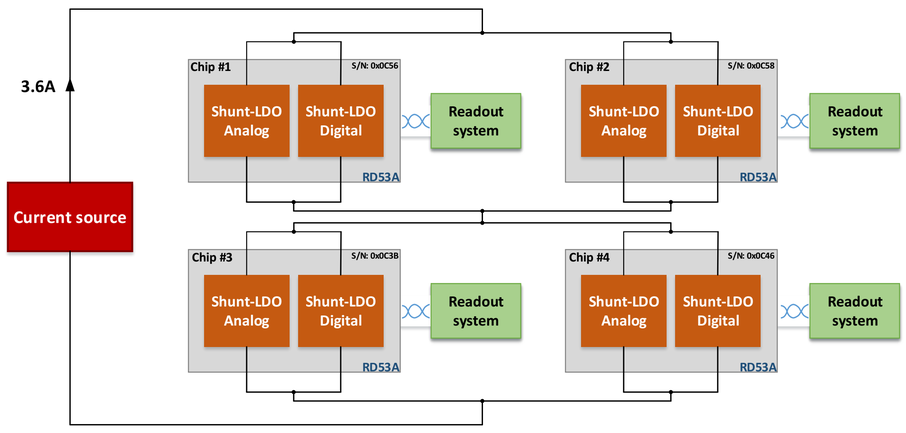




- Decreasing the current headroom, increases the transient peak as expected.
- The nominal value of 25% seems like a safe value that can possibly be decreased in the final system.

## 3. Serial power chain

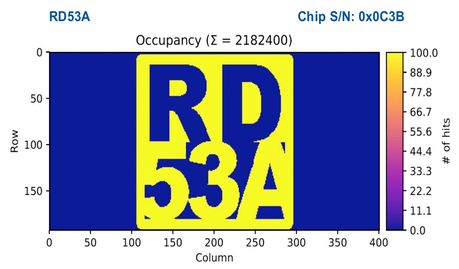
### a) Setup

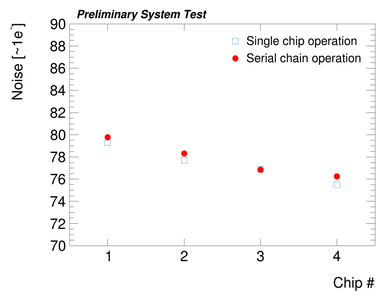
- First tests were done putting four chips in a serial power chain as depicted below.
- The chips were configured with the same Shunt-LDO parameters using internal bandgap offset and reference voltages and a constant current of 3.6A was provided to the chain.
- Four readout systems were used to communicate with the chips (not synchronized).




### b) Operating chips in a serial power chain

- Two tests were performed with all four chips at the same time:
  - Digital scans with a customized mask to assess functionality.
  - Threshold scans with the arbitrarily chosen, linear front end (UNTUNED) to a first study of the impact of power mode to noise levels.




- Example of a digital scan from one of the chips operated in the chain.
- No significant impact of serial powering to the noise levels of the chips was observed.

## 4. Summary & future work

- First serial powering results with the 2.0A Shunt-LDOs of the RD53A are shown.
- The Shunt-LDO works well. A comprehensive evaluation of its characteristics is ongoing.
- The line regulation behavior is dominated by bandgaps as expected from simulations.
- The RD53A chip can be fully operated in a serial chain using the Shunt-LDO with all the internal voltages provided by the bandgaps.

### Future work

- Further electrical characterization of the RD53A Shunt-LDO and reliability testing for radiation and temperature corner analysis.
- Transients and failure tests, studying the noise and failure propagation in a chain.
- System tests with pixel modules using large scale, detector-like assemblies to optimize the system parameters for reliable operation in the final system.

### References

**[1] M. Karagounis et al., "An integrated Shunt-LDO regulator for serial powered systems", *2009 Proceedings of ESSCIRC*, Athens, 2009, pp. 276-279**

**[2] RD53A collaboration, M. Garcia-Sciveres, "The RD53A Integrated Circuit", CERN-RD53-PUB-17-001**

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