The ITk Strips Powerboard (v2) For The ATLAS Barrel

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Introduction

The upgrade of the ATLAS silicone strip detector, the Inner Tracker (ITk) Strip detector[1], for the HL-LHC will employ a powering scheme where a **single power supply provides power to several modules in parallel**. This includes both the high voltage to bias the sensor and the low voltage to power the on-module electronics. The low voltage is supplied to the supporting stave structure using an external 10-11V. The power of a single module will be managed using a custom electronics board called the Powerboard.

The Powerboard v2 has **four main functionalities**

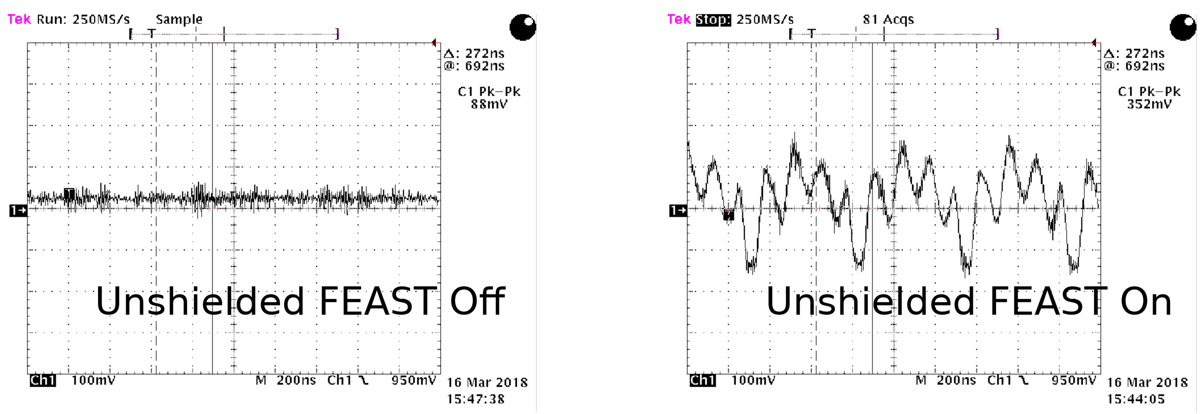
- use FEAST2.1 to step low voltage from 11V to 1.5V for the on-module power,
- monitor the low and high voltage currents directly on a module,
- disable power in case of module failure,
- and monitor the local temperature.

The last three tasks are accomplished using a custom ASIC called the Autonomous Monitor And Control (AMAC) chip.

This poster will contains the design of the **second version (prototype) of the Powerboard** aimed at barrel modules, initial results of the monitoring functionality and summarize the plans for scaling up the the production of the full ~10,000 Powerboards required for the ITk Strip upgrade.

Shield Box

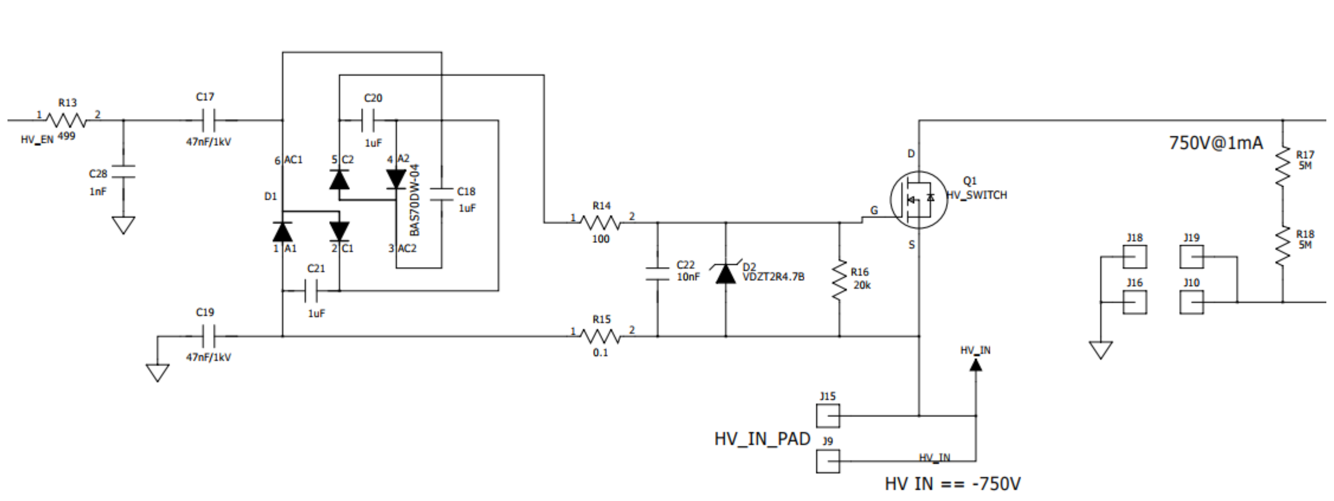
A **tin-coated aluminium shield box** is soldered with a continious seam to the Powerboard to block the noise induced by the coil.



Shield box performance can be tested by measuring the noise on a coil placed below the Powerboard (above).

HVMux and Voltage Multiplier

The Powerboard contains a **rad-hard GaN FET** that acts as a switch for the sensor high voltage bias (HVmux). It is **rated to 500V**, plus a safety margin. The gate voltage for changing the FET to ON state is higher than the AMAC can output. Instead the AMAC outputs a clock signal with a tunable 0-100 kHz frequnecy and a 3V amplitude. It is fed into quad voltage multiplier circuit.



Mass Testing Plans

The Powerboard V3 (production) will be **tested in the industry**. A prototype of the mass test system is being designed for the Powerboard v2.

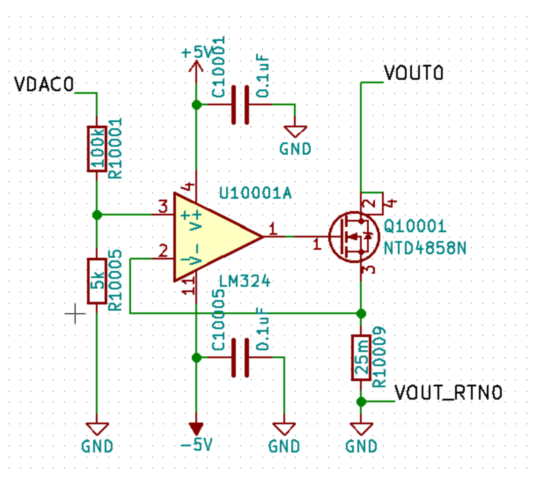
The goal is to have a carrier card for **~30 Powerboards** that can handle

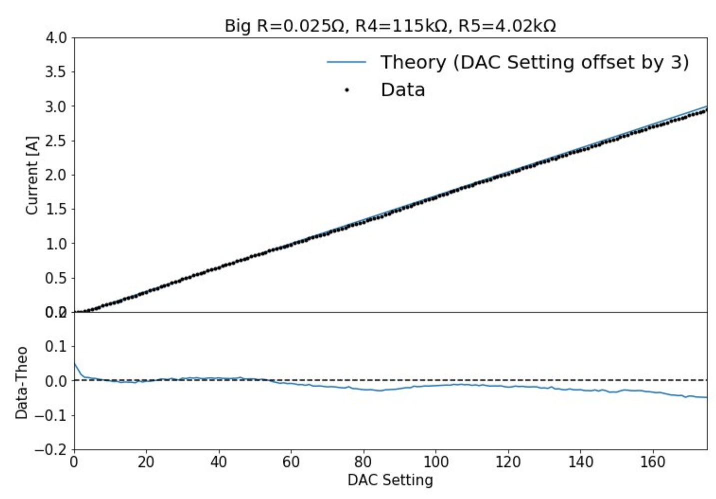
Wirebonding
- Holes connecting to a vacuum system placed underneath bonding pads

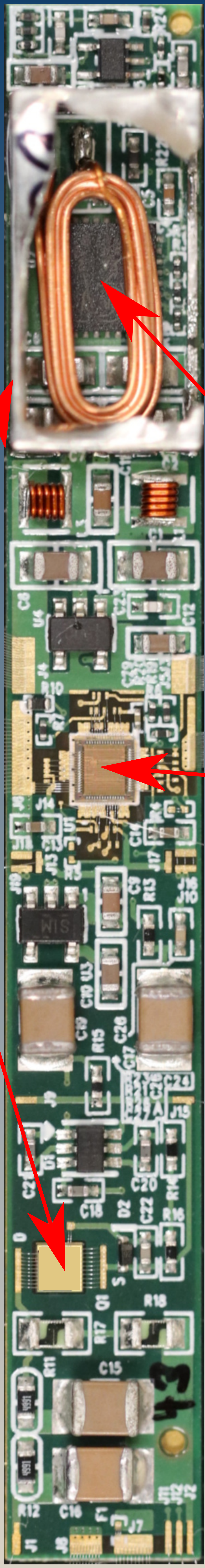
Electrical Tests
- The (passive) carrier card will be connected to an active card
- MicroZed Zynq (FPGA+SoC) board used for control
- Active board contains ADCs for PB output voltages and a variable load for LV

Transport
- 3D printed bar presses down on the Powerboards for long term attachement
- Allows module building sites to test the PB after transport

An custom variable load is being designed to test the DCDC converter efficiency at currents in the range from ~100 mA to 4 A. It will be easily replicable.

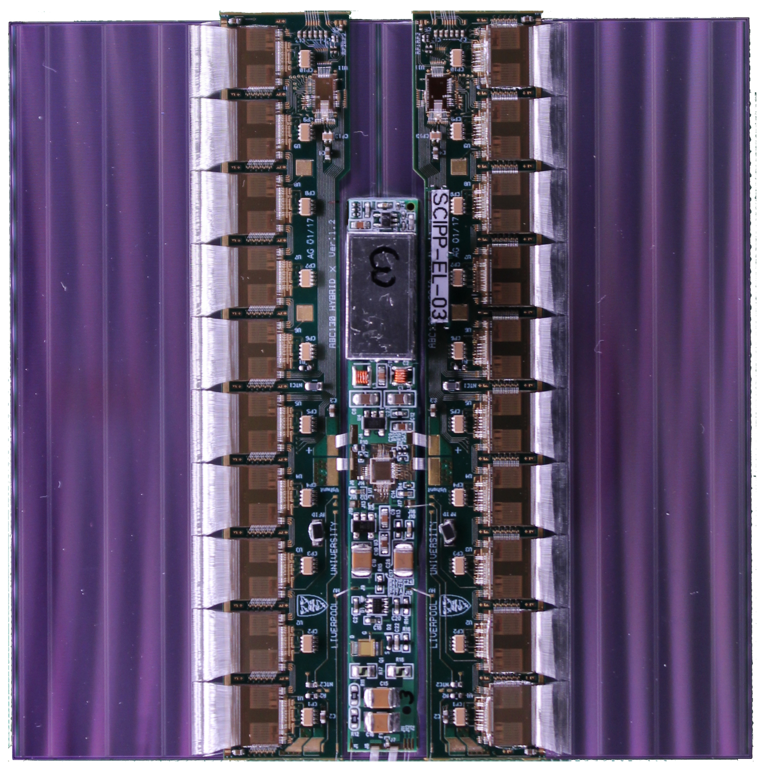






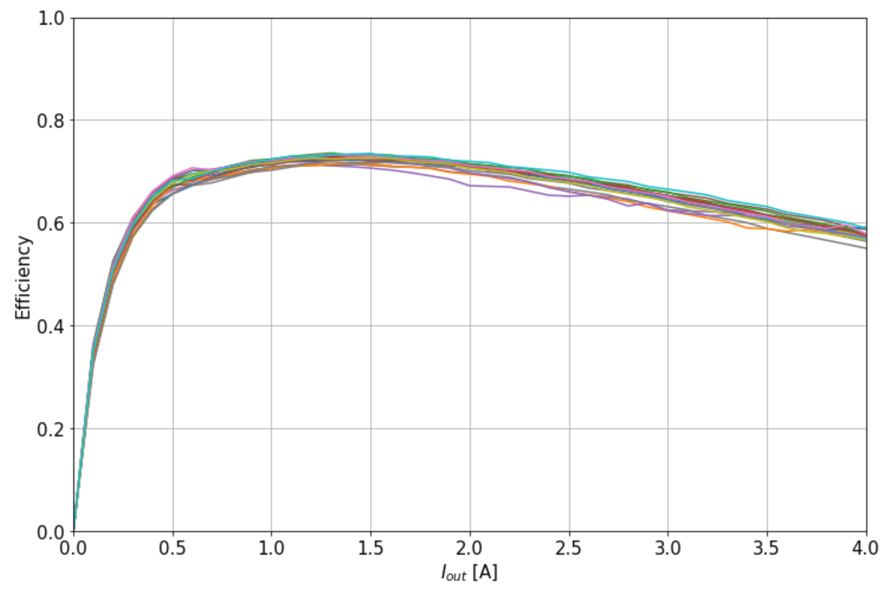
ITk Strips Module

The ITk Strips module[2] consists of a silicon sensor, two PCBs containing the readout electronics (aka "hybrids") and a Powerboard in the middle.



DCDC Converter

The **FEAST2.1**[3] is a **rad-hard swiching DCDC regulator** developed by CERN. It is responsible for converting the 11V Low Voltage input to 1.5V required by the on-module electronics. It uses a solenoid air coil designed at Yale.



The **efficiency** of the DCDC converter is around **70% at the expected 2A** load current.

Autonomous Monitor and Control

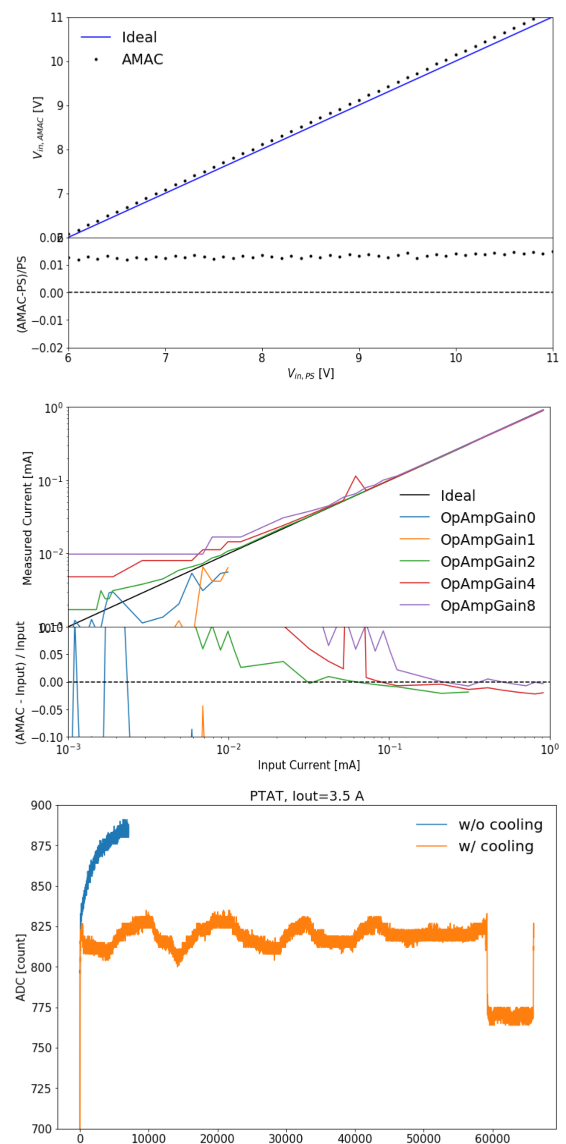
The functionality is controlled using the Autonomous Monitor and Control (AMACv1a) ASIC provided by University of Pennsylvania.

The Control Tasks
- Binary signal to enable LV output
- Clock signal to charge a voltage multiplier for HVMux enable signal

The Monitoring Tasks
- Input and output LV levels
- LV output current
- HV Leakage current
- bPOL12V, AMAC and PB Temperatures
- bPOL12V status (PGOOD)
- AMAC input voltage and internal LDO
- Internal bandgap reference voltage

The AMAC contains interlock functionality to disable power output if any of the monitoring channels that exceed a programmable treshhold.

Communication with the AMACv1a is accomplished using I^2C.

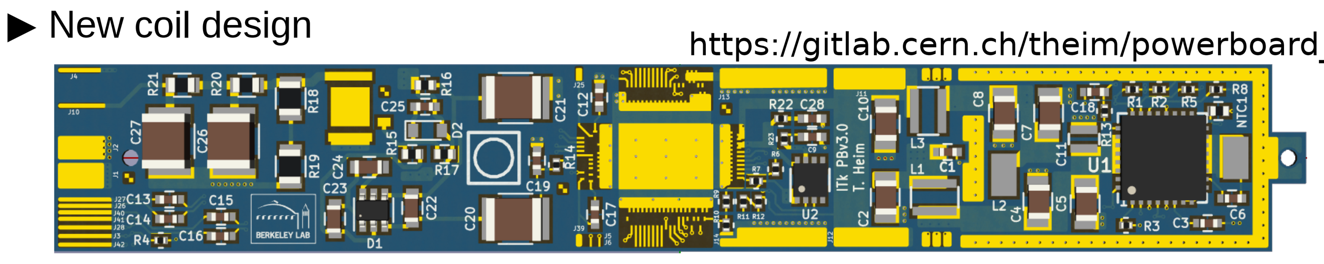


Towards Powerboard V3

The next version of the Powerboard is being designed. It will act as a base for the production version. The main changes are

- Support for updated version of the chips (AMACv2, bPOL12V)
- Rad-hard LDO for the AMAC (linPOL12V)
- Shhh functionliaty for adjacent modules
- Current measurement circuit moved into AMAC
- Improved input (NEW) and output current shunts
- Control and calibration signals to hybrid chip LDOs
- New coil design

https://gitlab.cern.ch/theim/powerboard_v3



References:

[1] "Technical Design Report for the ATLAS Inner Tracker Strip Detector", *The ATLAS Collaboration, 2017*
[2] "ATLAS ITk Short-Strip Stave Prototype Module with Integrated DCDC Powering and Control", *A.Greenall (Liverpool), 2017*
[3] "FEAST 2.1 Datasheet", *http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEAST2.1%20datasheet.pdf*
[3] "HVMUX, a high voltage multiplexing for the ATLAS Tracker upgrade", *E.Giulio Villani (Rutherford) et al.. 2017.*