AM07: Characterization of the Novel Associative Memory Chip Prototype Designed in 28 nm CMOS Technology for High Energy Physics and Interdisciplinary Applications

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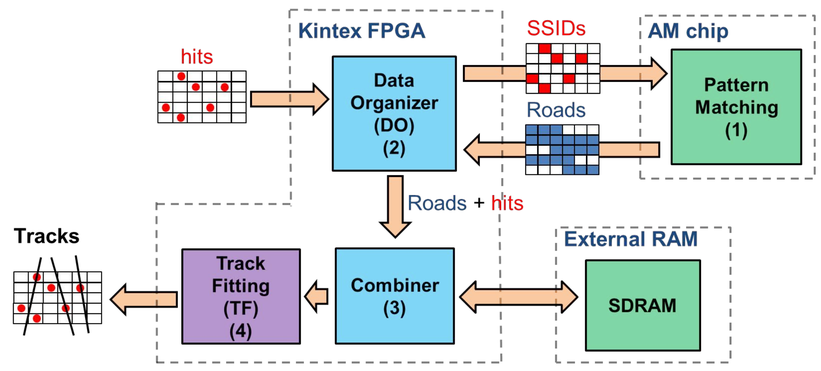
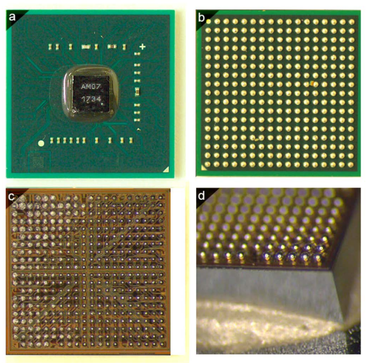
Introduction

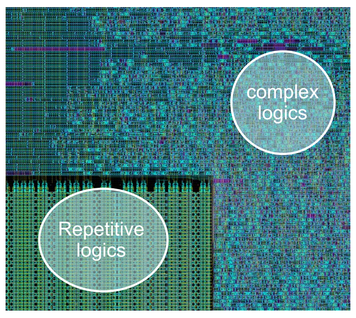
- At High Luminosity LHC ($5 \cdot 10^{34}$ cm^{-2} s^{-1}), the number of interactions per bunch crossing will increase to 140 (and up to 200), and the **trigger challenges** due to the high pileup will be insurmountable with the current systems:
  - Silicon-based tracking information is one of the most effective way for pileup mitigation. If it can be made available to hardware trigger and elaborated within the required **latency O(microseconds)**;
  - A dedicated **hardware processor** has been proposed in ATLAS (HTT) and CMS to be used in the trigger to select interesting events in real time.
- The reconstruction of the tracker tracks at first-level trigger can be fulfilled using **dedicated ASIC,** which exploits the computational power of the **Associative Memories (AM)** as it has been done for ATLAS (FTK) and CDF experiments;
- Benefits of having a dedicate ASIC are the low **cost/computational power** ratio and the high **energy consumption efficiency**, which can be exploited in non-HEP as well;
- We characterized a 28nm AM ASIC (AM07) with novel custom cells, a fast way of data transmission, and the 28nm CMOS ASIC design (first known attempt in HEP).



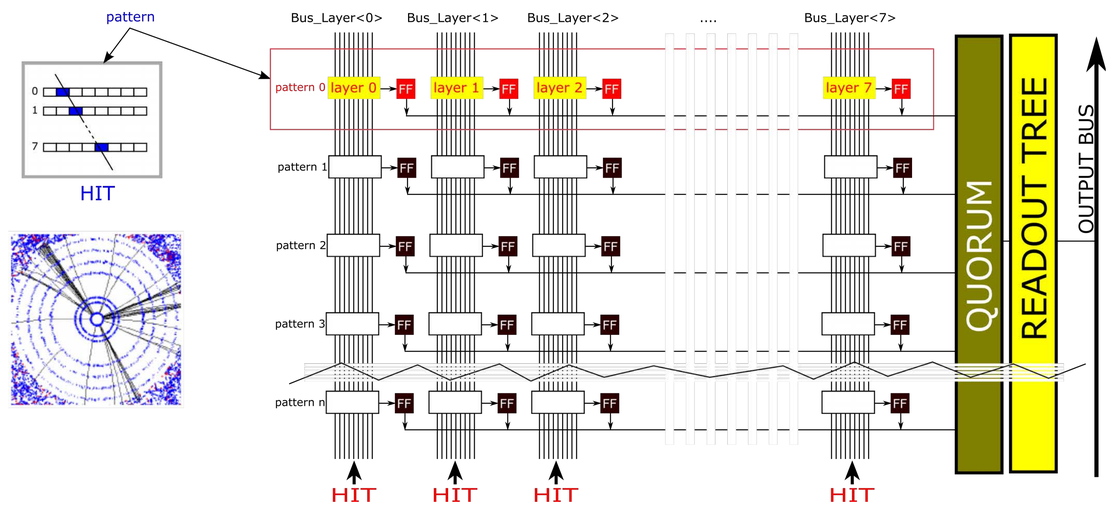
The AM07 ASIC

- The AM ASIC provides highly parallelized and **fast pattern recognition**;
- In 2015 the first AM06 production chip was released. AM06 was manufactured in 65nm CMOS technology (128kpatterns);
- We estimate that the HL-LHC AM ASIC should have to be denser by a factor of 3 with respect to the AM06. To comply with this, the AM07 is designed in an advanced 28nm CMOS technology;
- **Custom memory cells: two DOXORAM blocks and two KOXORAM blocks**, each containing 4×1024 patterns operating at up to 200 MHz;
- Ideal for HEP applications. Other applications (DNA sequencing, fast image analysis) are investigated.





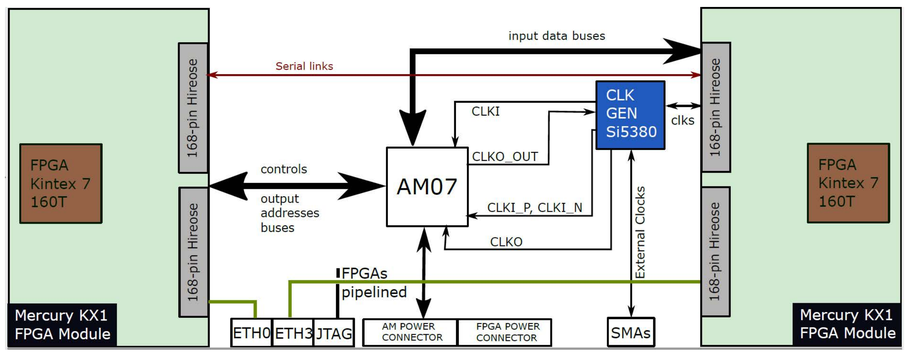
Associative Memory: operating principles

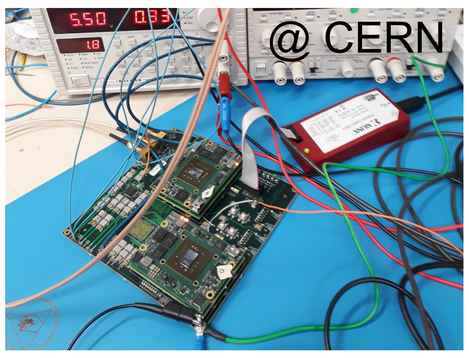


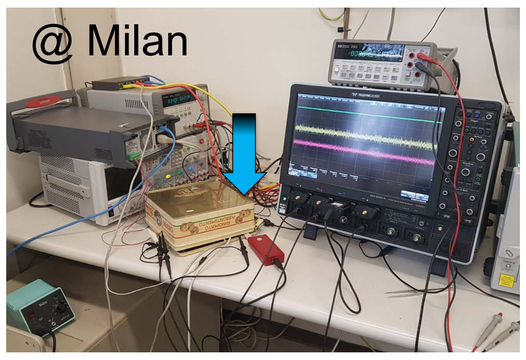
- AM compares its own content with all data received. If it matches, a memory is set (FF);
- The partial matches go through the quorum and to the threshold logic;
- A readout encoder sorts the matched patterns out.

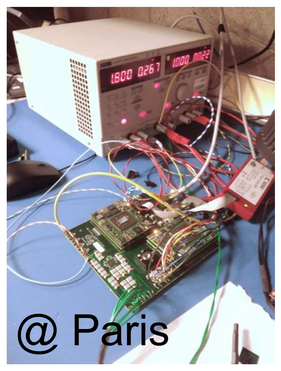
The AM07 Test stand

Three testing sites: CERN, Milan, Paris





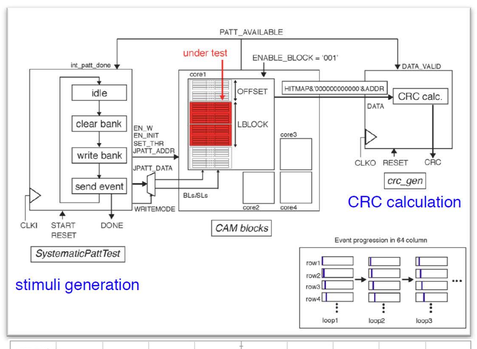


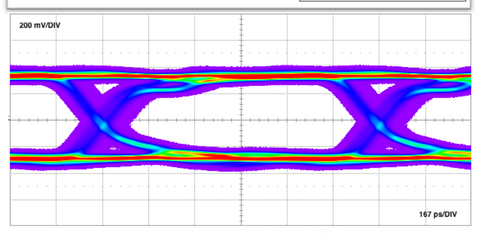


Results

The main goals of the characterization of AM07 is the 28nm design; the custom cells (DOXORAM, KOXORAM) design and power consumption; the custom LVDS drivers.

- The operation of the internal **AM banks were tested using a Built In Self-Test** (BIST) which writes the banks and test each pattern, outputting a CRC code summing up the results of the test;
- **LVDS drivers and receivers** have been measured with good results up to 1.1 Gbit/s. Power dissipation (TX+RX) is about 8 mW at 1 Gbit/s;
- Leakage current was measured without clock signals in the idle state:
  - 1.21 mA in Milano, 4.1 mA in Paris;
- **KOXORAM and DOXORAM power consumption was measured**. Results at 184.32 MHz are as expected in the simulations: DOXORAM consumes 0.832 fJ/bit versus 0.91 fJ/bit in simulation, KOXORAM consumes 0.684 fJ/bit versus 0.69 fJ/bit in simulation;
- **Pattern matching** using hits sent via LVDS links was successful;
- Compared to the AM06 chip, the AM07 exhibits a **reduced power consumption** by a factor of 1.7 and a increased density by a factor of 2.9;
- **LVDS driver, AM custom cells, and the overall logic are properly working. Custom-memory cell power consumption is in agreement with the simulations.**
- Further tests are ongoing.





SHMOO PLOT SHOWING THE WORKING FREQUENCY LIMIT IN MEGAHERTZ

I/O supply [V] \ Core supply [V]	0.65	0.75	0.85	0.95	1.00	1.05	1.10
2.0	fail	fail	105	184	245	245	245
1.9	fail	fail	105	184	245	245	245
1.8	fail	fail	105	184	245	245	245
1.7	fail	fail	105	184	245	245	245
1.6	fail	fail	105	184	245	245	245
1.5	fail	fail	105	184	245	245	245
1.4	fail	fail	105	184	245	245	245

CURRENT CONSUMPTION DUE TO THE CLOCK PROPAGATION FROM THE EXTERNAL PIN TO THE INTERFACE OF EVERY CORE

Frequency [MHz]	Current consumption [A] Paris	Milano
35.11	$5.89 \cdot 10^{-3}$	$2.63 \cdot 10^{-3}$
105.32	$1.08 \cdot 10^{-2}$	$7.90 \cdot 10^{-3}$
147.46	$1.40 \cdot 10^{-2}$	$1.08 \cdot 10^{-2}$
184.32	$1.68 \cdot 10^{-2}$	$1.40 \cdot 10^{-2}$
245.76	$2.08 \cdot 10^{-2}$	$1.80 \cdot 10^{-2}$

CURRENT/ENERGY CONSUMPTION VS CELL TECHNOLOGY

		meas [A] Paris	Milano	# bits involved	average meas [fJ/comp/bit]	sim [fJ/comp/bit] Calibre	%
DOXORAM	Baseline	4.26E-02	3.94E-02	589824	0.362		
	Activity on 1/8 input buses	5.36E-02	5.07E-02	589824			
	Δ (Activity on 1/8 input buses)	1.10E-02	1.13E-02	73728	0.832	0.91	91%
	Δ (Activity on whole input buses)	1.31E-01	1.30E-01	589824	1.194		
KOXORAM	Baseline	4.14E-02	3.82E-02	589824	0.351		
	Activity on 1/8 input buses	5.03E-02	4.75E-02	589824			
	Δ (Activity on 1/8 input buses)	8.90E-03	9.30E-03	73728	0.684	0.69	99%
	Δ (Activity on whole input buses)	1.13E-01	1.13E-01	589824	1.036		
	KOXORAM vs DOXORAM				-0.147	-0.22	

REFERENCES

[1] A. Annovi, et al., *"A low-power and high-density Associative Memory in 28 nm CMOS technology"*, **DOI:** 10.1109/MOCAST.2017.7937632

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