Redesign of the ATLAS hadronic Tile Calorimeter read out link and control board (Daughterboard) for the Phase-2 upgrade heading towards the High Luminosity Large Hadron Collider.

(1) Introduction.

The High-Luminosity LHC (HL-LHC) will have an instantaneous luminosity of five times the nominal design value. For the ATLAS Hadronic Tile Calorimeter (TileCal) to meet the new challenges for trigger and data acquisition, considerable R&D has been carried out on the back-end and front-end electronics.

In the Phase II upgrade design, the 256 calorimeter modules are instrumented with 1024 read-out units (Minidrawers) (Figure 1), each with up to 12 photomultipliers (PMTs). Each Minidrawer includes a Main Board (MB) that performs calibration, signal shaping and digitization.

A control and readout link Daughterboard (DB) receives the digitized PMT data from the MB, and communicates through multi-Gb/s optical links with the Tile Pre-processor (TilePPr) at the off-detector systems. The DB provides LHC synchronized timing, configuration and control to the front-end, and continuous readout of all the Mainboard (MB) channels to the back-end.

We present the DB revision 5 design and the results from the TID radiation tests performed.

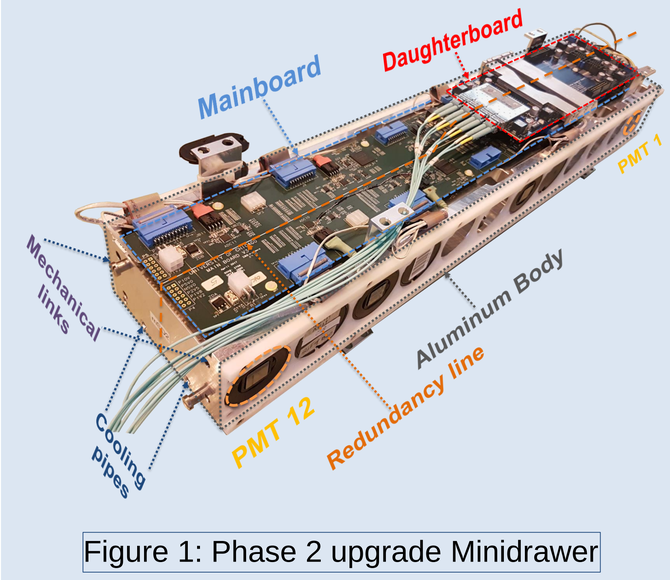


Figure 1: Phase 2 upgrade Minidrawer

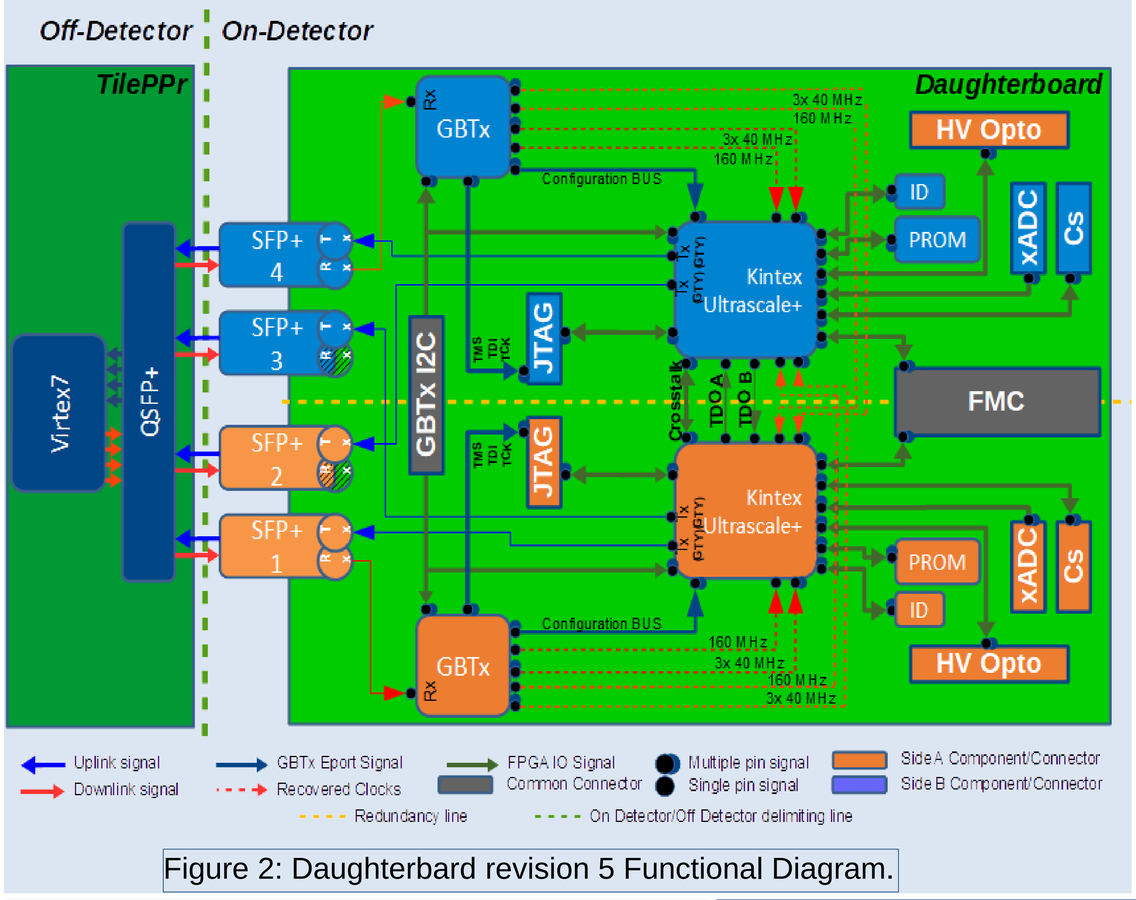
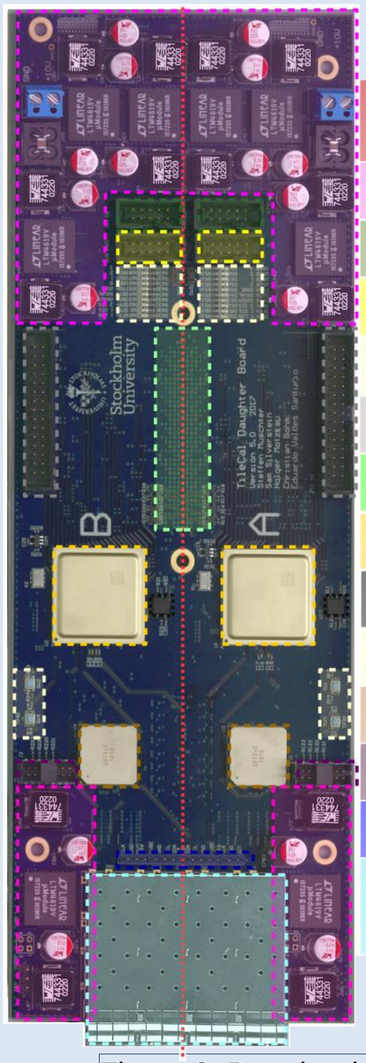


Figure 2: Daughterbard revision 5 Functional Diagram.

(2) DB Revision 5 design (figure 2).

- Double Redundant design that allows nominal running with either one or two working links.
- Migration from Kintex-7 (GTX transceivers) to Kintex Ultrascale+ (GTY transceivers) to improve radiation tolerance[3] and the handling of 9.6 Gbps transmission.
- Backward compatible with legacy HV-OPTO, FMC and Cs interface options[2].
- New digital unique ID serial chip and xADC panel for extra sensor monitoring.
- Migration from 2x QSFP to 4x SFP+ servicing:
  - Two redundant input links to a pair GBTx modules for:
    - recovering 2x 160 MHz LHC synchronized clocks to drive both FPGAs transceivers,
    - recovering 6x 40 MHz TTC phase configurable clocks, 2 driving FPGAs relevant logic and 4 driving the digitizing blocks on each Minidrawer quadrant,
    - propagating configuration and control commands to both FPGAs through the EPorts via a configuration bus,
    - propagating remote FPGA resets and remote configuration of FPGAs and PROMs though the Eports by means of controlling both FPGAs JTAG chains (the TDO returning signal is transmitted from the opposite FPGA uplink.
  - Two pairs of redundant readout downlinks from the FPGAs powered with TMR capable firmware providing continuous GBT CRC protected words with two gains of digitized data and SC information to the back end via GTY transceivers.



- 2x independent sides (**Redundancy** line)
- Power circuitry.
- **2x Cs** interface (5V)
- **2x xADC** interfaces
- **10x** user/debug **LEDs**
- **2x HVOpto** interface
- **400 pin FMC**
- **2x Kintex Ultrascale+**
- **2x 48 bit ID chip**
- **4x User switches**
- **2x GBTx**
- **2x JTAG** interface
- **GBTx I2C** interface
- **4x SFPs** (2x RX – 4x TX)

Figure 3: Daughterboard revision 5.

(3) TID tests.

- A DB with functional firmware connected to a TilePPr was exposed to a total of 20 kRrad delivered by a 9 MeV electron beam (figure 4) in six doses over ~ 1 hr (figure 5a), following the ESCC-22900 standard[5]:
  - Level E of TID (20kRad/200Gy)
  - Standard Rate (Window 1)
    - 365 Rad(Si) / min @ 9 MeV
    - 381 Rad(Si) / min @ 12 MeV (T1a*)
- Between doses, the system was power cycled and FPGAs reconfigured from the PROMs.
- Currents monitored were constant over the full dose, apart from the GBTx which had a small but measurable current decrease over the 20 kRad exposure (figure 5b).
- Temperature and current monitoring showed no evidence of latch-up (figure 5c).
- Core FPGA voltages were extremely stable over entire irradiation period (figure 5d) .
- No component failures:
  - FPGAs, GBTx, PROMs,
  - Two types of SFP+ tested:
    - CORETEK CT-000NPP-SB1L-D (baseline),
    - AVAGO AFBR-709SMZ.

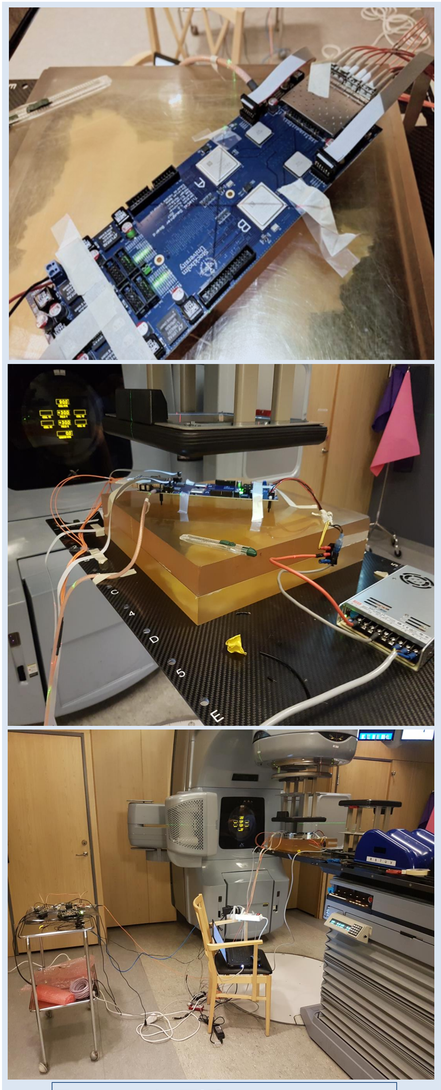


Figure 4: TID test setup.

Test steps	Delivered MU	Delivered Dose		Cumulative Dose	Energy
	[MU]	[Gy(Si)]	[kRad(Si)]	**[kRad(Si)]**	[MeV]
T1a*	180	1.14	0.114	**0.114**	12
T1b	2820	17.2	1.72	**1.83**	9
T2	6000	36.5	3.65	**5.48**	9
T3	9000	54.8	5.48	**10.96**	9
T4	8000	48.7	4.87	**15.83**	9
T5	6884	41.8	4.18	**20.00**	9

(a)

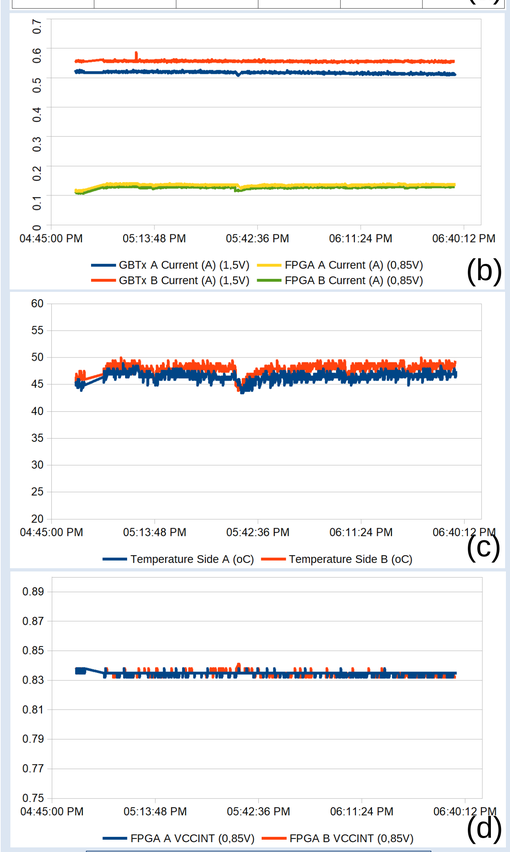


Figure 5: TID test Charts.

(4) Outlook.

The DB revision 5 meets the design and TID requirements for Phase II Upgrade. Currently, it is being integrated to the Minidrawers and firmware improvement is taking place. Radiation tests for NIEL and SEU are planed for May and September 2018 respectively. Near future plans include integrating it in the Extended Barrel to test in the May-June 2018 test beam campaign and electromagnetic tests that will take place in mid June 2018.

(5) References.

[1] I. Asensi. **Upgrade of the ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC.** EPJ Web Conf. Volume 170, 2018.

[2] S. Muschter *et al*. **Readout link and control board for the ATLAS Tile Calorimeter upgrade.** *DiVA: 805818*, 2015.

[3] H. Åkerstedt, **A radiation tolerant Data link board for the ATLAS Tile Cal upgrade,** *DiVA:921061*, 2016

[4] **GBTX Manual**, https://espace.cern.ch/GBTProject/GBTX/Manuals/gbtxManual.pdf, 2016.

[5] **TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD ESCC22900,** http://escies.org/escc-specs/published/22900.pdf, 2016.

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