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# Redesign of the ATLAS hadronic Tile Calorimeter read out link and control board (Daughterboard) for the Phase-2 upgrade heading towards the High Luminosity Large Hadron Collider.

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The Daughterboard (DB) interfaces the front-end and off-detector electronics. The newest revision migrated from two QSFPs to four SFP+ modules operating at: $4 \times 9.6$ *Gbps* uplinks handled by two Kintex Ultrascale+ FPGAs and $2 \times 4.8$ *Gbps* downlinks handled by two GBTxs. The DB provides continuous high-speed readout of digitized PMT samples through the uplink, and receives configuration, control and LHC synchronized timing through the downlink. TMR, FEC and CRC strategies, plus a double redundant design, aimed to virtually eliminate all possible single failure points and withstand damage from minimum ionizing and hadronic radiation, as well as single-event upsets.

## Summary

The R&D for the new on-detector electronics for the Phase-2 ATLAS upgrade heading towards the High Luminosity Large Hadron Collider (HL-LHC) has lead to progressive redesigns of the ATLAS hadronic Tile Calorimeter (TileCal) Daughterboard (DB). The DB is the read out link and control board that interfaces the front-end and off-detector electronics by means of multi-gigabit optic links. We present a redesign of the of the DB to its newest revision focusing on the main changes and specifications required for the ATLAS phase II upgrade. The DB revision 5 saves cost and complexity by migrating from two QSFPs to four SFP+ modules that operate: $4 \times 9.6$ *Gbps* uplinks handled by two re-programmable Kintex Ultrascale+ Field Programmable Gate Arrays (FPGAs) and $2 \times 4.8$ *Gbps* downlinks handled by two CERN-developed gigabit link application-specific integrated circuits (GBTx). After the upgrade, 1024 DBs will serve up to 12 photomultiplier tube (PMT) channels each, providing continuous high-speed readout of two gains of digitized PMT data samples to the off-detector through the uplink. Simultaneously, the downlink will provide the DB with configuration, control and timing so that the GBTx chips recover and distribute LHC synchronized phase configurable clocks to drive the FPGAs transceivers and to the ADC readout blocks. Moreover, the GBTx will drive a configuration bus that will propagate slow control commands to the FPGAs and allow remote access to the FPGAs JTAG chains and configuration flash memories. The Kintex 7 FPGAs were migrated to the new Kintex Ultrascale+ architecture, providing more radiation tolerance in addition to improved high-speed uplink timing by means of GTY transceivers. The new Ultrascale+ FPGAs will propagate clocks and configuration commands, while formatting the readout data to be sent off-detector. The DB revision 5 has a double redundant radiation tolerant design aimed to virtually eliminate all possible single failure points, in consequence only one downlink and two uplinks are required for nominal running. Giving the DB's position on the detector, it has to withstand radiation damage from minimum ionizing and hadronic radiation, as well as single-event upsets. Minimizing radiation-induced errors and enhanced data reliability is achieved by: implementing Triple Mode Redundancy (TMR) in the FPGA firmware, using Cyclic Redundancy Check (CRC) error verification in the redundant uplinks and adopting Forward Error Correction (FEC) in each GBTx in the downlinks.

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