The π-Lup board: functionality, performances and potential application.

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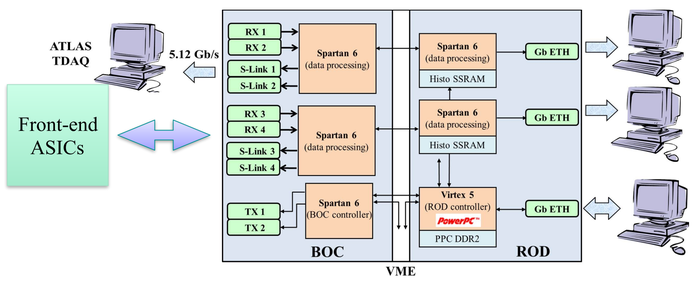
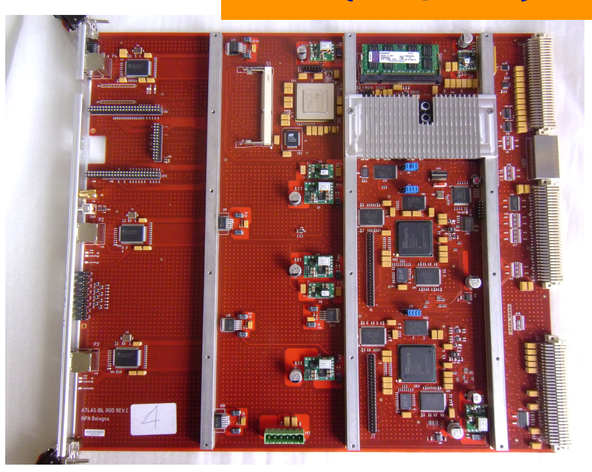
THE (RECENT) PAST

ROD cards For ATLAS Pixel (IBL, Layer-2, Layer-1, B-Layer and Disks)

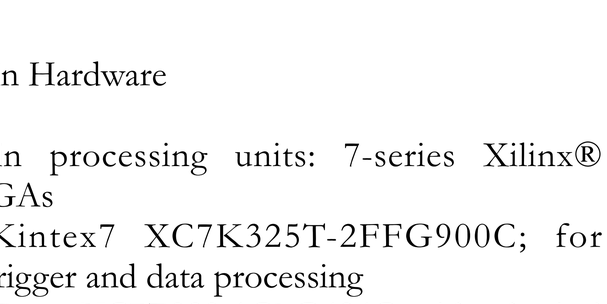




Over the last years the Bologna Division of I.N.F.N. and the Physics Department of the University of Bologna have collaborated to the ATLAS Pixel Detector upgrade designing the ROD (Read-Out-Driver) board for the off-detector read-out system. The ROD boards are mainly devoted to data formatting as well as detector configuration, calibration and triggering; about 100 RODs have been installed and are now in operation.

PixelROD board

As for the future upgrade of the Pixel Detector, new read-out electronics will have to face increased I/O bandwidth due to the new huge matrices of sensors that are foreseen to be installed.



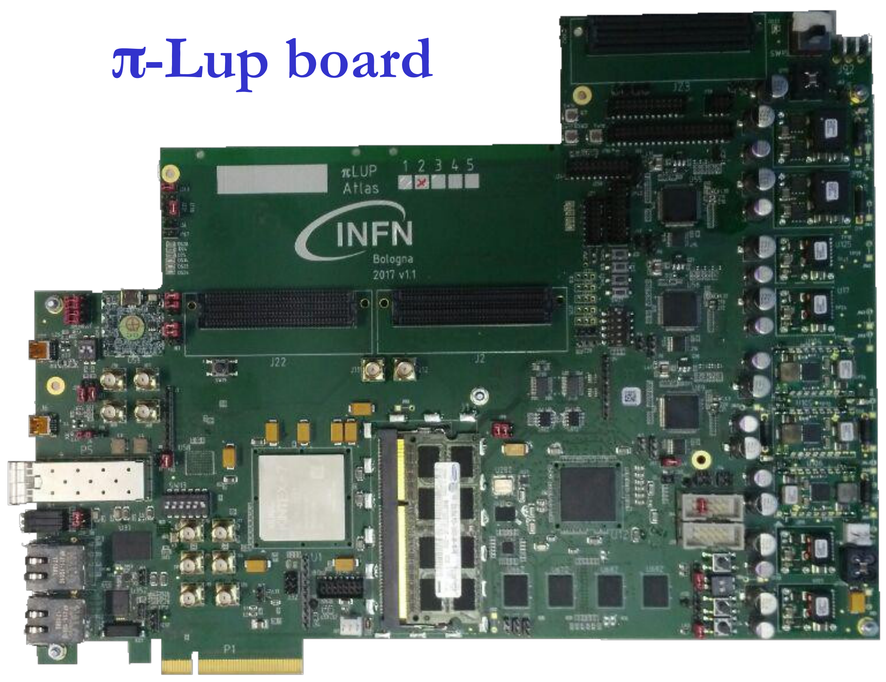
The experience gained from the ROD board production has led us to design an improved version of the ROD, called PixelROD, with plenty of potential application, even in the framework of the ATLAS TDAQ system.

THE PRESENT

- We are proposing the board as a tool to test, qualify and read out the recent front-end chips (and/or channels) which are under development at the present time in order to interface the new generation of pixel detectors, besides those for the LHC upgrade.
- We are favourable to extend the use of the board within other CERN-based collaborations.
- Case study for the implementation of neural networks aimed to track reconstruction (TimeSpot INFN Project).
- Several tests are performed in order to verify functionality and performances as well as to demonstrate potential use. As an example of tests, an 8-hour PCI-express DMA readout has been proved towards a PC mother board, with an overall BER < 10^{-15}. High speed links have been stressed and tested up to 10 Gb/s.

- The more up-to-date prototype, called π-Lup board, features a 8x PCI express Gen 2 bus and two Xilinx FPGAs: 1 Kintex7 and 1 Zynq with an embedded physical dual-core ARM Cortex-A9 processor.

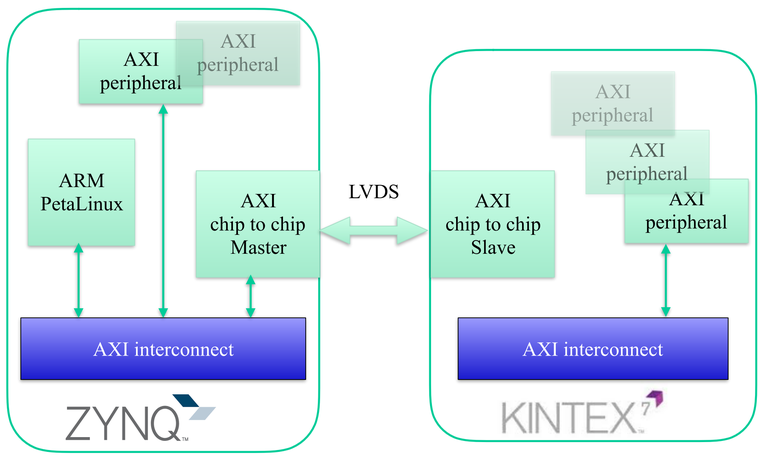
π-Lup board



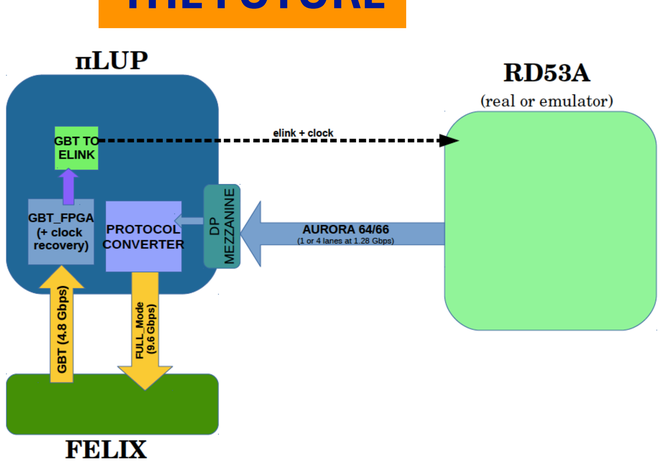
Main Hardware

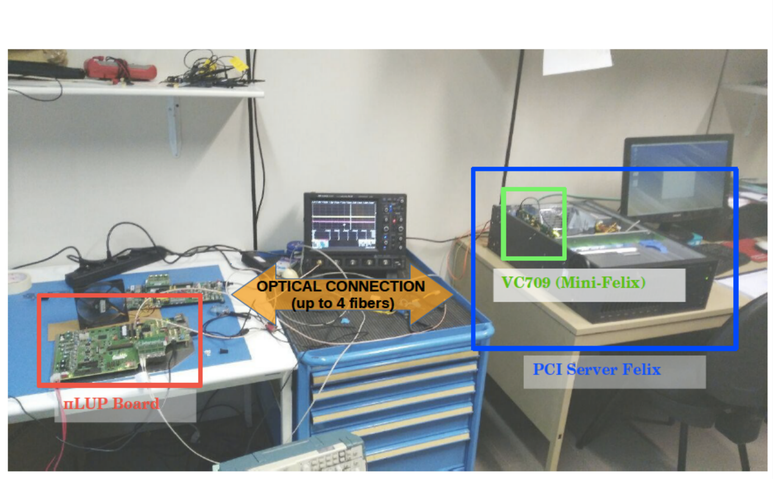
- Main processing units: 7-series Xilinx® FPGAs
  - ✓Kintex7 XC7K325T-2FFG900C; for trigger and data processing
  - ✓Zynq XC7Z020-1CLG484C with physical dual-core ARM Cortex-A9; for control and monitoring purposes
- High rate interfaces: 16 x GTX@ 12.5Gb/s on different physical ports (on Kintex)
  - ✓8 used to implement 1 x PCIe Express Gen2 8x-lane
  - ✓1 x SFP
  - ✓4 over FMS- HPC (400-pin) connectors
  - ✓4 overFMC- LPC (160-pin) connectors
  - ✓1 x Eth connector
  - ✓1 x SMA
- Memories:
  - ✓DDR3 2GB x 667 MHz (Kintex)
  - ✓DDR3 1GB x 667 MHz (Zynq)

THE FUTURE



Heavy effort on the firmware: developing a dedicated connection between the two FPGAs so that the custom logic being implemented into the Kintex7 can act as a peripheral of the Zynq's microprocessor, thus high performances in monitoring incoming/ outgoing data can be achieved.





As for a possible future application of the π-Lup board, we are developing an interface with a mini-FELIX card (Xilinx VC709) by establishing a communication through both GBT (4.8 Gb/s) and Full_Mode (9.6 Gb/s) protocols. In parallel, tests have been physically carried out at a rate of 4.8 GB/s using the 64b/66b Aurora protocol among two π-Lup boards. An achievable goal is to design with the π-Lup a "protocol converter" between the mini-FELIX and the new RD53A chips that will be used for the LHC upgrade. In order to accomplish that, further tests are currently in operation to interface the π-Lup with a RD53A chip emulator implemented on a second π-Lup device.