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The PiLup board: functionality, performances and potential application.

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The PiLup board has been designed by INFN and University of Bologna for a possible use in the framework of the ATLAS TDAQ system. As an improved version of the ROD for the ATLAS Pixel Read-out, it hosts two Xilinx FPGAs: A Kintex-7 featuring high throughput and heavy data-processing capability, and a Zynq-7000 equipped with an embedded System-On-Chip. The functionality and the performances of the more up-to-date prototype will be described. As an example of potential application, tests to interface a RD53 pixel emulator and the ATLAS Felix board will be shown.

Summary

Over the last years the Bologna Division of I.N.F.N. and the Physics Department of the University of Bologna have collaborated to the ATLAS Pixel Detector upgrade by designing the ROD (Read-Out-Driver) board for the off-detector read-out system. The ROD boards are mainly devoted to data formatting as well as detector configuration, calibration and triggering; about 100 RODs have been installed and are now in operation.
As for the future upgrade of the Pixel Detector, new read-out electronics will have to face increased I/O bandwidth due to the new huge matrices of sensors that are foreseen to be installed. The experience gained from the ROD board production has led us to design an improved version of the ROD, called PiLup, with plenty of potential application, even in the framework of the ATLAS TDAQ system.
The more up-to-date prototype of the PiLup board features a 8x PCI express Gen 2 bus and two Xilinx FPGAs: the Kintex7 XC7K325T-2FFG900C and the Zynq XC7Z020-1CLG484C with an embedded physical dual-core ARM Cortex-A9 processor. The Kintex7 device features 16 transceivers nominally running at up to 12 Gb/s; they are connected to different types of physical ports: 8 PCI_express, 4 HPC FMC, 1 LPC FMC, 1 SMA, 1 SFP and 1 Gb-Ethernet port. In addition the two Xilinx devices feature DDR3 external memories tested with read-write cycles at 667 MHz.
We are proposing the board as a tool to test, qualify and read out the recent front-end chips and/or channels under development and the present time, with the target to interface the new generation of pixel detectors, besides those for the LHC upgrade. We are planning to extend the use of the board within other CERN-based collaborations.
Several tests are performed in order to verify functionality and performances as well as to demonstrate potential use. As an example of tests, an 8-hour PCI-express DMA readout has been proved towards a PC mother board, with an overall bit-error-rate less than 10-15. In addition, heavy effort is on the firmware side too: for instance, we are developing a dedicated connection between the two FPGAs so that the custom logic being implemented into the Kintex7 can act as a peripheral of the Zynq's microprocessor, thus high performances in monitoring incoming/outgoing data can be achieved.
As for a possible future application of the PiLup board, we are developing an interface with a mini-FELIX card (Xilinx VC709) by establishing a communication through both GBT (4.8 Gb/s) and Full_Mode (9.6 Gb/s) protocols. In parallel, tests have been physically carried out at a rate of 4.8 GB/s using the 64b/66b Aurora protocol among two PiLup boards. An achievable goal is to design with the PiLup a "protocol converter"between the mini-FELIX and the new RD53A chips that will be used for the LHC upgrade. In order to accomplish that,

further tests are currently in operation to interface the PiLup with a RD53A chip emulator implemented on a second PiLUp device.

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