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Silicon photonic wavelength division multiplexed high-speed links

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We present our recent developments on an optical wavelength division multiplexed data transmission system. The nearly completed link demonstrator aims for a data rate of 4x10 Gb/s with the potential to scale the data rate up into the terabit-per-second range. Key component is a silicon-photonic chip with monolithically integrated, active and passive photonic components and circuits, whose characteristics will be shown.

Summary

Silicon photonics is the big promise for highly integrated high-speed links for future detectors. The essential components are silicon-based optical modulators, which have already proven their radiation hardness in several studies. We present our recent developments on an optical transmission system, where silicon-photonic modulators are integrated in the detector front-end while the light sources providing the optical carriers to encode data on are located off-detector. Each link consists of two optical fibers: one glass fiber connects the continuous-wave light source with the modulator and another fiber guides the modulated carrier to a receiver located in the counting room. While the modulators typically achieve a modulation bandwidth of up to 18 GHz, the electrical driver circuitry limits the data rate to around 10 Gb/s.
However, the data rate per fiber may be significantly increased by wavelength-division multiplexing (WDM), where several optical data signals at different wavelengths are modulated and transmitted over a single glass fiber. This multiplies the total link data rate by the number of parallel data signals and is well known in commercial telecommunication.
We developed a silicon-based WDM transmitter with four wavelength channels in the C-band around 1550 nm. Electrooptical modulators, optical multiplexers and demultiplexers are monolithically integrated on a single photonic chip, which is the key component of a nearly completed link demonstration system with a data rate of 4x10 Gb/s. By increasing the number of WDM channels, an aggregated data rate up to the terabit-per-second range is possible. Complex and data-intense network structures such as trigger architectures in large-scale detector systems can profit tremendously. Due to the high data rate, the read-out of most of the detector's raw data becomes feasible. Thus, the trigger architecture's complexity can be reduced significantly.
In this work, we present the design and measurement results of the transmitter sub-components. The steady-state characterization of modulators of our new system chip shows nicely working devices and a good RF performance at least similar to our former devices is expected, which exhibit a 3 dB cut-off frequency of up to 18 GHz. The wavelength multiplexers and demultiplexers have an average channel loss below 4 dB and the cross talk is less than -20 dB. This data indicates the designed WDM components match our requirements.

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