Monolithic Pixel Developments

ACES 2018 - Sixth Common
ATLAS CMS Electronics
Workshop for LHC Upgrades

Thanushan Kugathasan (CERN)

ALICE ITS upgrade collaboration
ATLAS ITK CMOS collaboration
CERN EP-ESE Microelectronics section
STREAM project
Hybrid pixels are used as tracking devices in the innermost layers of LHC experiments, sensor and ASIC are independent units

- Pixel sensors based on standard CMOS (Complementary Metal Oxide Semiconductor) process

- Separate optimization of sensor and FE-chip
- Fine pitch bump bonding to connect each pixel in the sensor to a readout cell in the ASIC (additional cost and limitation in size)
- Large sensor capacitance (~ 100 fF)
- Thick detector modules: ~ 300 µm sensor + ~ 250 µm sensor

**Challenge:**
integrate the sensors into the CMOS layer
Advantages of monolithic pixels in High Energy Physics:

- Detector assembly and production cost.
  - Standard CMOS processing (larger wafer diameter, low cost per area)
  - No need for cost intensive fine pitch bump bonding
- Better power-performance ratio for monolithic on the condition of better Q/C (cabling and cooling material reduction)
- Thin detectors (O(50 μm Si)) and high granularity (small pixel sizes)

<table>
<thead>
<tr>
<th>Required Time Res. [ns]</th>
<th>STAR RICH</th>
<th>ALICE-LHC</th>
<th>ILC</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>20,000</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>4</td>
<td>10</td>
<td>250</td>
</tr>
<tr>
<td>Non Ionizing Energy Loss Fluence [n_{eq}/cm²]</td>
<td>&gt; 10^{12}</td>
<td>&gt; 10^{13}</td>
<td>10^{12}</td>
</tr>
<tr>
<td>Total Ionizing Dose [Mrad]</td>
<td>0.2</td>
<td>0.7</td>
<td>0.4</td>
</tr>
</tbody>
</table>

MIMOSA28 (ULTIMATE)
IPHC Strasbourg
First MAPS system in HEP
0.35 μm CMOS
- Rolling shutter readout

ALPIDE - First MAPS in HEP with sparse readout similar to hybrid sensors
Reverse bias to increase depletion volume (-6 V)
the sensor is not fully depleted especially in between deep pwell and substrate

$w \propto \sqrt{\rho \cdot V}$
Power, Signal to Noise and Sensor Capacitance

Minimum Ionizing Particle (MIP) creates ~ 60 e/h pairs per micron of silicon traversed (in case of thin silicon)

For 25 um thick layer: 1500 e/h

<table>
<thead>
<tr>
<th></th>
<th>Diffusion</th>
<th>Drift</th>
</tr>
</thead>
<tbody>
<tr>
<td>Region</td>
<td>Non depleted</td>
<td>Depleted</td>
</tr>
<tr>
<td>Force</td>
<td>Charge carrier concentration gradient</td>
<td>Electric field</td>
</tr>
<tr>
<td>Collection time</td>
<td>&gt; 10 ns</td>
<td>&lt; 10 ns</td>
</tr>
<tr>
<td>Minority charge carrier path</td>
<td>Long</td>
<td>Short</td>
</tr>
</tbody>
</table>

Collection by drift advantages:
- Tolerance to non ionizing radiation (less trapping probability)
- Reduction of the cluster size (less charge sharing → more charge per pixel)

Front-end performance:
Fixing the Signal to Noise ratio for a given bandwidth, lower C/Q allows for a lower power

\[ P \propto \left( \frac{C}{Q} \right)^2 \]

C : sensor capacitance
Q : pixel charge
ALPIDE sensor for ALICE – Inner Tracking System

1.5 x 3.0 cm² 0.5 Mpix, high granularity (~30 x 30 μm²), thin sensor (50 μm)

G. Aglieri et al, DOI 10.1016/j.nima.2016.05.016

Outer Barrel Stave (98 chips ~100 M pixels)

ALPIDE is also used for the ALICE Muon Forward Tracker
Several experiments interested in using ALPIDE

Monolithic Pixel Developments - T. Kugathasan - ACES 2018 - CERN - 25/04/2018
**ALPIDE architecture**

- Analog front-end **continuously active** (40 nW/pixel)
  - analogue delay line (~2 μs peaking time)
  - Good threshold uniformity: $Q_{th} = (64.6 \pm 11.4)$ e-
  - Low noise: ENC = $(5.6 \pm 0.8)$ e-
- Global threshold for discrimination => binary pulse OUT_D
- Digital in-pixel circuitry with three hit storage registers (multi event buffer)
- Global shutter (STROBE) latches the discriminated hits in next available register triggered or continuous readout
- Zero suppressed readout, no hits no power
Sensitive area (4.12 cm$^2$) power density 6.2 mW/cm$^2$
Chip power density < 35 mW/cm$^2$
(20 mW/cm$^2$ with readout from parallel port)
ALPIDE – test beam performance

Large operational margin before and after irradiation up to 10 x lifetime NIEL
$(1.7 \times 10^{13} \text{n}_{\text{eq}}/\text{cm}^2)$
Towards more demanding applications

Specifications for the ATLAS Inner Tracker Upgrade Phase 2 (HL-LHC)

<table>
<thead>
<tr>
<th></th>
<th>ALICE-LHC</th>
<th>ATLAS-HL-LHC</th>
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<tbody>
<tr>
<td>Required Time Res. [ns]</td>
<td>20 000</td>
<td>25</td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>10</td>
<td>1000</td>
</tr>
<tr>
<td>Fluence [nₑq/cm²]</td>
<td>&gt;10¹³</td>
<td>10¹⁵</td>
</tr>
<tr>
<td>Ion. Dose [Mrad]</td>
<td>0.7</td>
<td>50</td>
</tr>
</tbody>
</table>

- **Time resolution**: fast collection by drift (<< 25 ns) ➔ larger depletion
- **High particle rate**: short dead time (< 1 us)
- **Tolerance to non-ionizing radiation (displacement damage)**:
  - fast collection by drift to decrease signal charge trapping probability ➔ larger depletion
- **High Q/C for power optimization**:
  - High Q: less charge sharing (small cluster) ➔ larger depletion
  - Low C: smaller junction capacitance ➔ larger depletion
Large collection electrode (HV-CMOS)

Approach to increase depletion: circuit inside the collection electrode
Traditionally called High Voltage CMOS technology

- Deep n-well collection electrode, risk of coupling circuit signals into input needs special attention (e.g., Current steered logic)
- Transistors isolated from the substrate (deep n-well)
- High reverse substrate voltage (~100 V)
- High resistivity p-substrate (>2 kΩ cm)
- Charge is collected by drift, good for radiation tolerance
- Limited circuit area, large capacitance (C > 100 fF)
Large collection electrode – LF Monopix

LF-Monopix is a demonstrator designed in LFoundry 150 nm HV-CMOS

LF Monopix

50 x 250 µm²

LFoundry 150 nm substrate ρ > 2 kΩcm

arXiv:1710.00074v1
T. Wang, Uni. Bonn

Column-drain architecture:
- Time stamp distributed in pixel array
- Hit information stored in the pixel (ToT)
- Hit read out following a priority scan

First measurements:
- $Q_{th}$ 2500 e⁻, ENC 200 e⁻
- No significant loss after irradiation (NIEL $2 \cdot 10^{15}$ n$_{eq}$/cm$^2$, TID 150 Mrad)

Efficiency

99.6 %

98.6 %

Efficiency

CERN

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Large collection electrode – ATLASPix1

AMS 0.18 um, first test on substrate \( \rho = 80 \, \Omega \, \text{cm} \)

AtlasPix1Simple:
- Column-drain architecture
- 25 \times 400 pixels, 130 \, \mu m \times 40 \, \mu m pitch
- 6 bit time-over-threshold

- Unirradiated sample
- Resolution consistent w/ pitch
- >99.5 \% efficiency
- Consistent results from multiple setups

\[
\text{HV} = -60 \, \text{V}
\]

(I. Peric, M. Kiehn)
Small collection electrode (modified CMOS Sensor process)

- Novel modified process developed in collaboration with the foundry (TJ)
- Adding a planar n-type layer significantly improves depletion under deep PWELL
- Possibility to achieve full depletion of the sensing volume
- No significant circuit or layout changes required
- Small collection electrode: low capacitance, lower power, less prone to coupling

W. Snoeys et al.
Fe$^{55}$ measurement before irradiation

Modified process:
Less charge spread over different pixels
More uniform time response

Note: circuit contributes significantly to the signal rise time
Measurements after irradiation

**90Sr source test (50 um x 50 um pixel)**

MPV = 19 mV pre-rad, 16 mV after $10^{15}$ n$_{eq}$/cm$^2$

σ = 1.96 ns pre-rad, 2.78 ns after $10^{15}$ n$_{eq}$/cm$^2$

Encouraging results on detection efficiency after irradiation ($10^{15}$ n$_{eq}$/cm$^2$)

H. Pernegger et al 2017 JINST 12 P06008
Small collection electrode demonstrators

- Measurement results show improved non-ionizing radiation tolerance for sensors manufactured using the modified process
- Analog front-end optimized for timing, based on ALPIDE

Design of two large scale demonstrators to match ATLAS specifications for outer pixel layers
Collaboration CERN – Uni. Bonn

The “MALTA” chip (2 x 2 cm²)
Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix

The “TJ-Monopix” chip (2 x 1 cm²)
Synchronous readout architecture.
Uses the well-established column drain readout architecture (experience from LF-Monopix design)
Low-power front-end based on ALPIDE front-end, optimized for timing (25 ns)
In pixel amplification and discrimination
Power consumption: 0.9 µW/pixel, ENC ~ 10 e⁻

Same front-end implemented in 2 chips:

MALTA
Clipping of the analog pulse duration
Analog information on time-walk
Binary data

TJ-Monopix
No-clipping, discriminated output duration for ToT
TJ Monopix

- 1 x 2cm² (1/2 of final size)
- 36 x 40µm² pixel size, 224 x 448 pixels
- 6-bit analog (charge) ToT information
- Column Drain architecture
- Low matrix power: ≅ 110 mW/cm²
  - Analog Power ≅ 50mW/cm²
  - BCID (clock) distribution: ≅ 60mW/cm²
  - Read-out power negligible (no current steered logic)
- High gain: 0.3 - 0.6 mV/e⁻ (due to the small C_d)

Q_{thr} = 230 e⁻
σ_{thr} = 22 e⁻

Low threshold dispersion, no in-pixel tuning
- No clock distribution over the pixel matrix – (power reduction of \( \cong 60\text{mW/cm}^2 \))
  - Analog power dominant < 70 mW/cm\(^2\)
- Pixel hit fast asynchronous transmission of the hits over high-speed buses to the end-of-column logic (programmable pulse duration 0.5 ns to 2.0 ns)
Signal from analog monitoring pixel
Good response after irradiation
• Charge collection time and front-end timing (< 25 ns) good after irradiation

\[ P_{\text{analog}} = 0.9 \ \mu\text{W/pixel} \]
Summary

ALICE – ITS Upgrade (LS2)
- ALPIDE - First MAPS in HEP with sparse readout similar to hybrid sensors
- Moderate requirement for timing and radiation tolerance
- Excellent sensor performance with large operation margin
- Production complete (1200 wafers) – Installation in 2019/2020

ATLAS ITk pixel outer layers (HL-LHC)
- 25 ns bunch crossing time and tolerance to NIEL fluence $> 10^{15}$ (1 MeV neq/cm$^2$)
  - Full depletion for radiation tolerance and fast charge collection
- Large collection electrode (HV-CMOS): Electronics in the collection electrode.
  - Functional sensors, good radiation tolerance, power penalty due to large sensor capacitance ($> 100$ fF) and robust design to avoid cross talk.
- Small collection electrode (CMOS sensor modified process) for full depletion combined with low C ($< 5$ fF, circuit + sensor)
  - Good sensor performance after irradiation
  - Design of two large-scale demonstrators with low power front-end ($< 25$ ns, $< 1$ µW)
    - MALTA, asynchronous readout, TJ-Monopix, synchronous readout
  - Characterization in progress. First results indicate good sensor performance after irradiation and functional matrices.
- Design effort now concentrating on periphery/system aspects to be compatible with RD53
  - serial powering, trigger memory, CDR + data transmission
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Large vs Small collection electrode

**Large collection electrode (HV-CMOS)**
- Large capacitance
- Higher power
- Practically uniform field
- Very high radiation tolerance

**Small collection electrode (TJ)**
- Small capacitance
- Lower power
- Less prone to coupling
- Longer signal travel path, process modification to increase radiation tolerance
Large vs Small collection electrode

**Sensor leakage noise**
Proportional to the integration time
Negligible for short integration time (1 µs)

**Input transistor noise**
1/f noise can be reduced by filtering, the thermal noise is dominant.
The proportionality constant depend on the type of filter.

Assuming that main analog power dissipation comes from the input transistor bias

\[
N \propto \frac{1}{\sqrt{g_m}} \quad S = \frac{Q}{C}
\]

\[
\frac{S}{N} \propto \frac{Q}{C} \sqrt{g_m} \propto \frac{Q}{C} 2a \sqrt{I}
\]

\[g_m \propto I^{1/a}\]

\[a = 2 \text{ in strong inversion} \]
\[a = 1 \text{ in weak inversion} \]

Fixing the S/N for a given bandwidth, lower C/Q allows for a lower power

\[
P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2a}
\]

\[
P \propto \left(\frac{C}{Q}\right)^{2a}
\]
Asynchronous matrix readout

- No clock distribution over the pixel matrix – (power reduction)

- Hits are stored using in-pixel flip-flops and transmitted asynchronously over high-speed buses to the end-of-column logic (programmable pulse duration 0.5 ns to 2.0 ns)

- Double-column divided into groups of 2x8 pixels ("red" and "blue")

- Buses shared by all groups of the same colour in the double-column

- Group number encoded on 5-bit group address bus
MALTA - Power to transmit matrix data to the periphery

- Assumptions: Matrix 2 cm x 2 cm, pitch 36.4 um
- CMOS signals in the matrix (no noise issues, no need to use power consuming differential transmission)
- Analog Power < 75 mW/cm²
- Power for clock distribution (not used in the asynchronous readout)
  - Energy per 1 cm toggled line at 1.8 V = 3.2 pF/cm x (1.8 V)² = 10.4 pJ
  - 137 lines per cm ( 1 per double column ) for 36.4 μm pixel pitch:
    \[ 137 \times 10.4 \text{ pJ} \times 40 \text{ MHz} = 57 \text{ mW/cm}^2 \]

- Matrix readout

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pixel hit rate</th>
<th>Power/bit/cm² (H=2 cm)</th>
<th>Matrix readout power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>hit/BC/mm²</td>
<td>Mhit/mm²</td>
<td>mW/cm²</td>
</tr>
<tr>
<td>0</td>
<td>0.68</td>
<td>27.2</td>
<td>17.7</td>
</tr>
<tr>
<td>1</td>
<td>0.21</td>
<td>8.4</td>
<td>5.5</td>
</tr>
<tr>
<td>2</td>
<td>0.043</td>
<td>1.72</td>
<td>1.1</td>
</tr>
<tr>
<td>3</td>
<td>0.029</td>
<td>1.16</td>
<td>0.8</td>
</tr>
<tr>
<td>4</td>
<td>0.021</td>
<td>0.84</td>
<td>0.5</td>
</tr>
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</table>