THE ATLAS TILE CALORIMETER PHASE-II UPGRADE DEMONSTRATOR DATA ACQUISITION AND SOFTWARE

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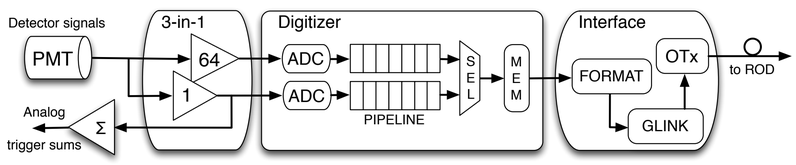
ON BEHALF OF THE ATLAS TILE CALORIMETER SYSTEM

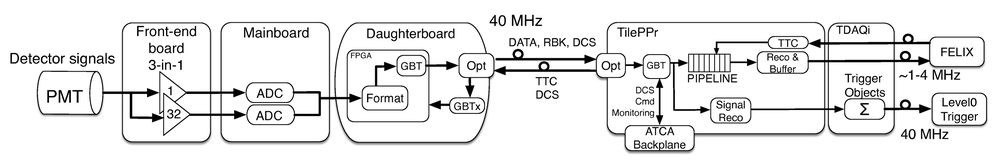
The Phase-II upgrades will prepare the ATLAS experiment for the High Luminosity LHC (*HL-LHC*). We expect 5-7x the current instantaneous luminosity and need to transmit the full set of digitized data off-detector at 40 MHz for the new trigger.

THE ATLAS TILE CALORIMETER PHASE-II UPGRADE

The Tile Calorimeter (*TileCal*) is the central section of the hadronic calorimeter in ATLAS. In the Current system the Digital samples of the PMT (*Photomultiplier Tube*) signals are stored in pipeline memories while the PMT analog signals are grouped and sent to the Level 1 (*L1*) Calorimeter system. The digital data for events selected by the L1 trigger system are transmitted to the Read-Out Drivers (*RODs*) located in the back-end system at a maximum rate of 100 kHz. The planned series of upgrades will impose new requirements that TileCal will need to accommodate. The TileCal read-out chain is being redesigned to read out the digitized data from every crossing using the PreProcessors (*PPr*) that are located off-detector.



Current Tile front-end schematic. *The required 16-bit dynamic range was achieved using two gains (factor of 64) into 10-bit ADCs located on the motherboard. The digitized data is buffered and sent to the back-end only if a Level-1 trigger-accept is received.*



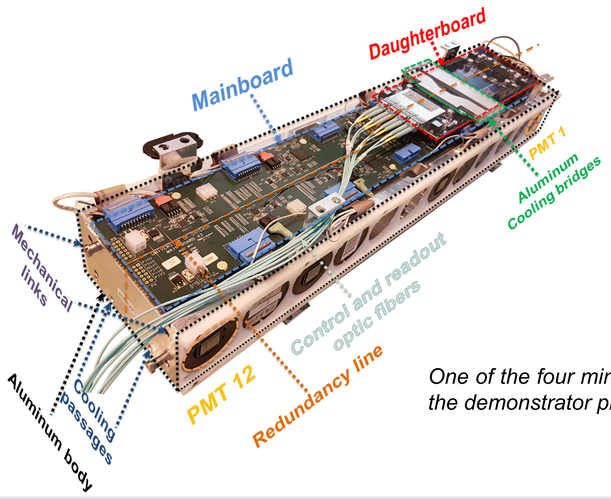
Phase-II Tile front-end schematic. *By using two gains (factor of 32) into 12-bit ADCs on the motherboard, a 17-bit dynamic range is achieved. The full set of digitized data is sent off detector at 40 MHz.*

TileCal Demonstrator Status

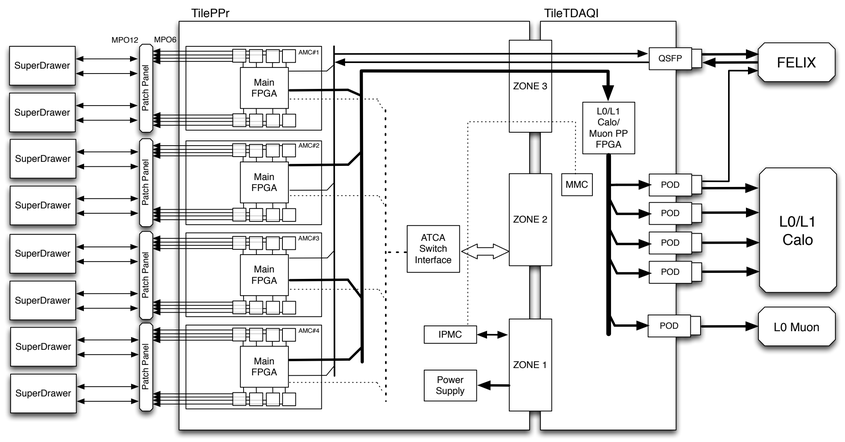
The Demonstrator Prototypes were built to evaluate the new electronics and read-out while maintaining backwards compatibility with the current setup. The demonstrator has been tested in various test-beam campaigns.

FRONT-END ELECTRONICS

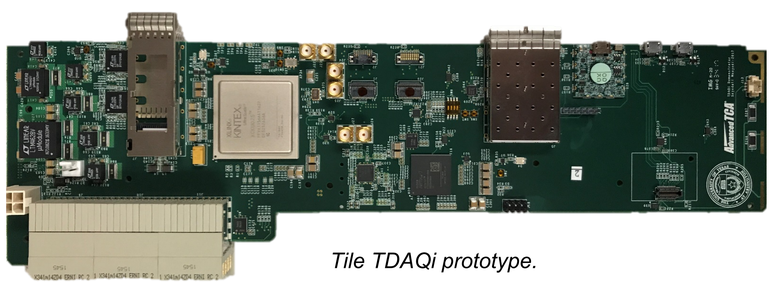
The *3in1* Front-End Board (*FEB*) option has been chosen to acquire the PMT signals. These are connected to a Mainboard that provides voltage and controls, digitizes the signal and sends it to the Daughterboard. The Daughterboard is the interface between the on- and off-detector (PPr) electronics.



One of the four mini-drawers of the demonstrator prototype.



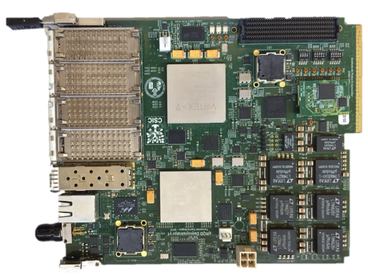
Block diagram of the final PPr design.

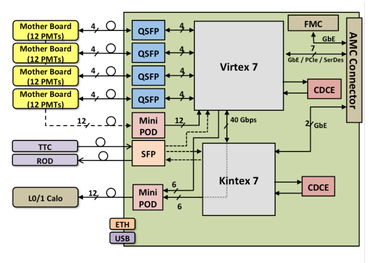


Tile TDAQi prototype.

PREPROCESSOR

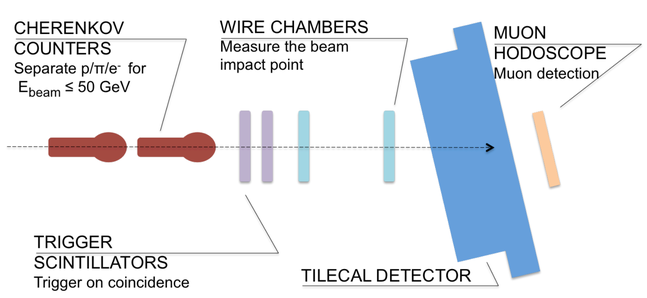
The PreProcessor (*PPr*) is the core element of the back-end system, providing communication with the front-end to transmit commands and to receive the digitized PMT data. Once a trigger signal is received the data is formatted and transmitted to the legacy Read-Out Driver, maintaining compatibility. During the HL-LHC the Trigger and DAQ interface (TDAQi) will provide preprocessed information to the new trigger and Front-End Link eXchange (FELIX) systems, the core of the new ATLAS Trigger/DAQ architecture.





Picture and block diagram of the PPr demonstrator module.

Test Beam

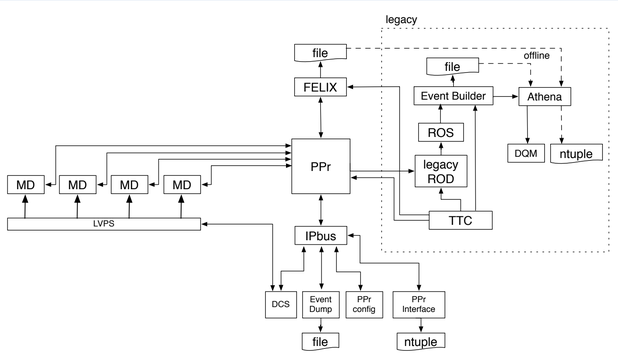


Beam line setup. Three TileCal modules, two long barrel and one extended barrel, were exposed to muons, electrons, pions, kaons, and protons.

DATA ACQUISITION AND PROCESSING

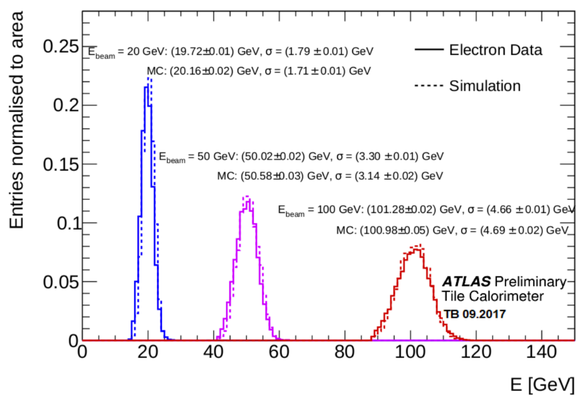
The demonstrator was inserted into a long barrel module and equipped with *3in1* cards. The data selected by the trigger system is stored in raw data files through the legacy Read Out System (*ROS*) and the new FELIX system in parallel. The ROS sends the data packets and saves the detector and beam data in a local disk.

The ATLAS software framework (*Athena*) is used to reconstruct the raw data stored in the Event Builder and FELIX to energy and time per cell. This operation is performed online for some events for monitoring.



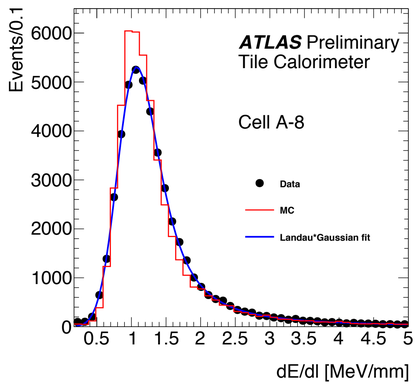
ELECTRONS

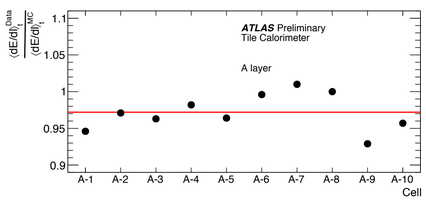
We expect electrons to deposit all of their energy in the calorimeter.



MUONS

Muon energy lost in ionization is proportional to path length.

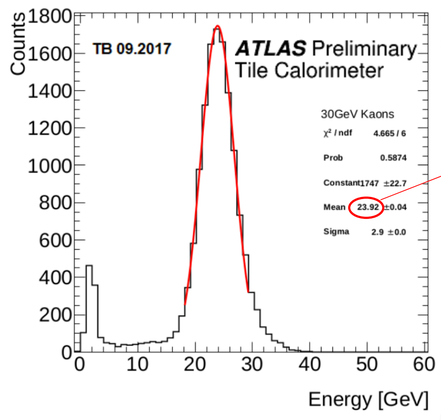


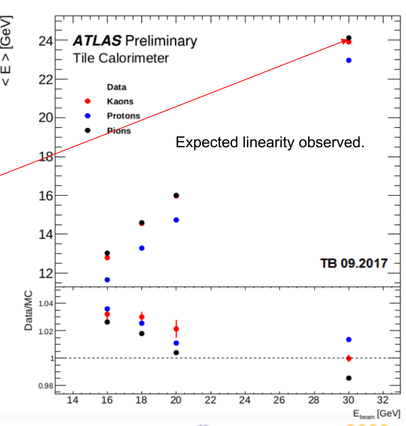


LEFT: Deposited energy per unit length for cell A-8 shown for data and simulation.
BELOW: Comparison for Data/MC for A-layer. Layer uniformity of 1% and Data/MC within 4%.

HADRONS

Response is calculated using the mean of a gaussian fit within $\pm 2\sigma$ of the peak.





This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168
AIDA 2020

Jared Little, on behalf of the ATLAS Tile Calorimeter System
The University of Texas at Arlington
Poster Preseted at LHCP, Bologna 4-9 June, 2018

ATLAS EXPERIMENT