The Fast TracKer system (FTK) is a track reconstruction processor. It receives data from the Inner Detector (ID) for all events accepted by the ATLAS Level 1 trigger and it performs full event tracking at the Level 1 trigger acceptance rate (100 kHz).

The LHC will deliver more and more challenging conditions:
- pile-up (peak mean number of interactions per bunch crossing) above 50 in recent data taking;
- higher pile-up expected in Run 3;
- Major combinatorial challenge to tracking!

The Fast TracKer system (FTK) is a track reconstruction processor. It receives data from the Inner Detector (ID) for all events accepted by the ATLAS Level 1 trigger and it performs full event tracking at the Level 1 trigger acceptance rate (100 kHz).

Idea: all possible tracks are simulated before an ATLAS data taking run. During the data-taking, the ID hits are compared with the hits expected from the simulated tracks as they are read out.

Hardware needed: the comparison is implemented using dedicated ASIC hardware based on associative memories and high performance Field Programmable Gate Arrays to provide the needed computing power.

Validation of patterns by running with FTK simulation on data (2018-2020);
- Slice A: full FTK slice (tower 22) saving 12-layer tracks
- Slice B: AUX to HLT (tower 40): saving 8-layer tracks
For commissioning FTK slices are prescaling on FTK trigger type

First data with FTK
- June 2017: 50 events have been compared to FTK simulation.
- The distribution of 8L tracks/event shows that FTK can handle high multiplicity events;
- validation of patterns by running with FTK simulation on data (2018-2020);
- problematics: inaccurate match to ID hits;
- deployment: "hemisphere" with half FTK coverage (2018);
- evaluation of the performance of FTK with FTK data when available and use collected problematic events to debug the system (2018);
- further validation and optimization with simulated data (2018-2020);
- plans for the future

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The system will deliver full-event reconstruction of all tracks with pT > 1 GeV at a much larger rate than is otherwise possible in the High Level Trigger (HLT), allowing for:
- better identification of physics objects such as b-jets and tau's;
- improved displaced tracks and secondary vertexes identification;
- refine missing transverse momentum reconstruction;
- help mitigating the effects of pileup;
- use looser HLT jet thresholds.

The FTK system is highly parallelized: the detector is divided in 64 η x φ slices processed in parallel by custom electronics boards (FTK slice):
- Input Mezzanine (IM) handles input from the ID and performs clustering.
- Data Formatter (DF) distributes clusters to the FTK towers.
- Auxiliary card (AUX) and Associative Memory Board: all possible track patterns have been determined from simulation and stored into associative memory (AM) chips;
- AM chips compare hits to O(10^9) patterns simultaneously;
- perform first-stage 8-layer track fit.
- Second stage board receives data from the AUX and further hits from the DF and performs a 12-layers fit.
- FTK to Level-2 Interface Card (FLIC) converts data into the ATLAS format and send them to the HLT.

The full system is constituted by ~ 450 boards, 8k AM chips, 2k FPGAs.

**References**

[1] Annovi, A. and others, "Design of a hardware track finder (Fast TracKer) for the ATLAS trigger" JINST (2014) no. 9, C01045

**Plans for the future**

Validate FTK so that HLT can trigger on its output in Run 3 (planned for 2021):
- evaluation of the performance of FTK with FTK data when available and use collected problematic events to debug the system (2018);
- deploy the "hemisphere" with half FTK coverage (2018);
- further validation and optimization with simulated data (2018-2020);
- plans for the future

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