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Test of a New Octal Amplifier Shaper Discriminator Chip for the ATLAS MDT Chambers at HL-LHC

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To exploit the physics potential of the ATLAS experiment at the HL-LHC a trigger system with a first-level trigger rate of 1 MHz at a maximum latency of 10 μ s will be employed. The TDCs of the current front-end electronics of the ATLAS muon drift-tube (MDT) chambers is incompatible with these trigger requirements and will have to be replaced by new TDCs. So will have the amplifier discriminator (ASD) chips which are mounted on common front-end cards with the TDCs.

A new ASD chip with 8 channels was developed in 130 nm CMOS technology in Global Foundries process. The system is composed by the cascade of the analog signal processing front end and the Wilkinson A/D, performing both time-over-threshold and charge measurement. The sensitivity at the output of the analog signal processing chain is 14 mV/fC, while the equivalent-noisecharge is 0.6 fC (\sim 3.38 ke), performing <12 ns preamplifier rise time. These performances have been achieved while managing very high detector parasitic capacitance at the front-end input (\sim 60 pF). Each channel consumes less than 10 mA from a single 3.3-V supply voltage. In 130 nm CMOS, the total area occupancy is 6.3 mm².

In our presentation the results of laboratory tests with test pulses as well as results which were obtained with the new chips on a muon chamber operated in a highly energetic muon beam under varying gamma background rated in CERN's Gamma Irradiation Facility GIF++. Thanks to a higher amplification the new chip shows a better spatial resolution than the old ASD chip currently used in the ATLAS experiment.

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