During 2019, the Large Hadron Collider (LHC) will undergo a phase known as Long Shutdown 2, during which all the particle accelerators and the experiments located on its circumference (such as the ATLAS experiment) will be upgraded in order to reach the performances required for the physics challenges foreseen. Here is shown a proposal for a new PCI Express based board, namely the PiLUP (Pixel detector high Luminosity lhC UPgrade), designed by the Electronic Laboratories of the Istituto Nazionale di Fisica Nucleare (INFN) and the Electronic Laboratories of the Bologna University as the successor of the current data taking board for the ATLAS Pixel Detector created by the same groups in 2012.

**HARDWARE PROPOSAL (PiLUP BOARD)**

- 3 Flash Memories (2x16 MB, 1x128 MB), 3 Clock Generators (1 Phase-Locked Loop).
- FMC CONNECTORS (400 PINS+4 TRANSCIEVERS (50 Gb/s), 124+1(12.5 Gb/s), 128)
- JTAG PROGRAMMER PORT MICRO-USB
- 2xUART PORTS (115200 BR ZYNQ-7000, 9600 BR KINTEX-7)
- SFP+ (10 Gb/s) OPTICAL FIBRES CONNECTORS
- 2xETHERNET PORTS (1 Gb/s ZYNQ-7000, 10 Gb/s KINTEX-7)
- SMA CONNECTORS (12.5 Gb/s)
- PCI Express Gen2 PORT (8 TRANSCIEVERS->100 Gb/s)
- 2 GB DDR3 RAM KINTEX-7
- 1 GB DDR3 RAM ZYNQ-7000

**LOW AND HIGH LEVEL CONTROL SYSTEM**

- arm Linux
- Chip2Chip master
- 21 LVDS lines
- Chip2Chip slave
- Custom Logic
- AXI REGS
- AXI Peripheral

All the logic cores communicate through AXI4 protocol

- Embedded Linux system running on the ARM processor;
- Complete low-level control from the Zynq-7000 and high-level management of the system from external interfaces;
- AXI4 addressable register block to control custom logic without AXI4 interface.

**PROPOSED SOLUTION FOR THE ATLAS DAQ TESTS**

- 28 nm FPGAs (xc7z020-1cgg484c & xc7k352t-2ffg900c);
- 21 differential bus at 200 MHz DDR between the FPGAs;
- Zynq-7000 Master with an ARM Cortex-A9 Dual-Core processor;
- Kintex-7 Slave with 16 fast links transceivers up to 12.5 Gb/s.

**TESTS FOR THE APPLICATION PROPOSED**

- Successful communication between PiLUP and FELIX cards;
- Developing and testing a RD53a emulator (on FPGA);
- Complete tests with FELIX cards, Protocol Converter and RD53a emulator going well.

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