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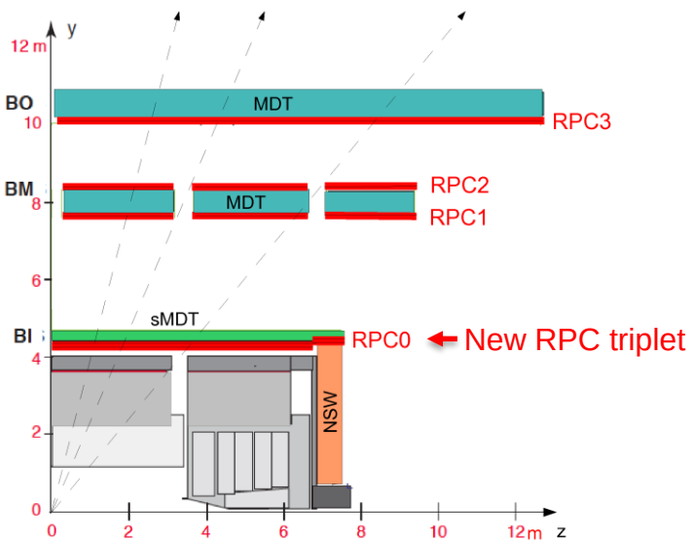
Studies of the Level-0 Muon Trigger algorithm in the Barrel region of the ATLAS experiment for High-Luminosity LHC

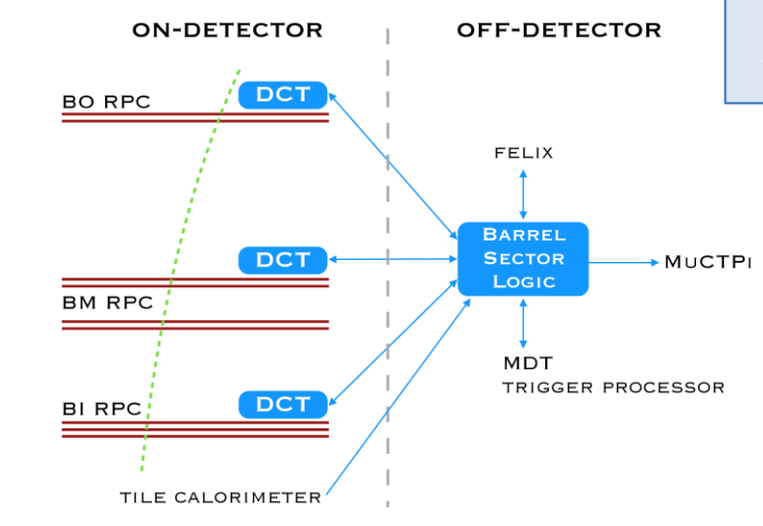
Abstract

The first level hardware trigger system of the ATLAS experiment is expected to be fully upgraded for HL-LHC to stand the challenging performances requested with the increasing instantaneous luminosity. The Level-0 Muon Trigger system has to maintain or increase its data selection capability during HL-LHC, despite of the higher detector hit rate, cavern background and trigger rate.
The Resistive Plate Chamber (RPC) detector provides the main trigger source in the barrel region of the Muon Spectrometer. The upgraded trigger system foresees to send RPC raw hit data to the off-detector trigger processors, where the trigger algorithms run on Field-Programmable Gate Arrays (FPGAs). The FPGA represents an optimal solution in this context, because of its flexibility, wide availability of logical resources and high processing speed.
Studies and simulations of different trigger algorithms have been performed, together with the evaluation of the performances and efficiency of the barrel trigger system. The FPGA logic resource occupancy has also been estimated.



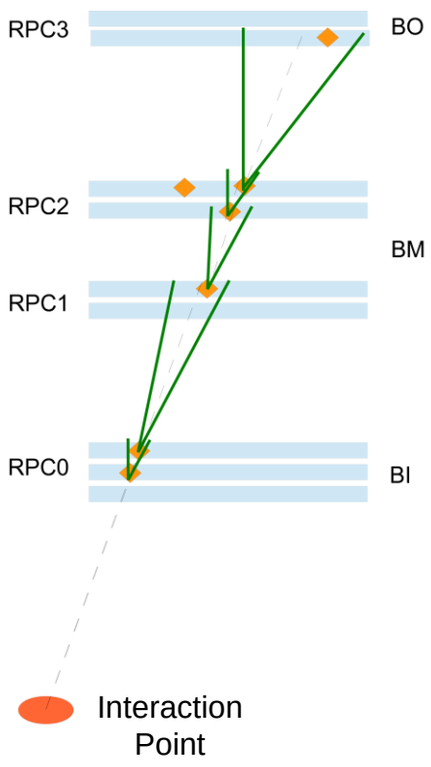
Main upgrades

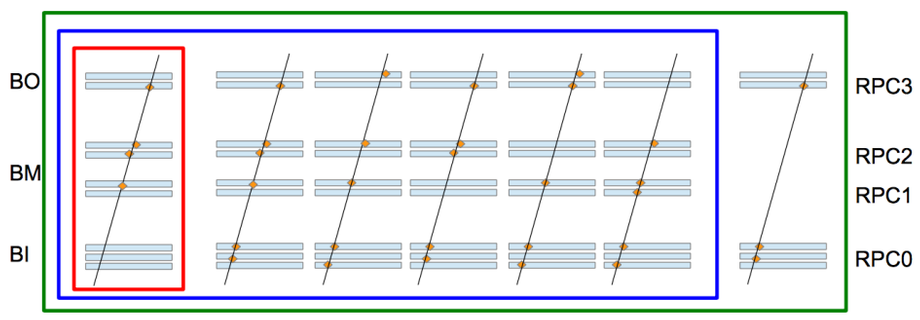
- Three additional RPC layers will be installed in the inner barrel region: muon barrel trigger acceptance will be extended from 80% to ~96%.
- The on- and off-detector trigger electronics will be replaced to make them compatible with the higher trigger rates and longer latencies necessary for the new Level-0 trigger.
- Usage of FPGAs both for Data Collector and Transmitter (DCT) and for the Barrel Sector Logic trigger algorithm.



Phase-2 Sector Logic Algorithm

- Recursive search for coincidence in all the layers
  - Define a pivot layer
  - Look for hits in a window of the nearest plan
  - If yes, iterate
  - Final path must satisfy some criteria
- Several coincidence scheme possible:
  3[RPC1+RPC2] AND 1[RPC3] or
  2[RPC0] AND 3[RPC1+RPC2+RPC3] or
  2[RPC0] AND 1[RPC3]
- RPC0 triplet (BI) useful to increase the acceptance and the robustness of the trigger.





Trigger Requirements and Simulation

ATLAS will have to face luminosity up to $7.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}}$.
L0 trigger will have a maximum latency of $10\ \mu\mathrm{s}$. Selected events will be sent to HLT at a rate of $1\ \mathrm{MHz}$.
Sector Logic Trigger algorithm has been simulated in order to test performances and efficiencies, also varying single-hit efficiency.
Expected trigger rates, depending on the algorithm:

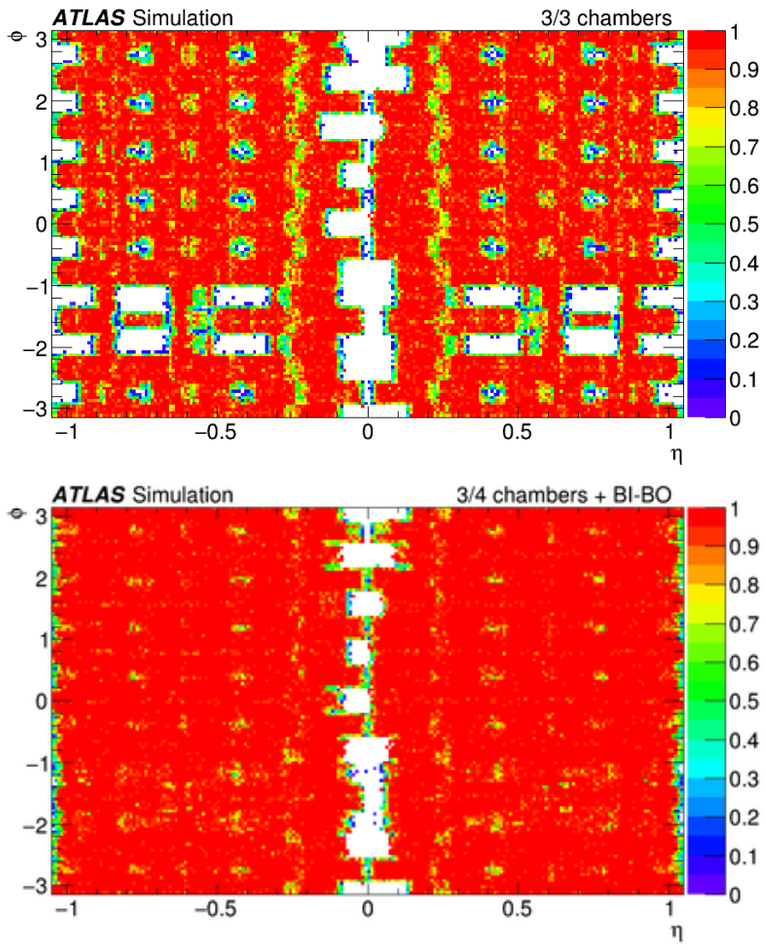
Requirement	Rate
3/3 chambers	20 kHz
3/4 chambers	30 kHz
3/4 chambers + BI-BO	85 kHz
3/4 chambers + BI-BO (*)	45 kHz

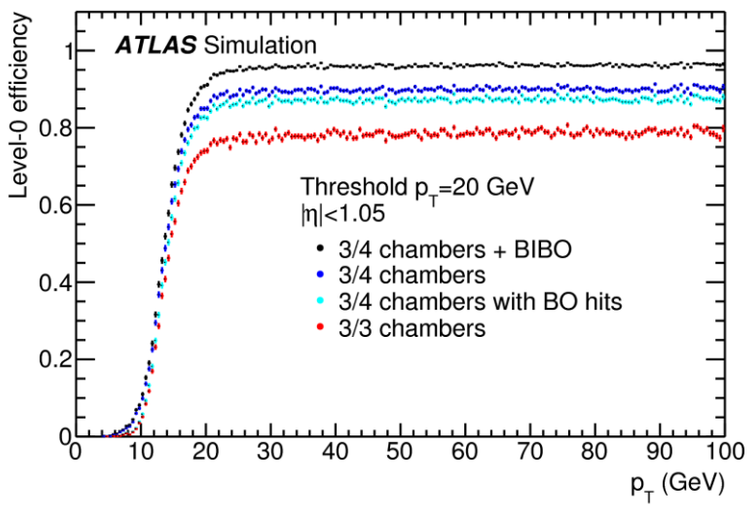
(*) if using BI-BO only in acceptance holes of 3/4 chambers trigger

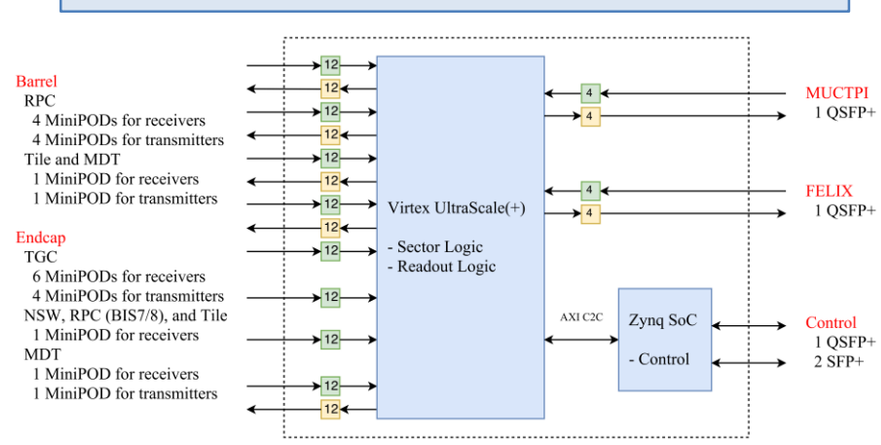
SL board FPGA

FPGA candidate:
Virtex UltraScale+ XCVU13P
- System Logic Cells (K): 3780
- Memory (Mb): 455
- GTY Transreceivers (32.75 GB/s): 128
- I/O Pins: 832

Logic resource occupancy expected to be <40%.







References and Acknowledgements

[1] Technical Design Report for the ATLAS Muon Spectrometer Phase-II Upgrade, ATLAS Collaboration, CERN-LHCC-2017-017, ATLAS-TDR-026, https://cds.cern.ch/record/2285580

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