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Studies of the Level-0 Muon Trigger algorithm in the Barrel region of the ATLAS experiment for High-Luminosity LHC

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The first level hardware trigger system of the ATLAS experiment is expected to be fully upgraded for HL-LHC to stand the challenging performances requested with the increasing instantaneous luminosity. The Level-0 muon trigger system has to maintain or increase its data selection capability during HL-LHC, despite of the higher detector hit rate, cavern background and trigger rate. The Resistive Plate Chamber (RPC) detector provides the main trigger source in the barrel region of the Muon Spectrometer. The upgraded trigger system foresees to send RPC raw hit data to the off-detector trigger processors, where the trigger algorithms run on Field-Programmable Gate Arrays (FPGAs). The FPGA represents an optimal solution in this context, because of its flexibility, wide availability of logical resources and high processing speed.
Studies and simulations of different trigger algorithms have been performed, together with the evaluation of the performances and efficiency of the barrel trigger system. The FPGA logic resource occupancy has also been estimated.

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