RD53A interface board spec

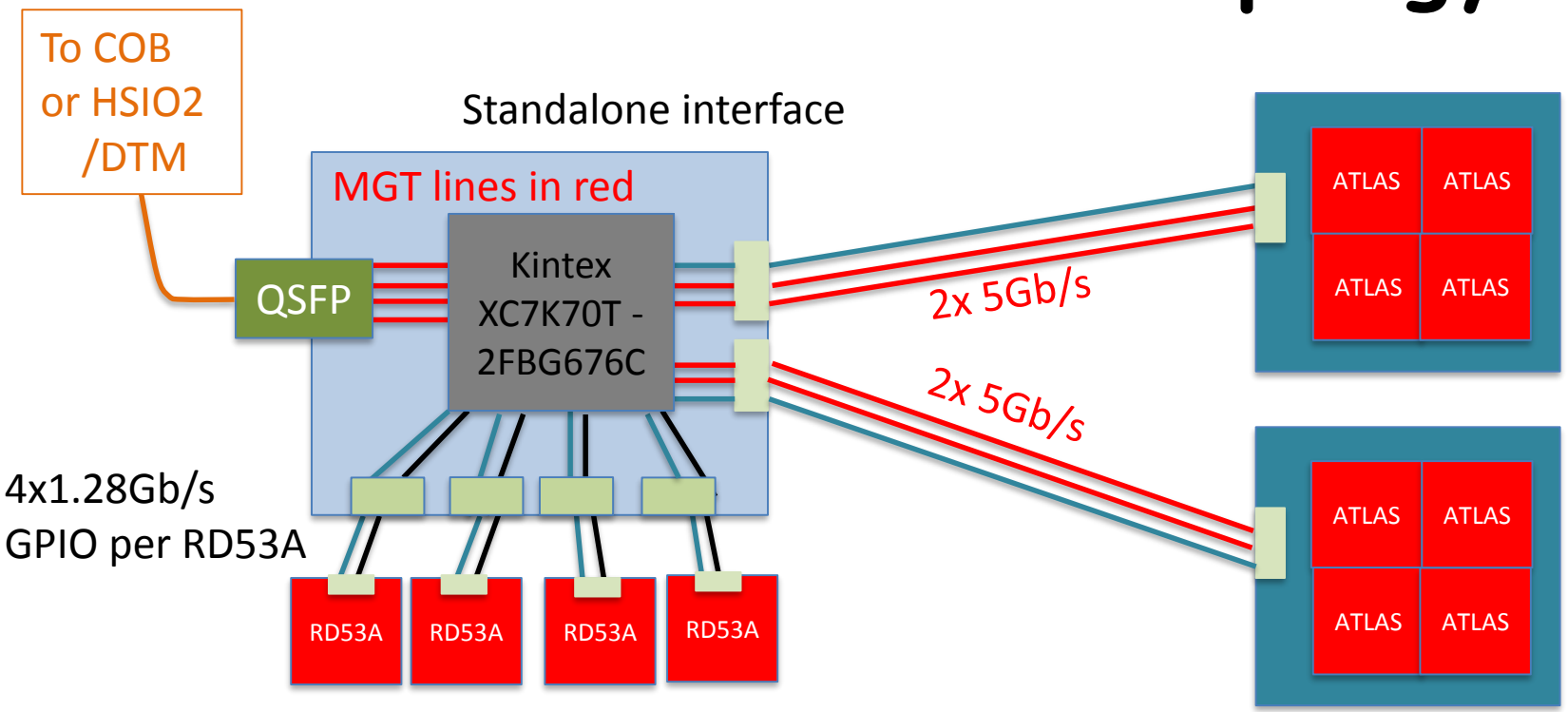
Su Dong

Nov/16/2017

Evolving RD53 / Module Topology

- RD53A Single Chip card with 4x1.28 Gb/s data links will be a more permanent feature with 5 Gb/s aggregation only off module ?
- All flavors of modules in two categories:
  - A: 1xCMD + 1xData: single chip, outer Quad, outer Dual
  - B: 1xCMD + 2xData: inner Dual, high rate inner Quad
- Will Quad/Dual module carrier retain DisplayPort interface or some compact flex header ? Will module carrier ever contain MUX to output 5 Gb/s ?

Possible Interface Topology

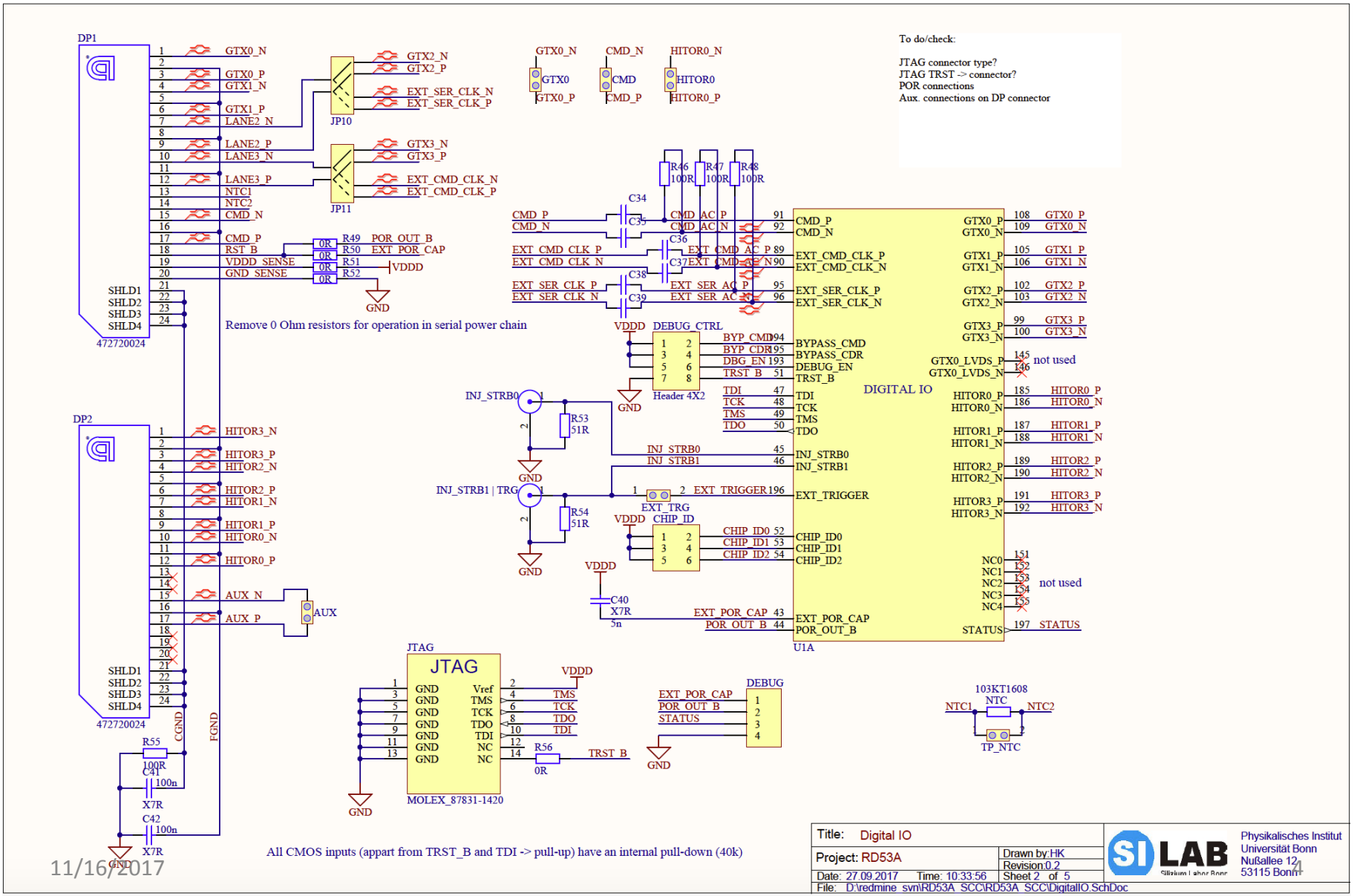


4 RD53A module DisplayPorts

Additional external clock/trigger not drawn

Is there a clever way to switch to 4 modules of single 5 Gb/s each ?

RD53A SC schematics



Signal Specs

- Selection of DP for different module types
  - 4x RD53A modules using GPIO lines
  - 2x (maybe 4) ATLAS modules using MGT lines
- Each module test carrier has two DisplayPorts
  - DP1 (RD53A): CMD^{+-},RST(?),$GTX[0:4]^{+-}$,NTC1,NTC2
    (ATLAS): CMD^{+-},RST(?),$GTX[0:1]^{+-}$,NTC1,NTC2
  - DP2: AUX^{+-} (ever needed?), $HitOR[0:3]^{+-}$
- Data links LVDS or CML ? Same FPGA pins OK ?
- At least one HitOR signal (LEMO?) need to be let out of the interface board ?
- External clock into interface – what type of connection ?
- Other misc signals to the interface ?