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CST Simulation of Speed Limitations of Inductive Voltage Adder Geometry

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The Time Domain solver of CST Microwave Studio is used to find a preferred geometry for the fastest possible pulse from an Inductive Voltage Adder (IVA).

Introduction

Rise time for simulation

Example geometries

Try replacing magnetic material with dielectric ?

For interest

Summary



Introduction – typical model, one cell only





Source Rise Time in Simulation

Chris_model_st1_seg2_60_vol3_L0_R3uC1-lessmesh_mue15k_6seg_01ns.cst· ¶



Bad luck with 0.1ns rise time. The resistive matched transmission line at the top of the model means longitudinal resonance can not exist. Transverse resonances seem possible with this period, but we did not see corresponding H and E fields to match this voltage. Result is also mesh-dependent. So this result may still be realistic but no use for the present study.



Source Rise Time in Simulation



Conclude:

To have some chance with comparing different simulation geometry:

avoid rise time <4ns

avoid any source impedance which could slow current rise



Basic Geometries









Ring to the wall

Ring to the base

Two metal rings















Output voltage at waveguide port for 4ns rise time for additional



Voltage [V]



Try replacing magnetic material with dielectric?

Example: σ=0, ε=15000, μ=1





Conclude:

Most energy is magnetic so dielectric constant of core is not so important Yes – an IVA needs magnetic material



possible high speed geometry using circuit board sandwich for minimum stage height





For interest –

what happens if only one stage is triggered?





- CST simulation is a tedious trade-off of model size, meshing parameters, etc. Expect a month's work to gain some confidence in results. Expect 4-8 hour run times.
- Use source excitation with 4ns rise time smaller rise times tended to give excessive simulation ringing which masked usable results
- Visualising the behaviour of vector fields in 3D is really confusing. In this presentation, only scalar E-Field magnitude was shown.
- Within the IVA structure, the transients propagate longitudinally go-and-return at the speed of light, independent of geometry. So if the structure is 1 meter long, the rise time limit is around twice 3ns plus source rise time.
- In practical terms, the inductance of the primary circuit dominates rise time. For this simulation, 16 radial voltage sources are used on each stage, each source 1V with impedance R=3uOhm, L=0nH, C=1F.
- For short pulses, the primary core material is not critical because any modest permeability is enough to slow the current rise of the source to practical values
- Only homogeneous core materials like ferrite have been used in simulation. So far, not able to simulate inhomogeneous, anisotropic materials like tape cores.

Appendix

References and Bibliography

[1] "The Small-Signal Frequency Response of Ferrites", Hamilton N., High Frequency Electronics, June 2011, and the references listed within

This reference is important !

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Wir schaffen Wissen – heute für morgen

My thanks go to

Martin Paraliev Aunt Helvetia







For fun – try adding a conducting tube to double the end-to-end propagation time











Steady-state H-field independent of geometry!

H (A/m) at 20ns





Example 1– Ring to the Wall

A/m 0.1 ± 0.0909

> 0.0727 0.0636 0.0545 0.0455 0.0364 0.0273 0.0182 0.00909





H (A/m) at 20ns



Example 1– Ring to the Wall

A/m 0.1 ± 0.0909

> 0.0727 0.0636 0.0545 0.0455 0.0364 0.0273 0.0182 0.00909









Example 2– Ring to the Base









0.001 + 0.00099 - 0.000818 - 0.000818 - 0.000727 - 0.000636 - 0.000545 - 0.000545 - 0.0009645 - 0.0009645 - 0.0009645 - 0.000964 - 0.000273 - 0.000964 - 0.000273 - 0.000964 - 0.000273 - 0.000964 - 0.000273 - 0.000964 - 0.000273 - 0.000964 - 0.000273 - 0.000964 - 0.000273 - 0.000964 - 0

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