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CST simulations of speed limitations of inductive adder topology

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"CST simulations of speed limitations of inductive adder topology"
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Using time domain simulations, the progression of E and H fields inside an IVA (Inductive Voltage Adder) can be visualised in 3D. The pulse generator sources are idealised voltage sources with minimum series impedance. A rise time of 4ns is typically used. Faster rise times lead to multiple resonant modes in the structure; these modes are sometimes asymmetric, and these modes make interpretation difficult. Many lengths and geometries of
an IVA are tried to find an optimum for speed. For practical application, the design of fast switches with minimial series impedance is dominating the problem, not the IVA itself.

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