

# The DBPM Development of IHEP

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Qiang Ye, YaoYao Du, **YuFei Ma**.

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# Outline

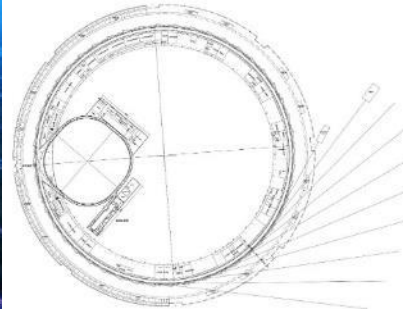
- General overview
- Hardware design
- Algorithm of Firmware design
- Software design
- Test results

# 1. General overview

# Team group of DBPM

- **Staff members:** ShuJun Wei, Qiang Ye, HuiZhou Ma, YaoYao Du, Fang Liu
- **Student members:** ZhiZhuo Wang, YuFei Ma, XingEr Zhang
- **Division of labor:**
  - ShuJun Wei , YuFei Ma (AMC) , YaoYao Du (RTM)
  - offline implementation of algorithm: Qiang Ye, Fang Liu
  - implementation of algorithm in FPGA: ShuJun Wei, YuFei Ma
  - Software development and application: Qiang Ye, HuiZhou Ma

# Brief introduction to DBPM

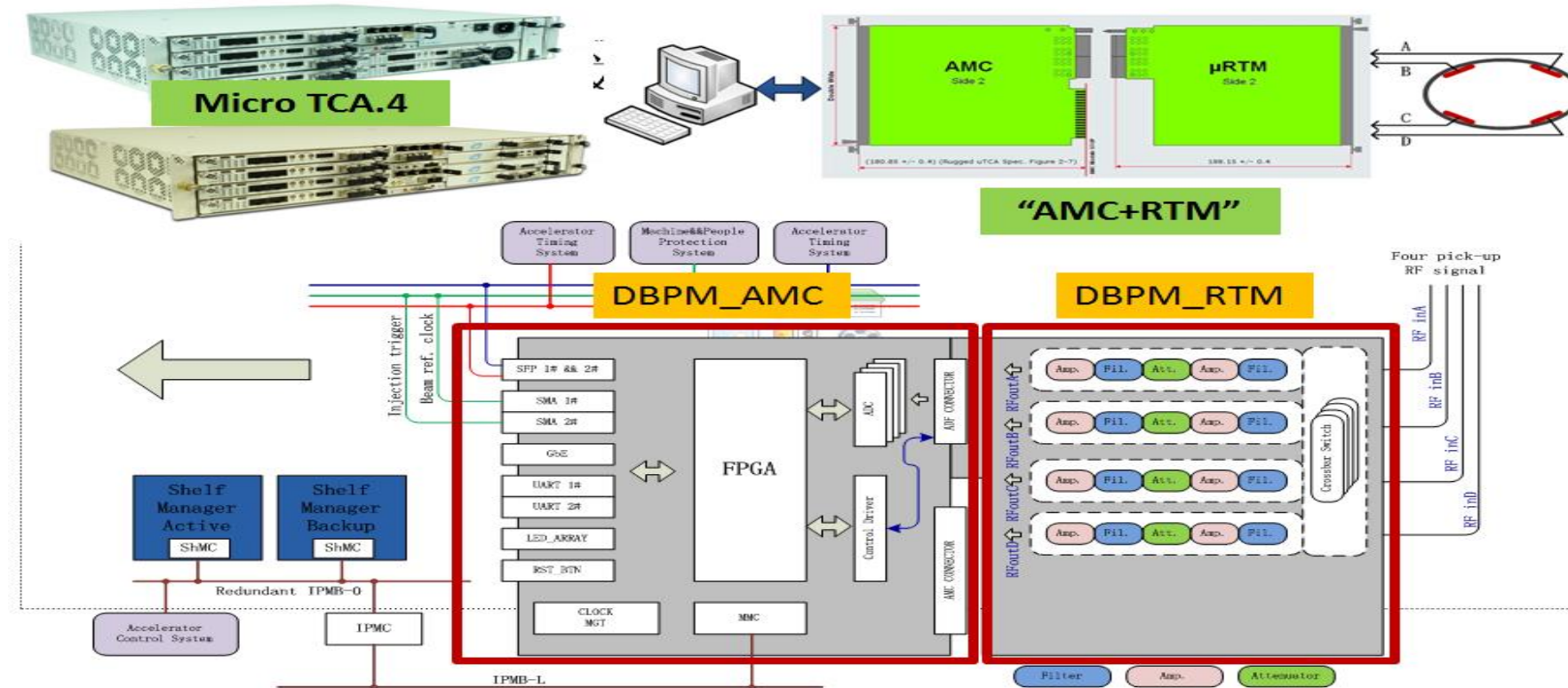


Storage ring circumference:  
1360m  
Energy: 6GeV  
Emittance: 60pmrad

## Main Parameter of DBPM

	<b>Libera Brilliance</b>	<b>DBPM@HEPS</b>	<b>DBPM@BEPCII</b>
<b>Turn by Turn Data</b>	<u>1<math>\mu</math>m @1.26MHz</u>	<u>1<math>\mu</math>m @220kHz</u>	<u>1<math>\mu</math>m @1.26MHz</u>
<b>FA data</b>	<u>0.1<math>\mu</math>m @10KHz</u>	<u>0.3<math>\mu</math>m @22KHz</u>	<u>0.3<math>\mu</math>m @10KHz</u>
<b>COD data</b>	<u>0.05<math>\mu</math>m @10Hz</u>	<u>0.1<math>\mu</math>m @10Hz</u>	<u>0.1<math>\mu</math>m @10Hz</u>

# DBPM System framework



The RTM board pick up analog signal from BPM probe, then fed the processed signal to AMC board; The analog signal is converted to digital signal first, then which are processed with special algorithm in FPGA.

## 2. Hardware design

2.1 RTM Design

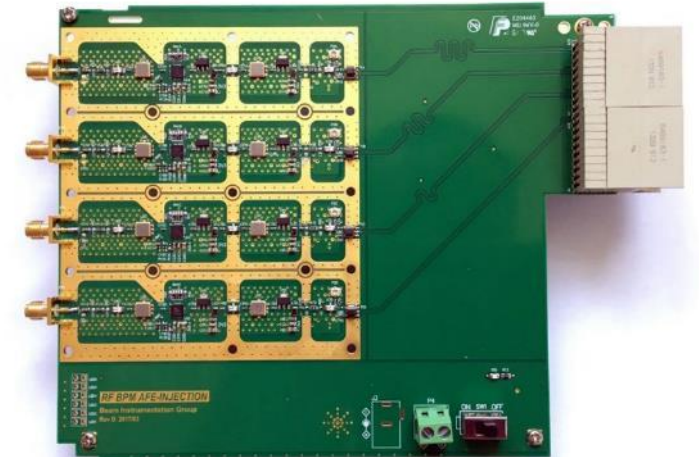
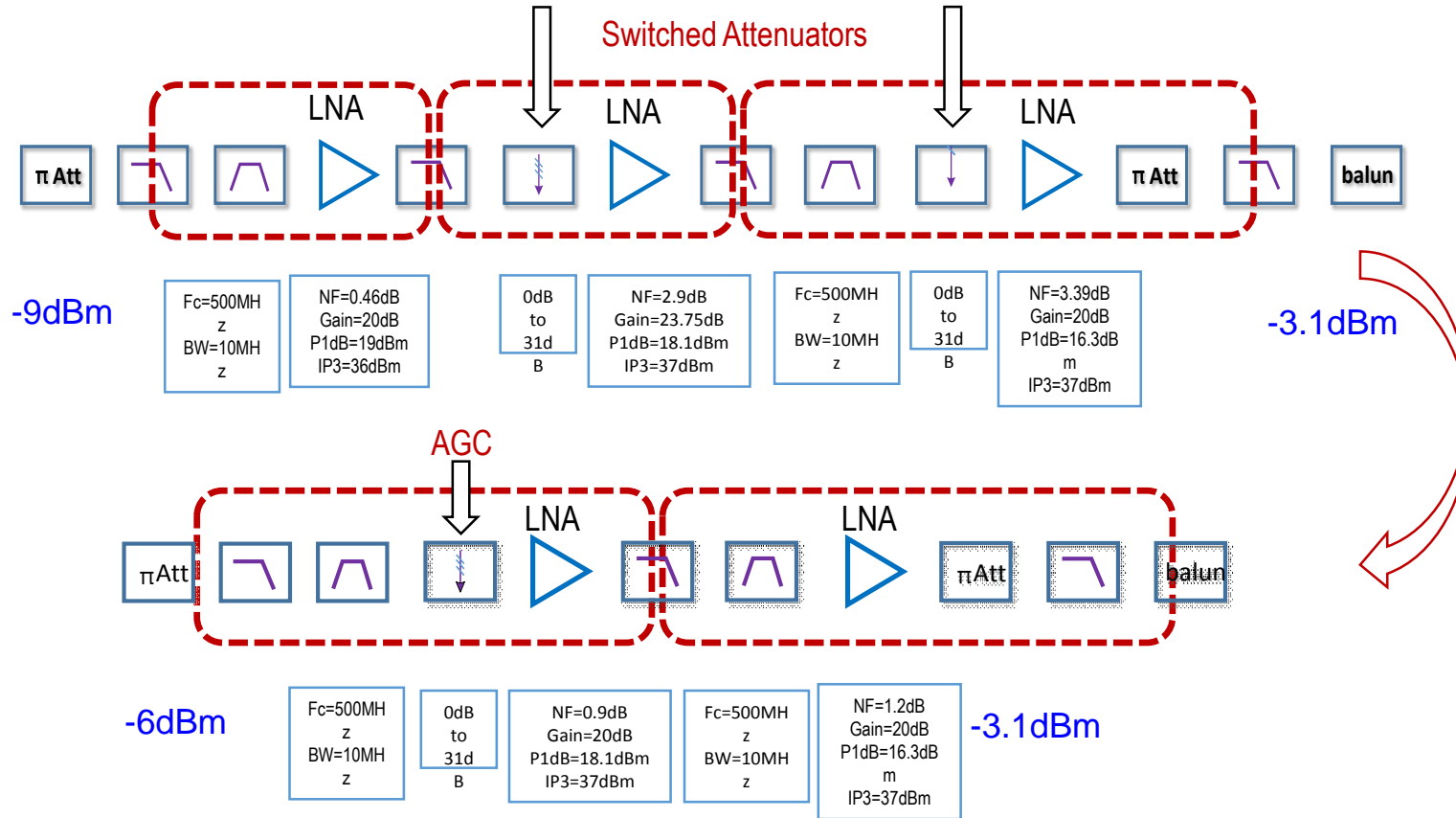
2.2 AMC Design

# 2.1 RTM Design

- Design scheme
- Signal test
- Main performance

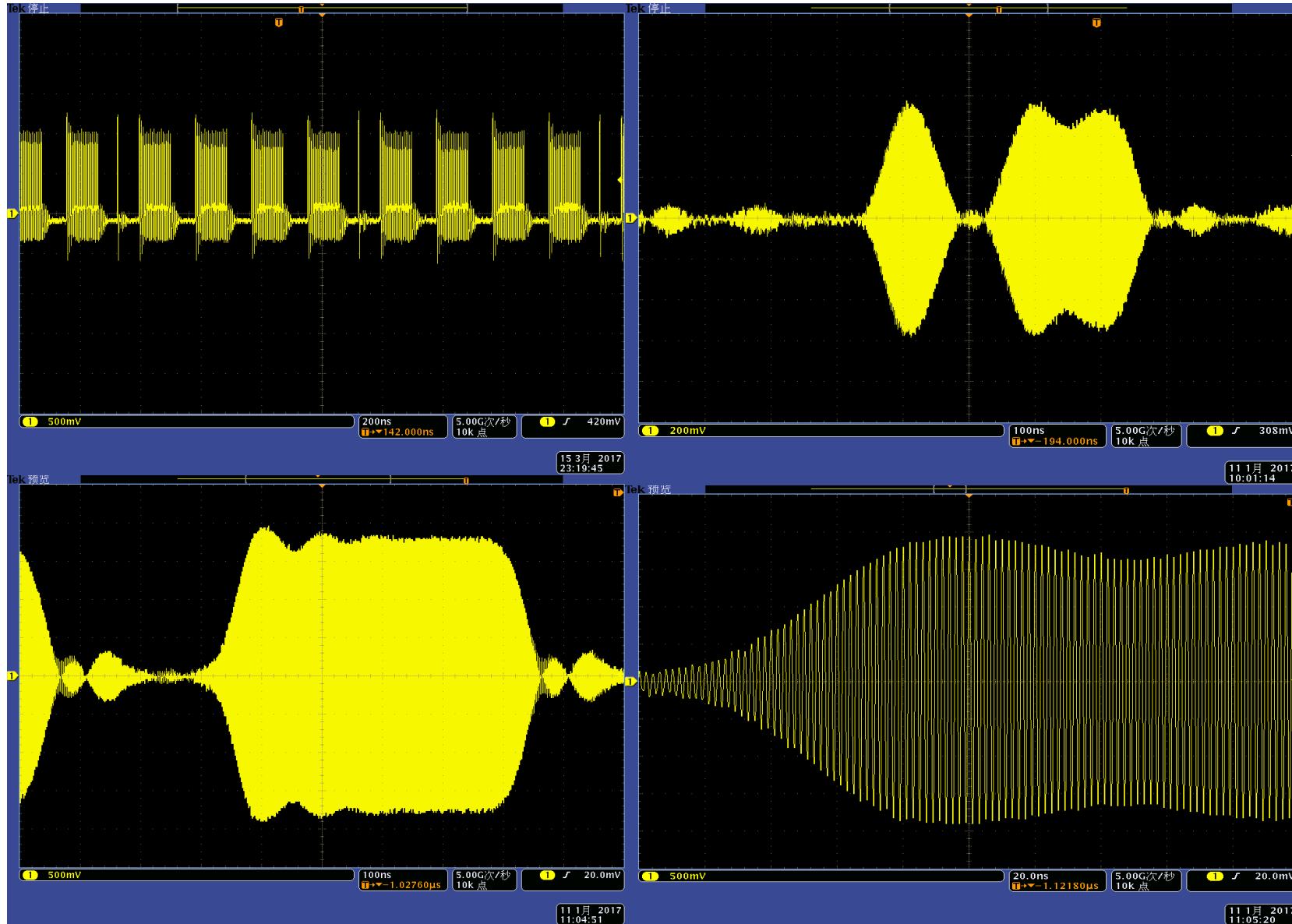


# Design scheme

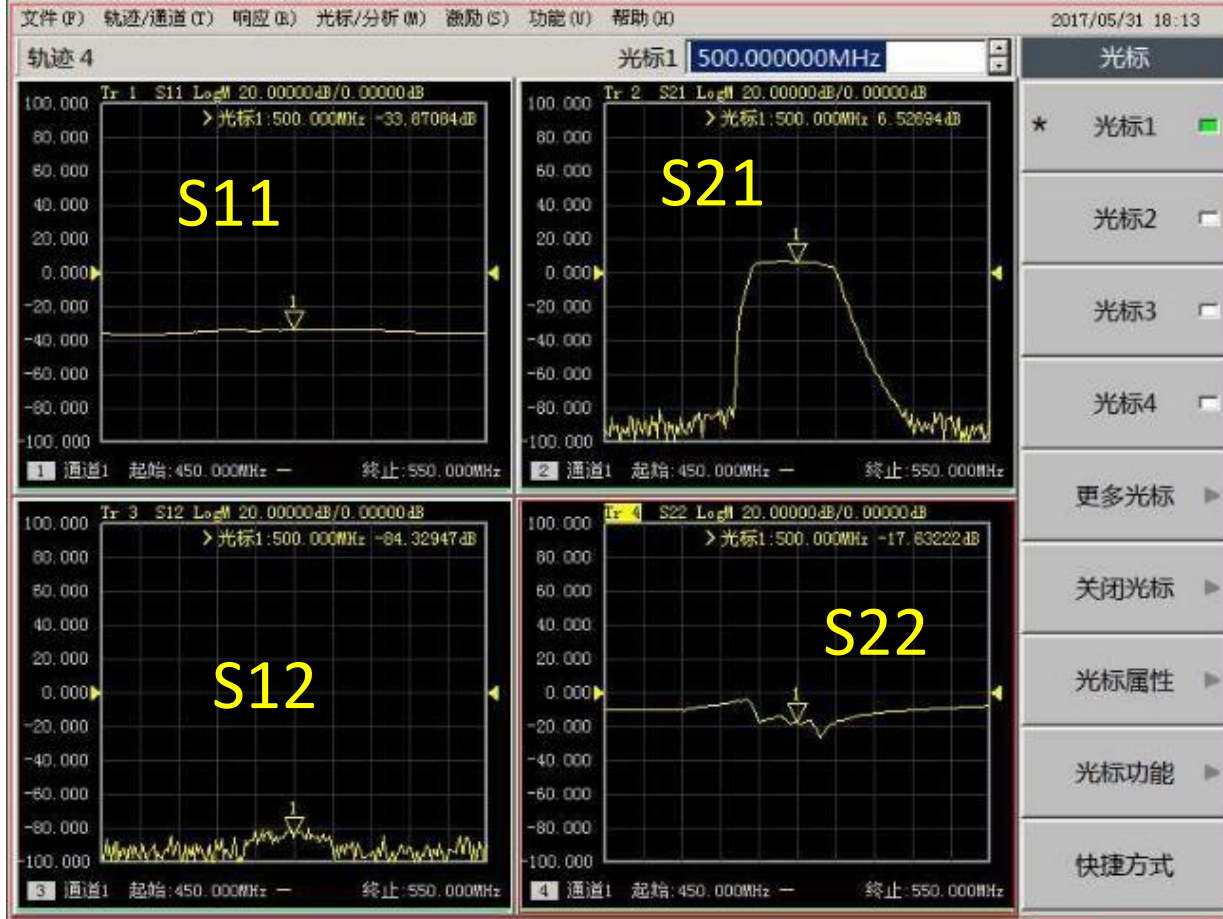


- 1、 Two design schemes
- 2、 Amplifier is sensitive to the temperature
- 3、 Two-stage amplification circuit

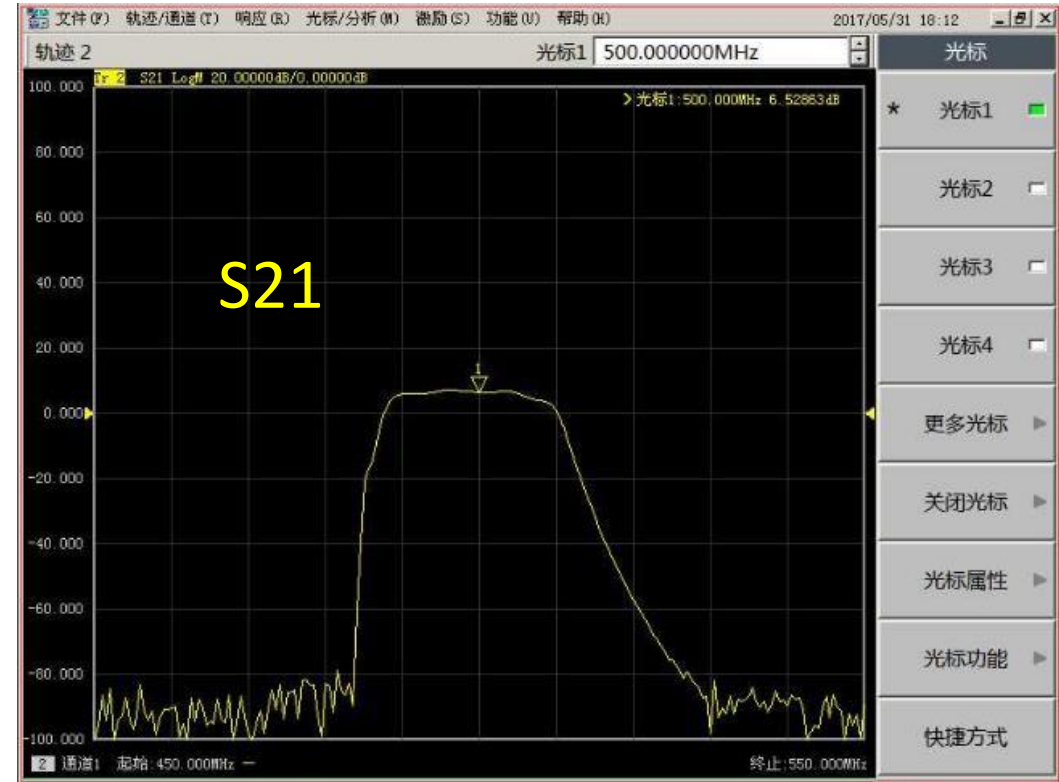
# Signal test specification



# Main performance



Receiver S-Parameter Characterization



$S_{21}$ -Parameter Characterization

The performance of band pass filter is good!

The output impedance matching still need improved!

# Main performance



**A→B**

$6.5\text{dBm} \rightarrow -78.8\text{dBm}$



**B→A**

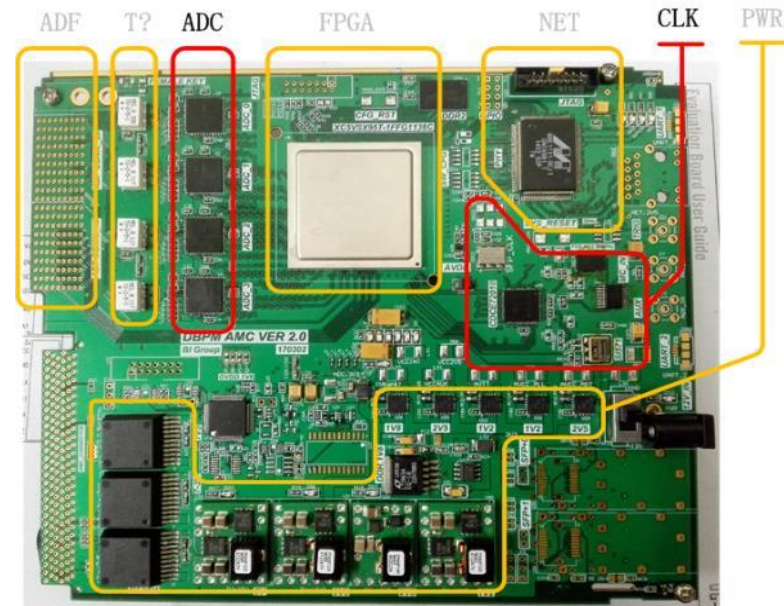
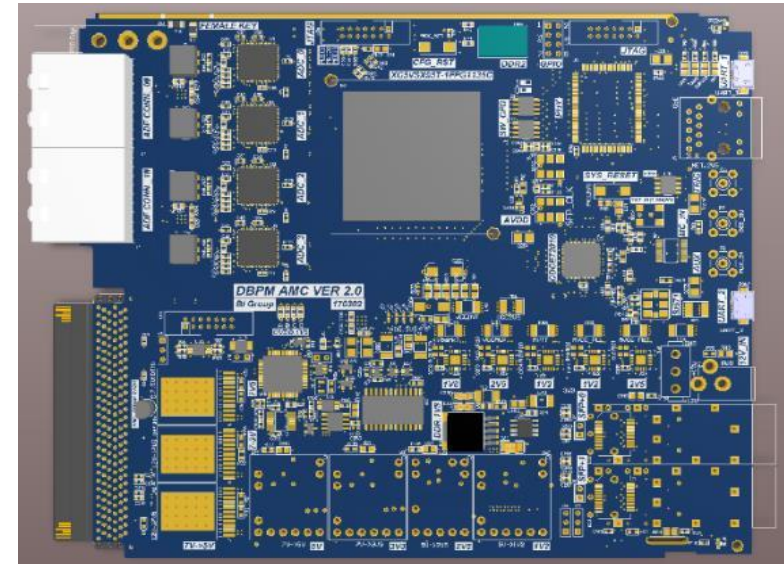
$6.5\text{dBm} \rightarrow -77.47\text{dBm}$

## 2.2 AMC Design

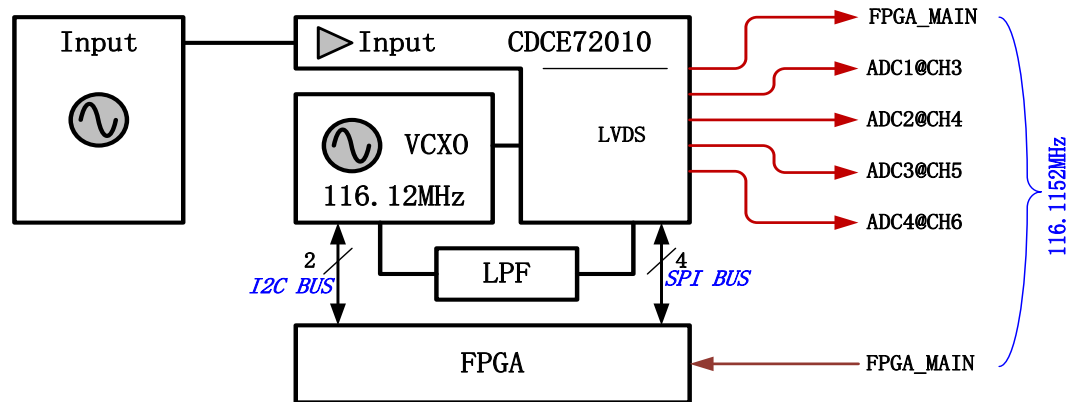
- Function module
- Signal test
- ADC SNR test

# Function module

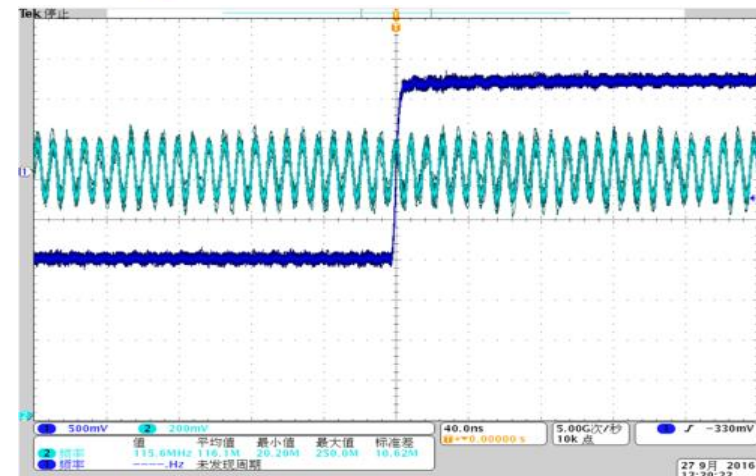
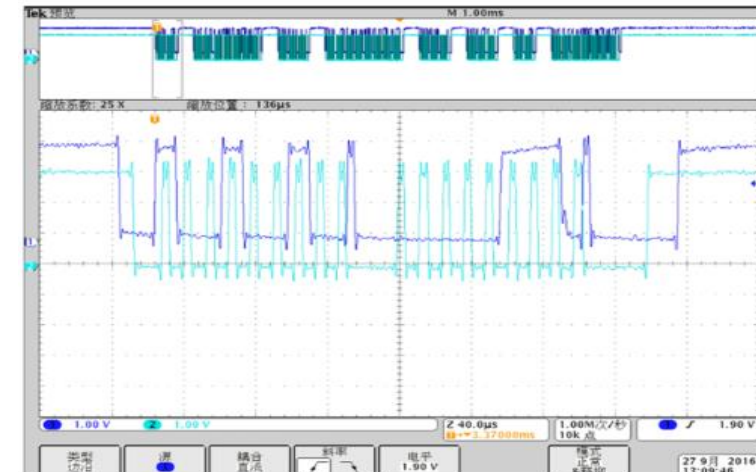
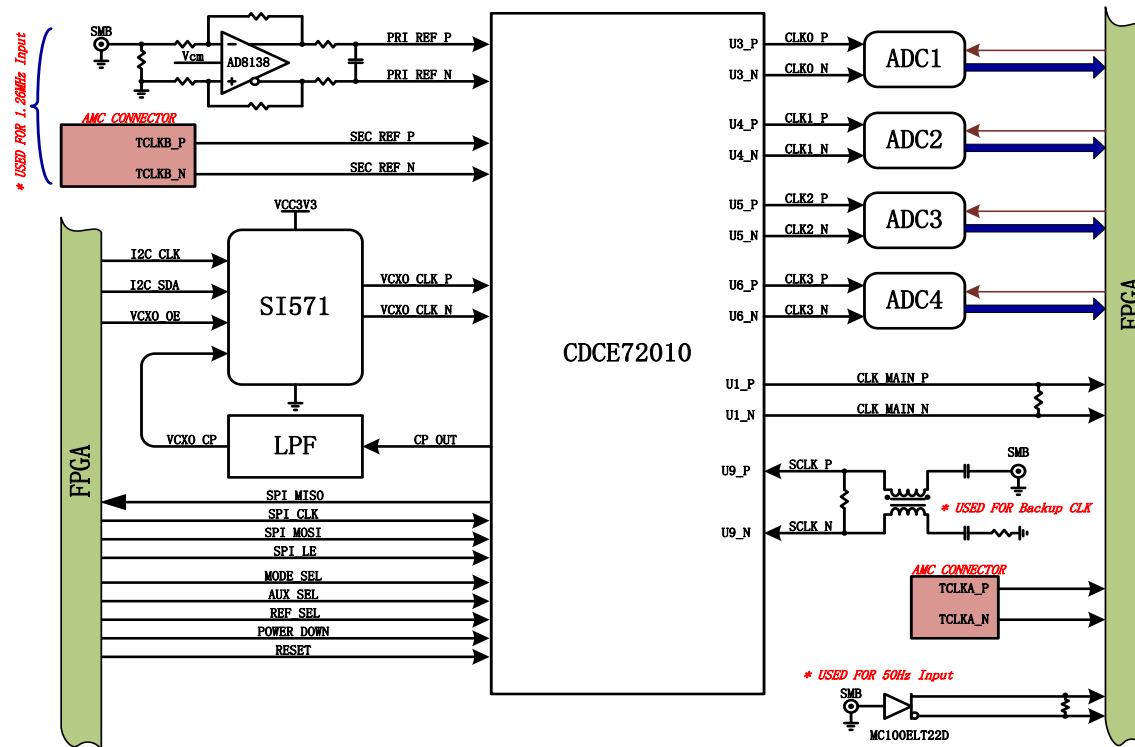
- Power Logic
- **Clock Logic**
- FPGA Logic
- **ADC Logic**
- NET Logic
- Other Logic...



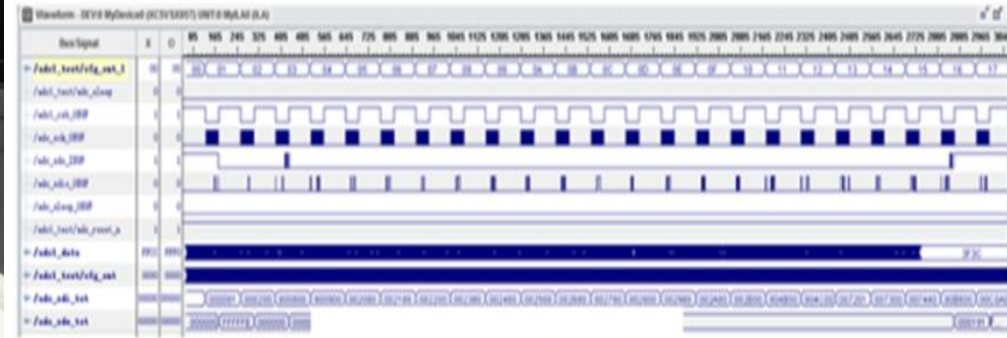
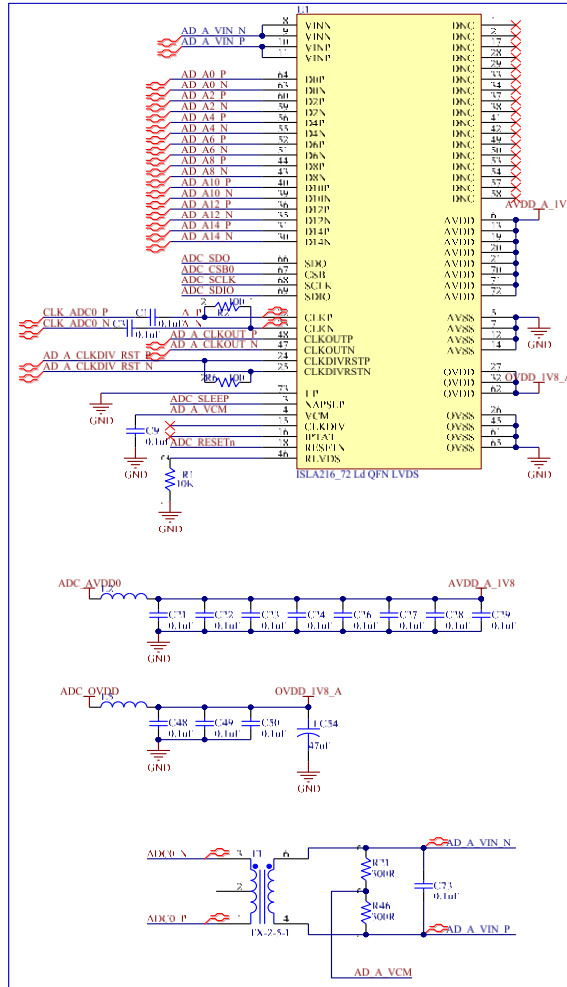
# Clock logic Scheme



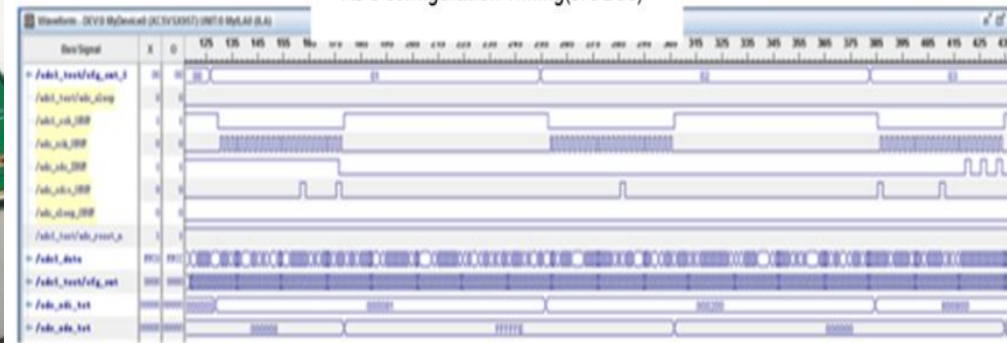
- SI571 Configuration (I2C)
- CDCE72010 Configuration (SPI)



# ADC logic scheme

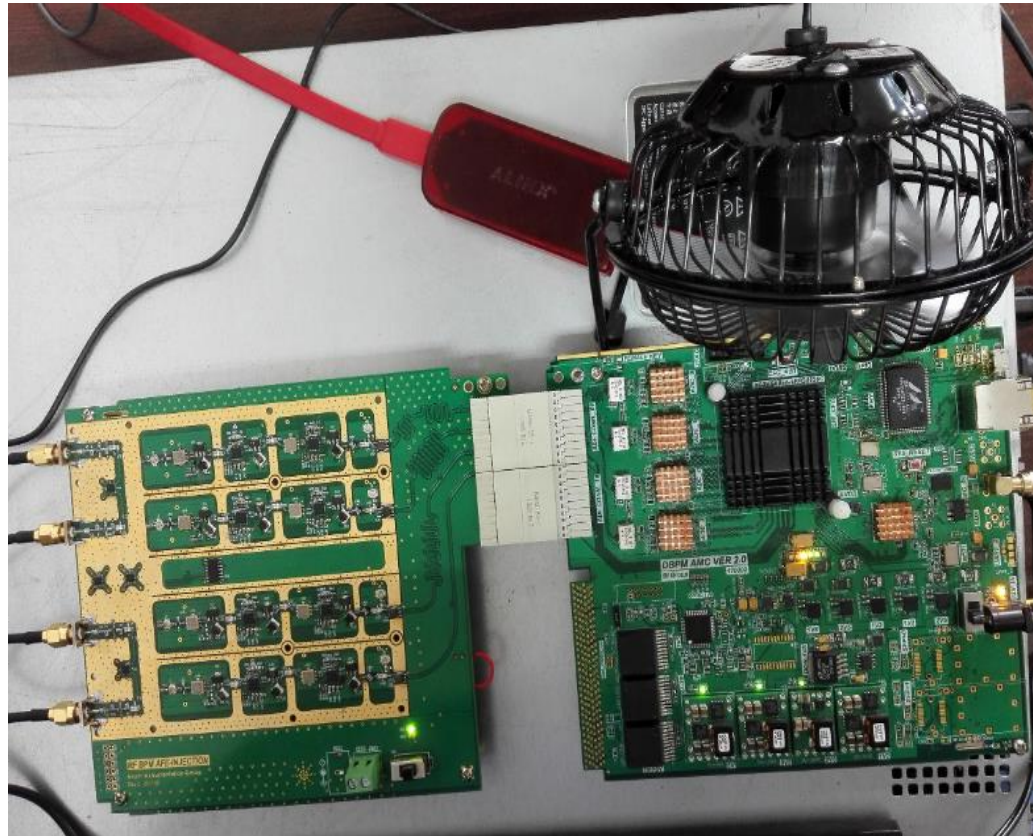


ADC configuration Timing(SPI BUS)





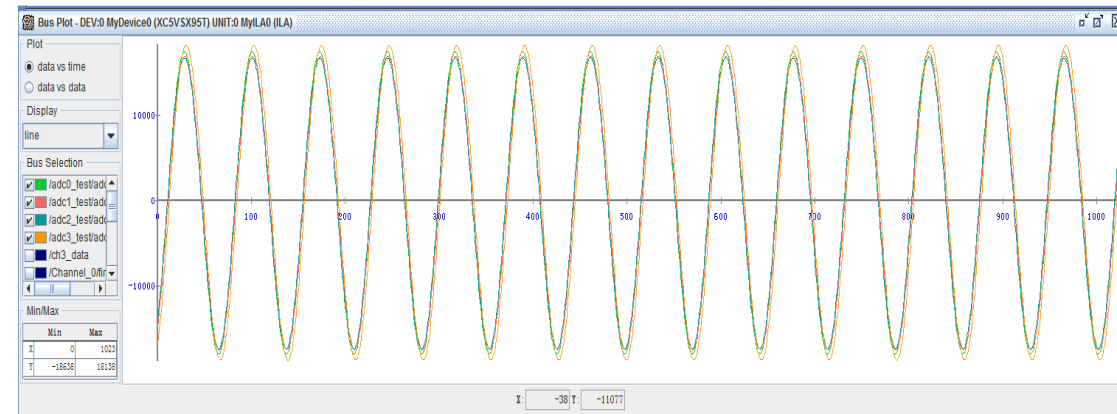
# Signal test specification



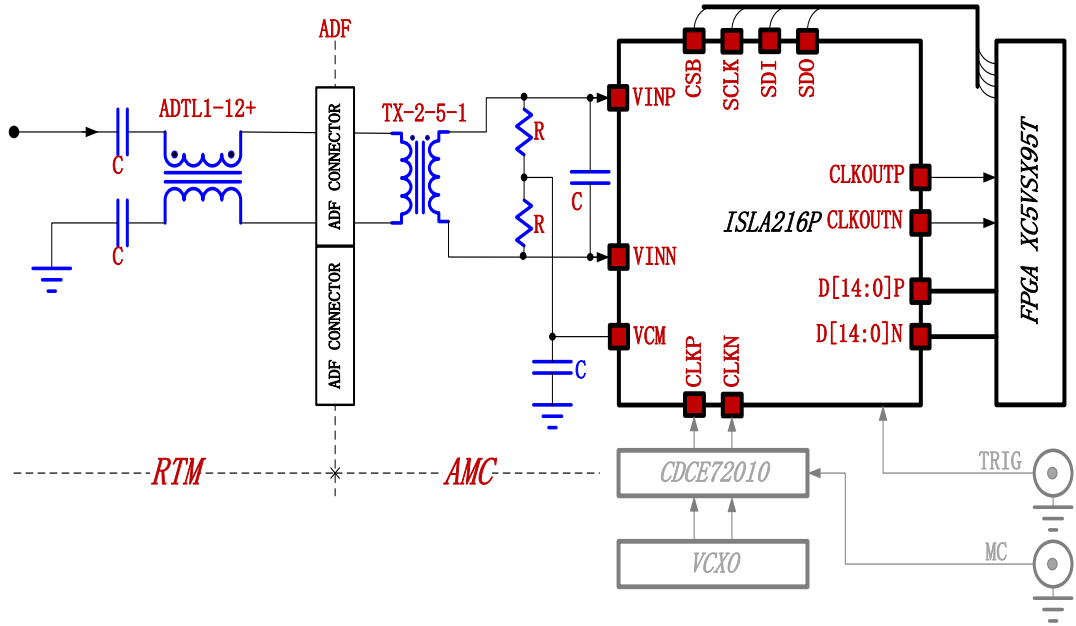
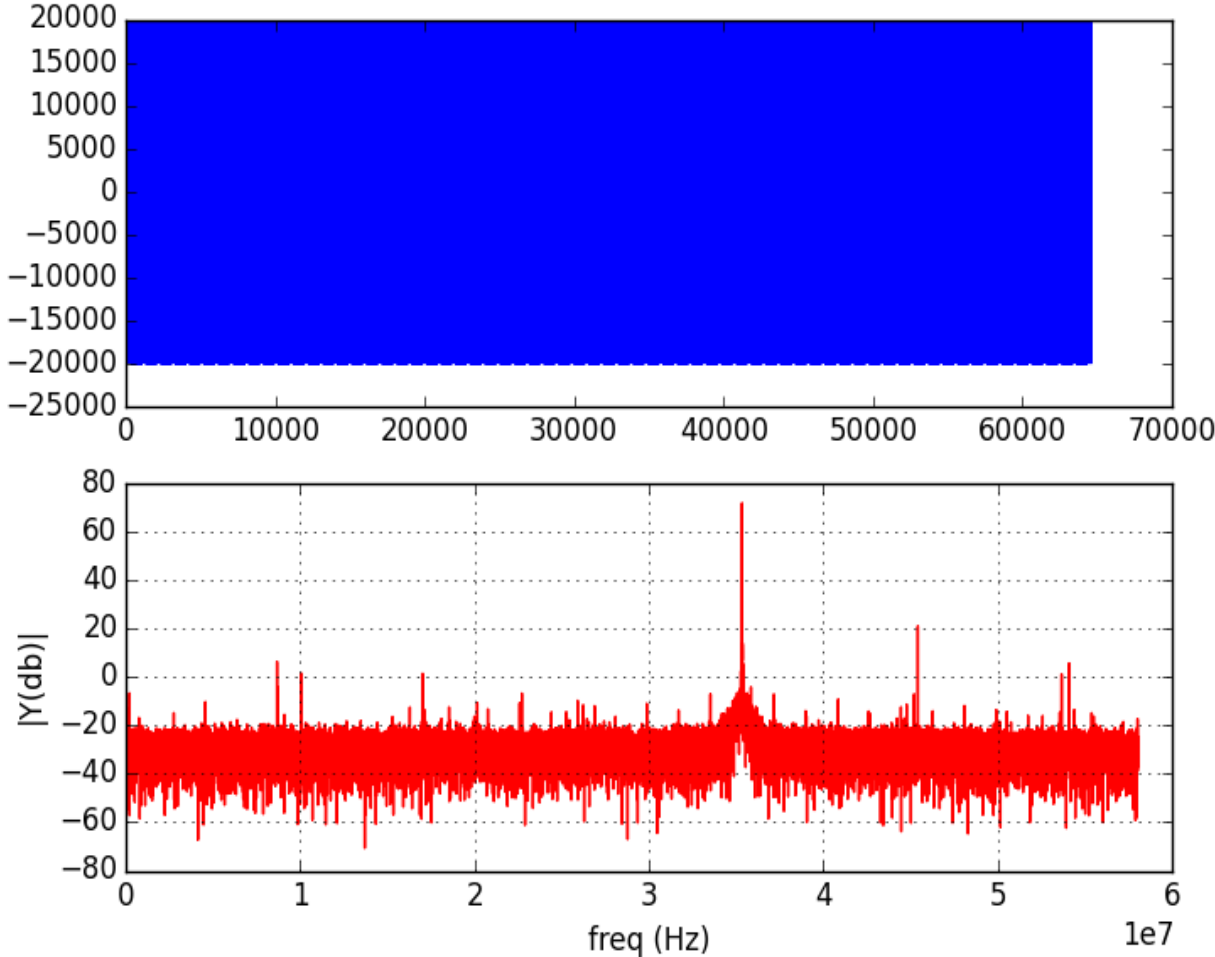
Without signal input:



With 500MHz signal input:



# ADC SNR test

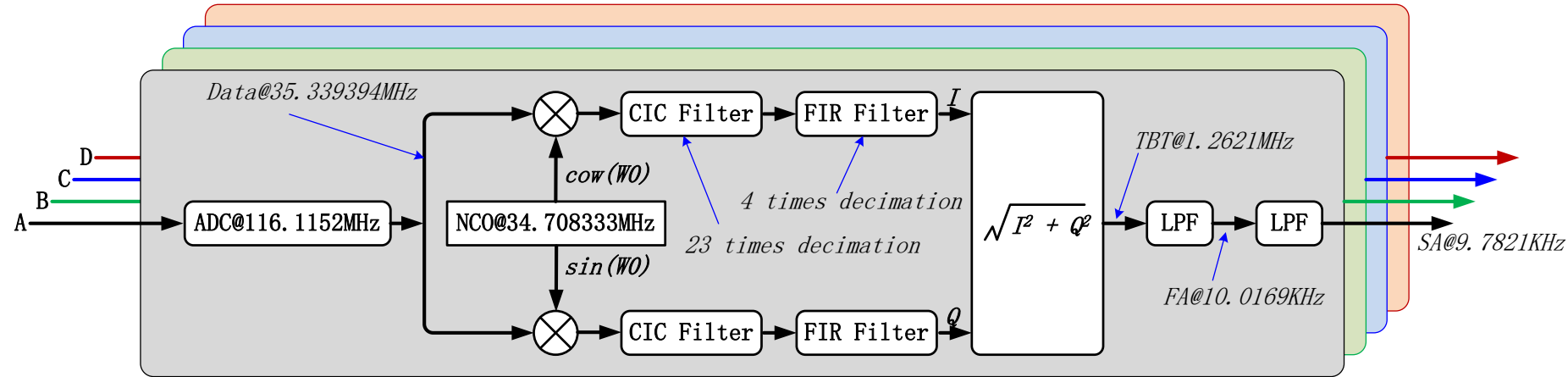


Better impedance matching is helpful to improve the SNR.

# 3. Algorithm of Firmware design

- Algorithm framework
- Algorithm simulation base on matlab
- Implementation of Algorithm in FPGA

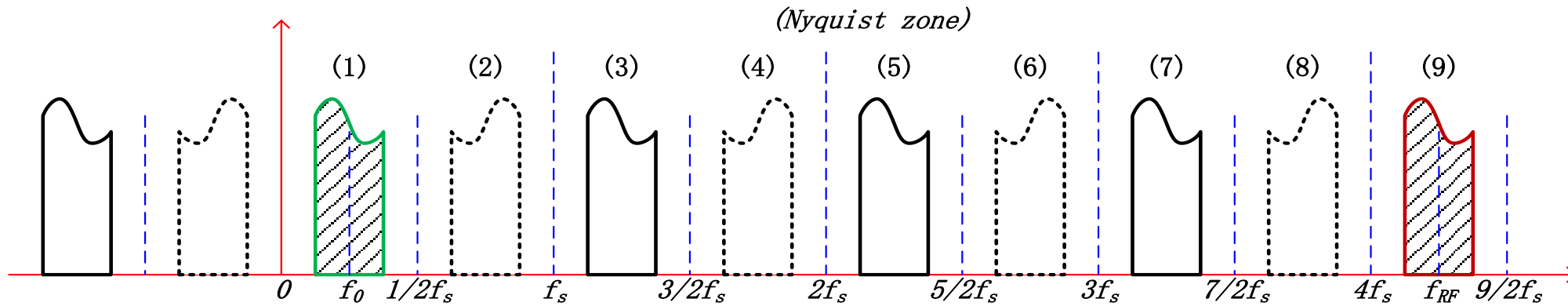
# Algorithm framework



Two selection principle of sampling frequency:

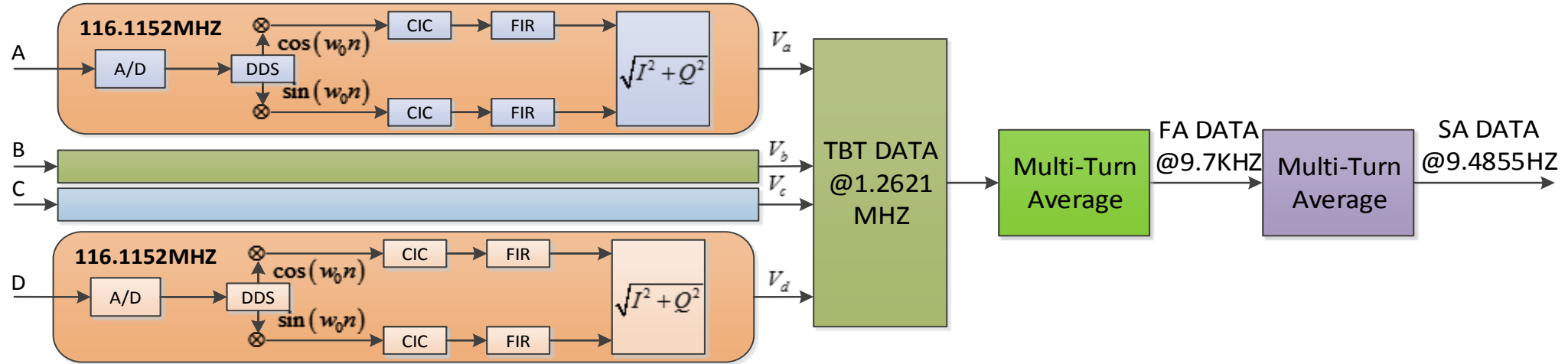
- Integer multiple of the cyclotron frequency
- RF frequency located on center of the odd Nyquist zone

# Sampling process

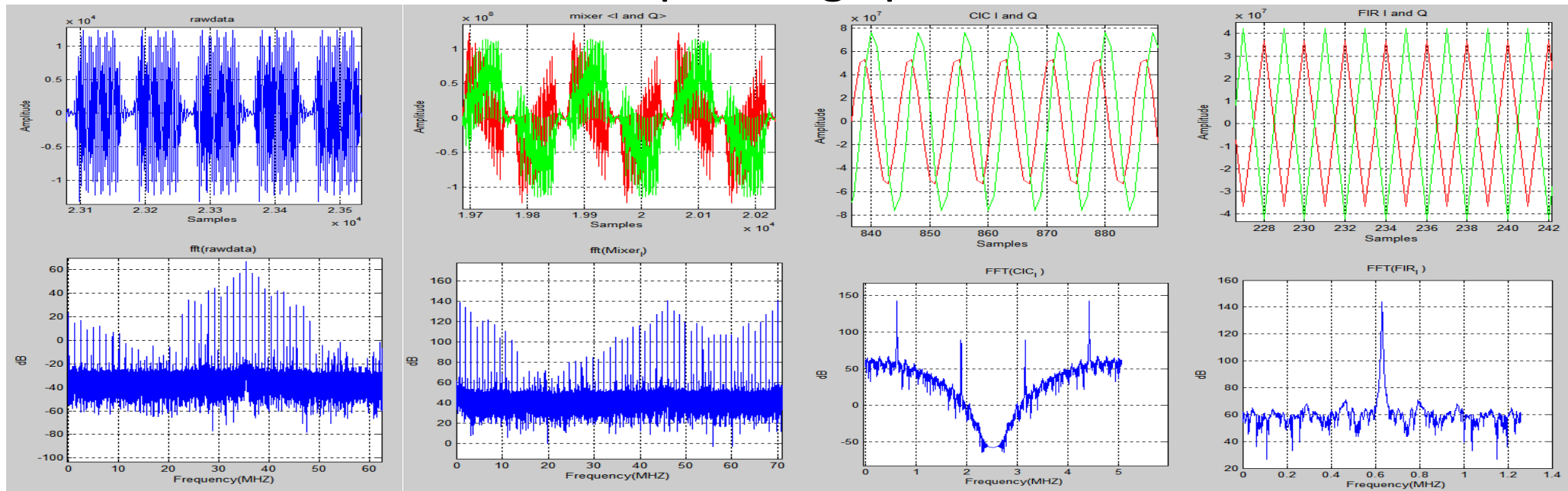


- RF frequency located on the center of ninth Nyquist zone
- Frequency of ADC data located on the center of first Nyquist zone

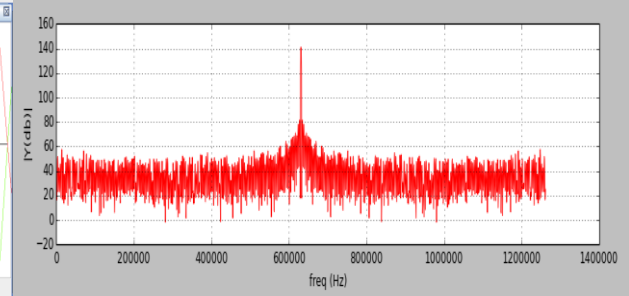
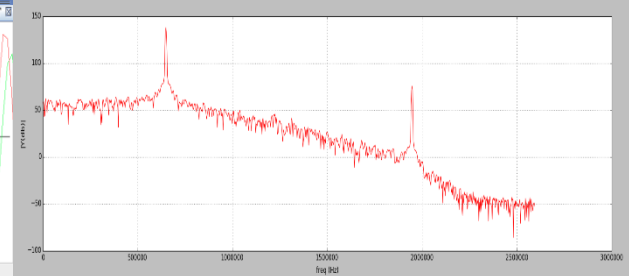
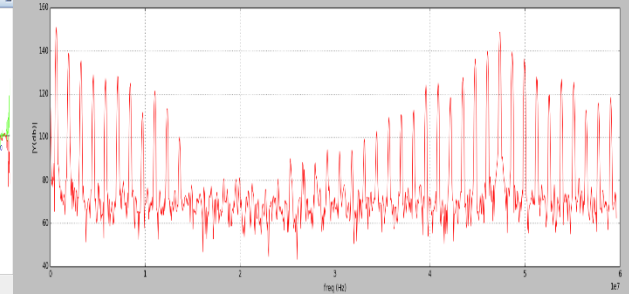
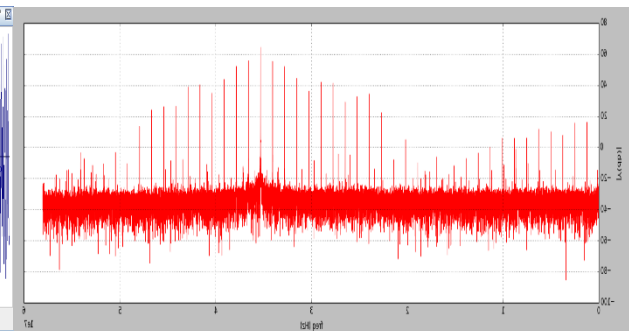
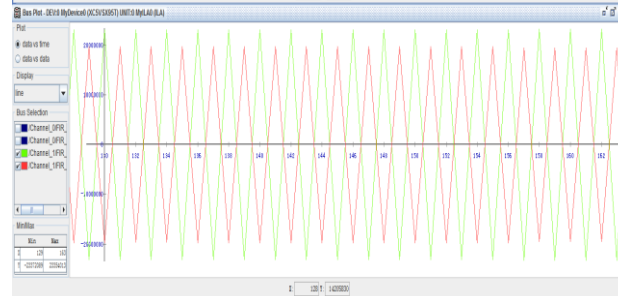
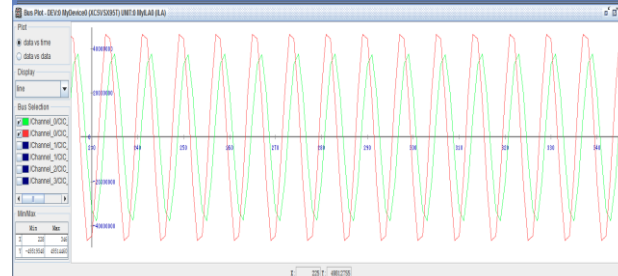
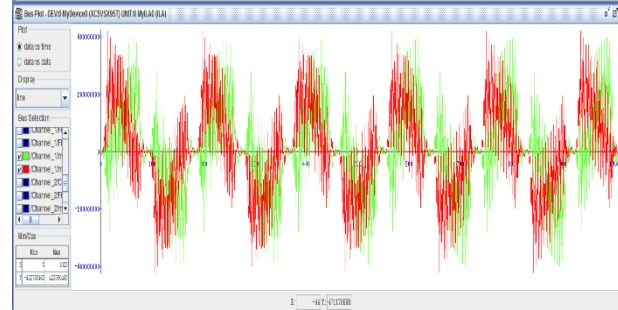
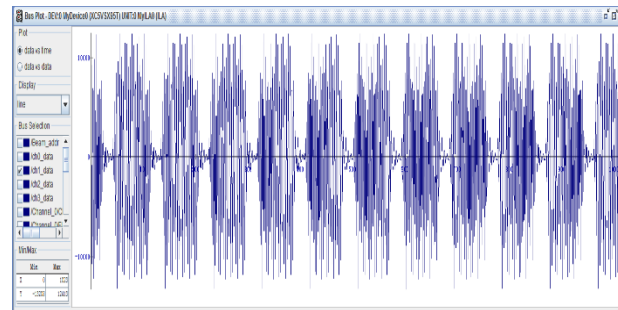
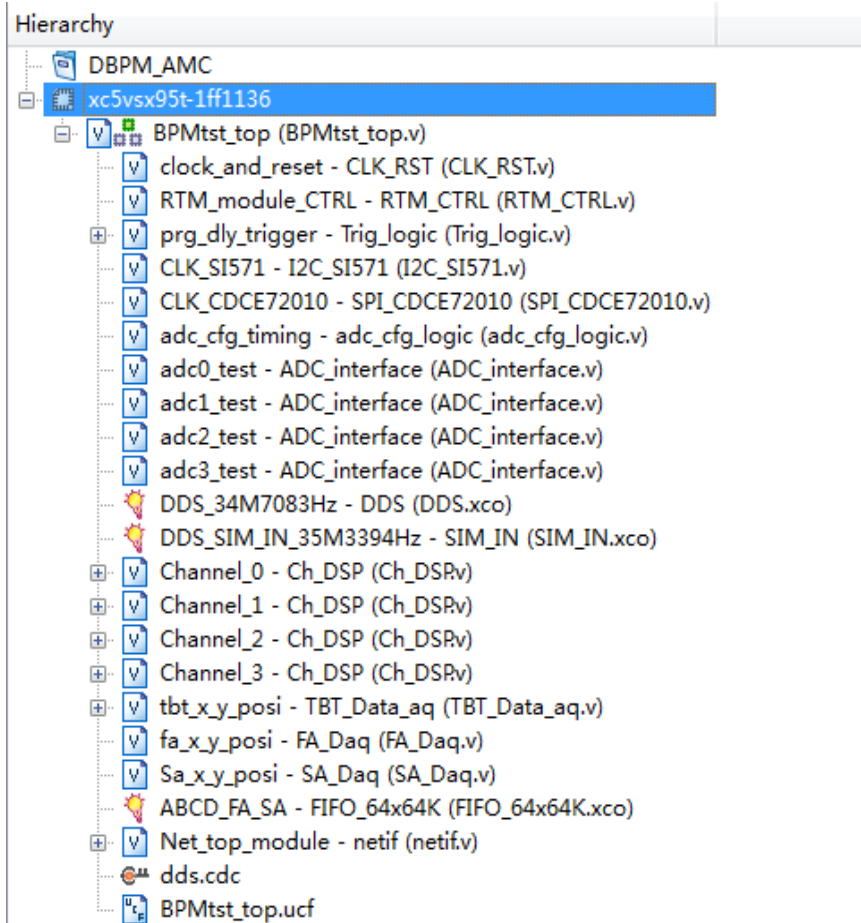
# Algorithm simulation base on matlab



time waveforms and corresponding spectrum:



# Implementation of Algorithm in FPGA



# 4. Software Design

- Software framework

  - Data Acquisition

  - Data Analysis

  - Data Storage

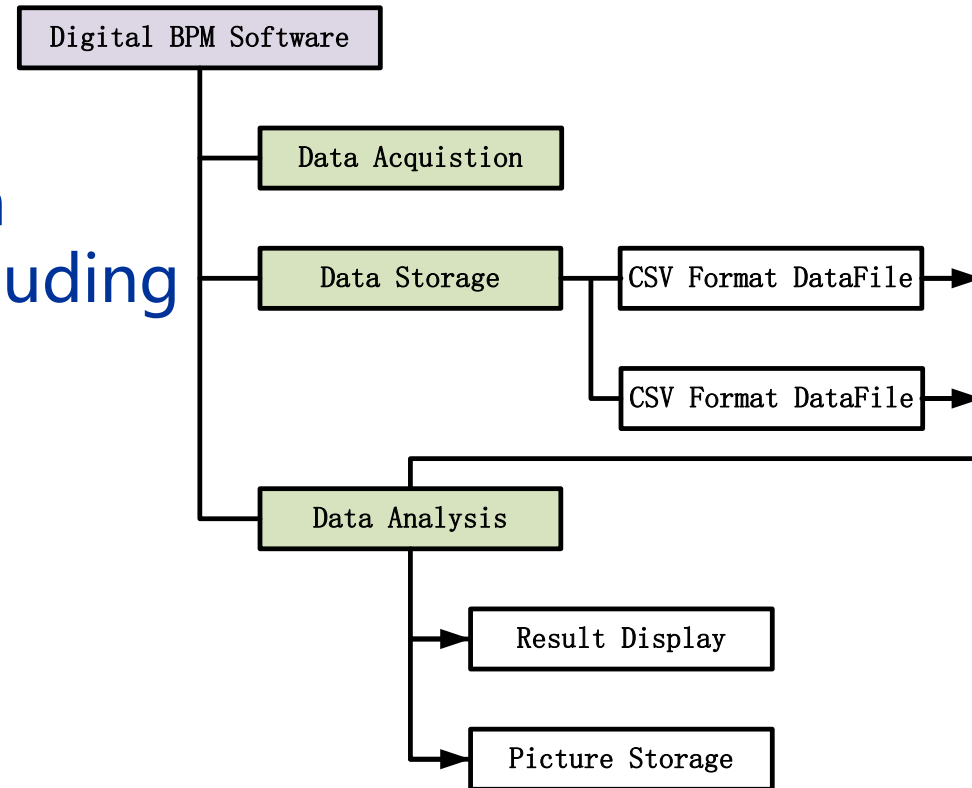


# 4.1 DBPM Software framework

- Software framework include 3 module:
  - Data Acquisition
  - Data Analysis
  - Data Storage

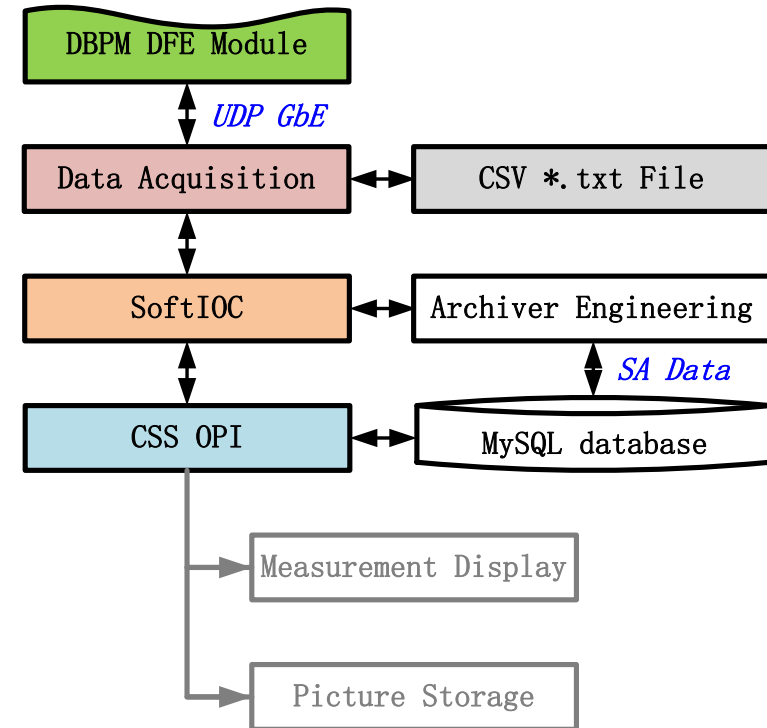
■ The Software is built with Python (2.7.10) tools, including module:

- Scipy1.0
- Numpy
- Pandas
- Matplotlib
- Pyepics
- PyQtgraph



# Data Acquisition Module

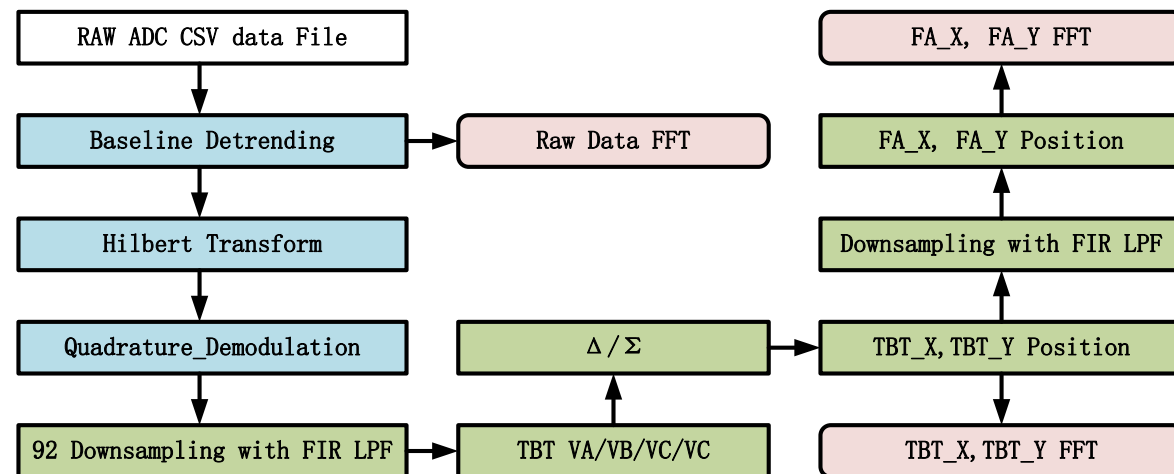
- Data Acquisition process:
  - Drive archiver engine
  - Store the data in the database
  - Display the calculated results or images
  - ...



# Data Analysis Module

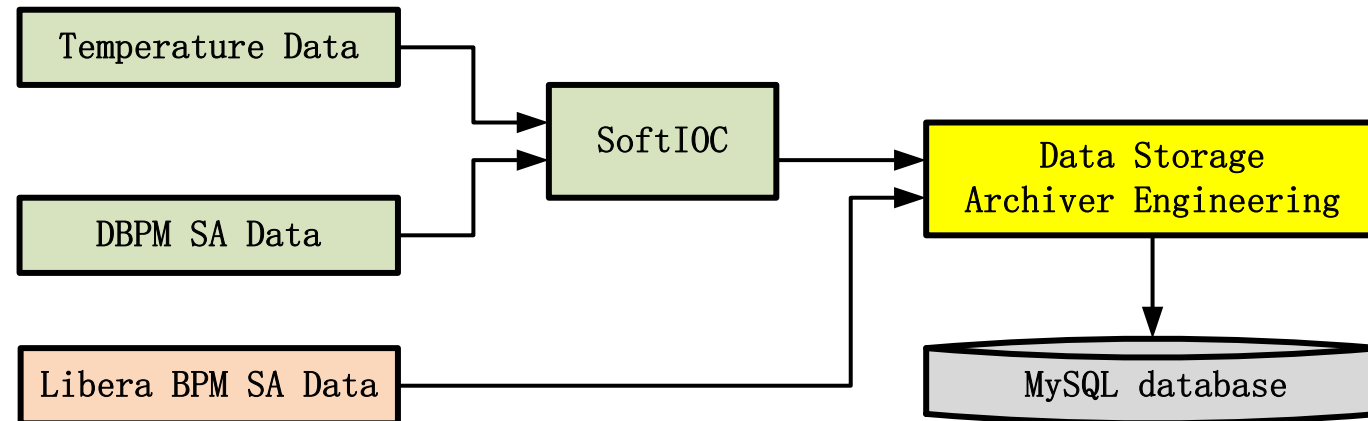
- Data Analysis function:
  - offline implementation of the Hilbert algorithm
  - FFT Analysis.

*Note: The function is check with FPGA implementation.*



# Data Storage Module

- Two forms of data storage :
  - CSV txt format file
  - MySQL database



# 5. DBPM Project tesing

➤ Testing condition in laboratory

➤ Test results in laboratory

✓ Tbt testing

✓ Fa testing

✓ Sa testing

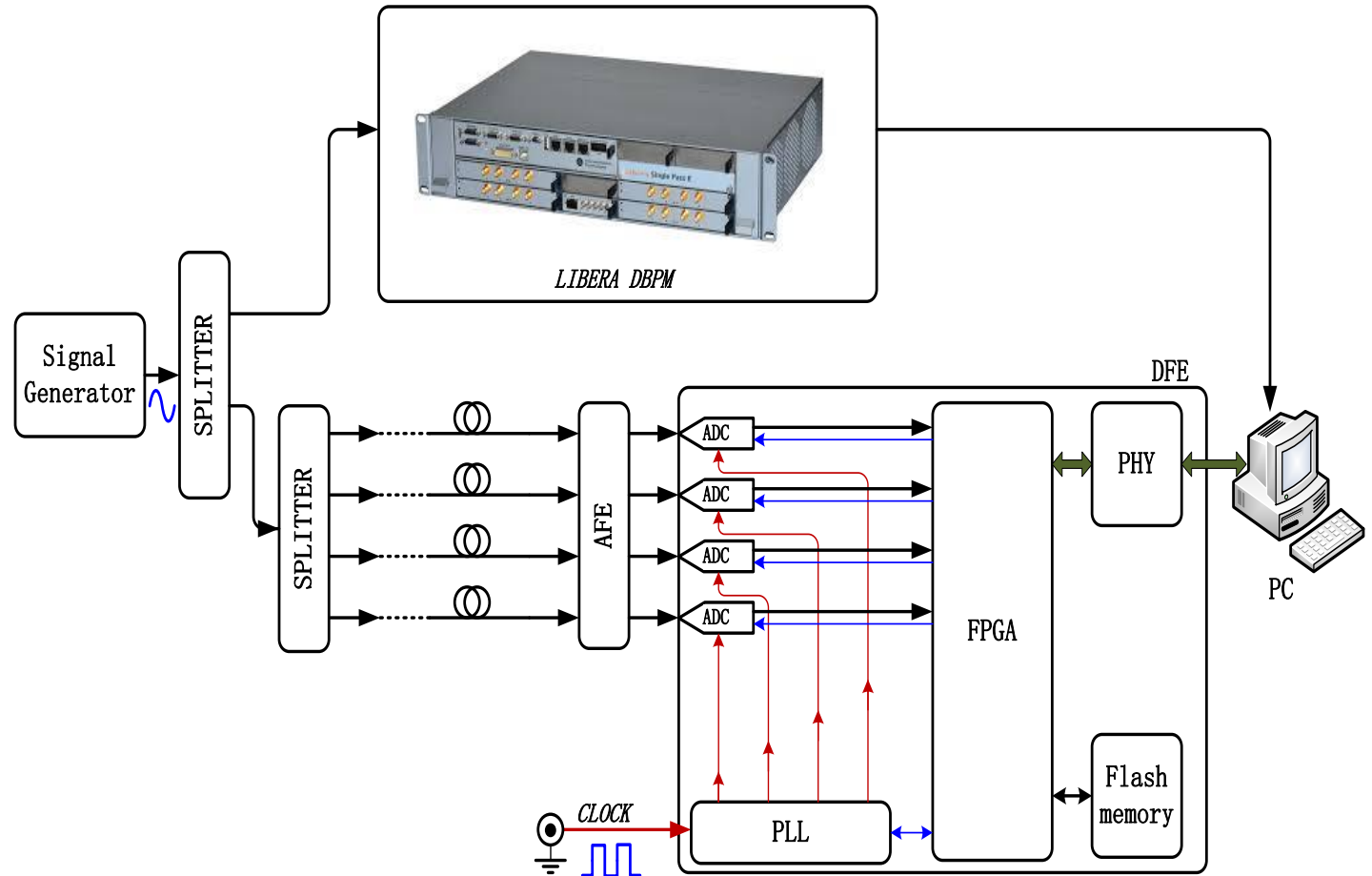
# Testing condition

◆ Signal frequency:

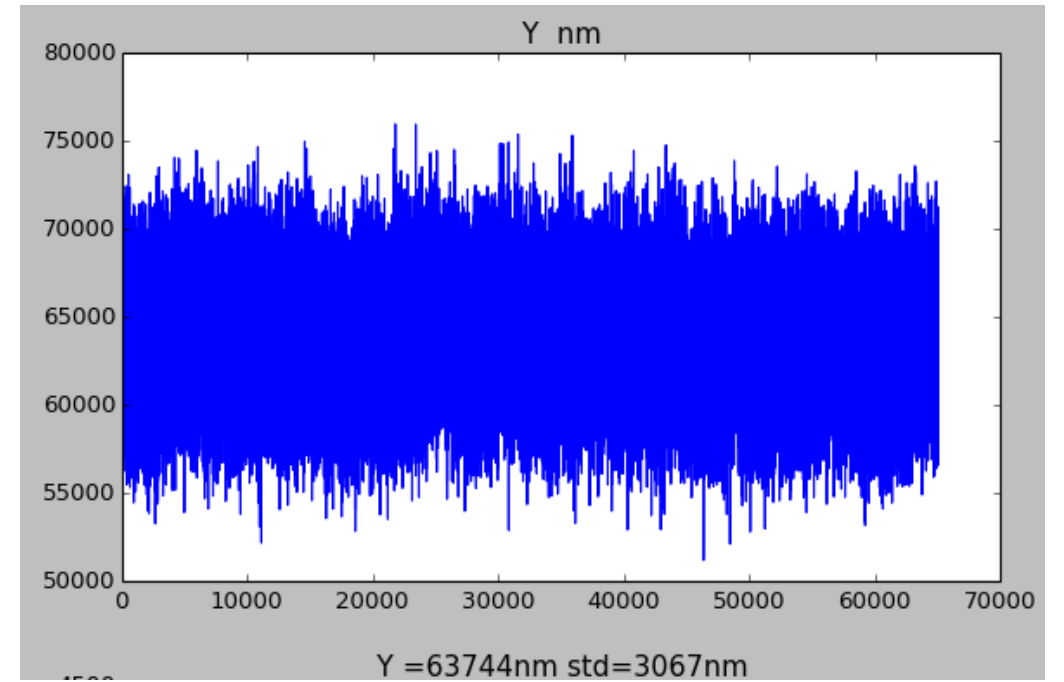
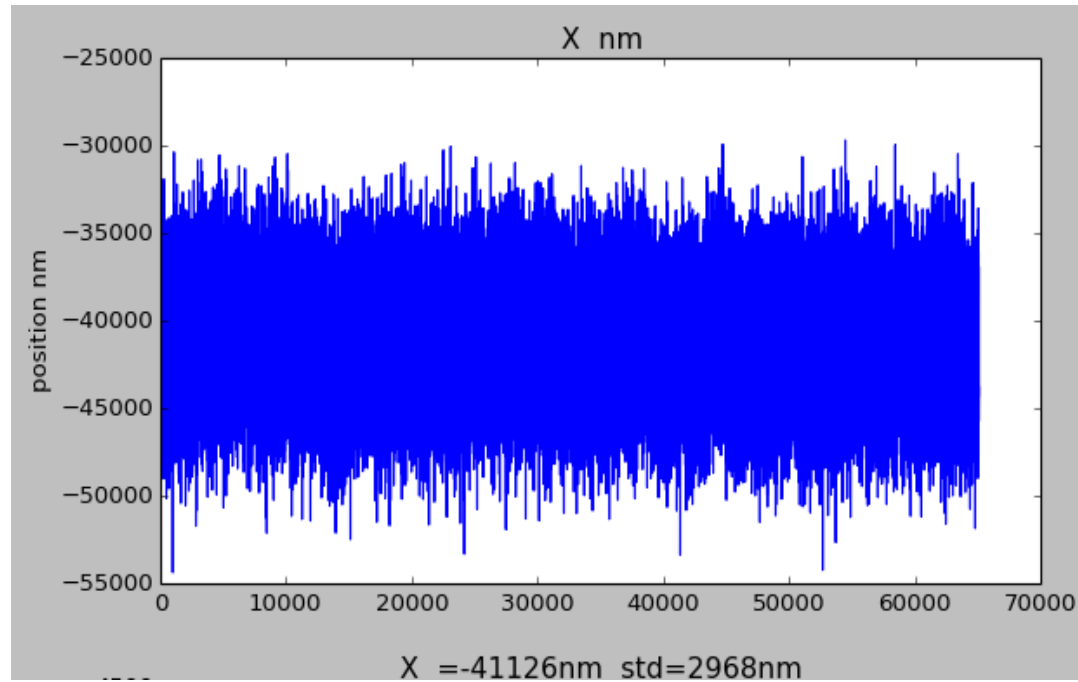
➤ 499.8MHz

◆ signal intensity:

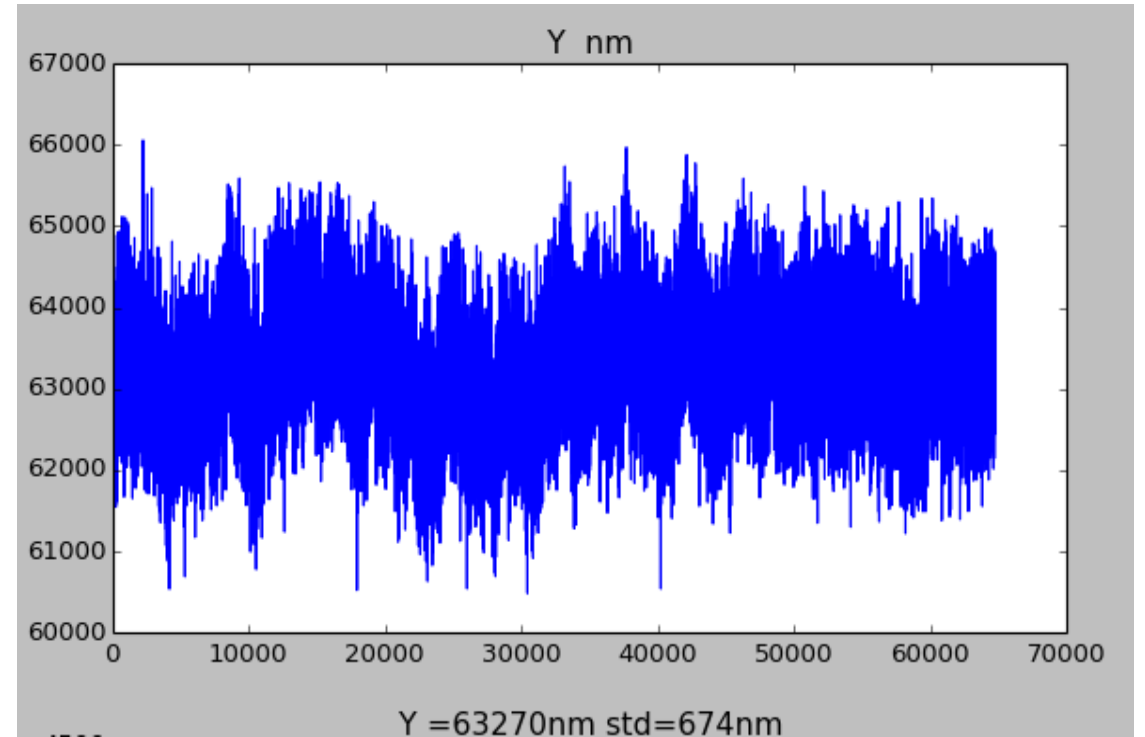
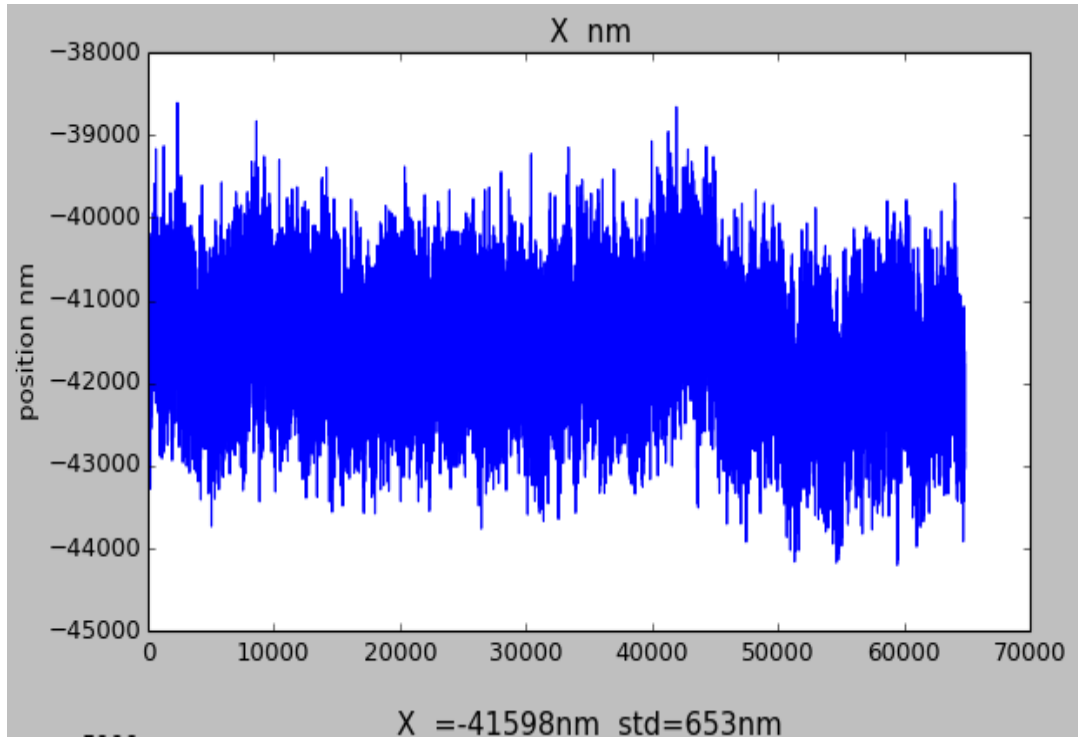
➤ -10dbm



# TBT results in laboratory

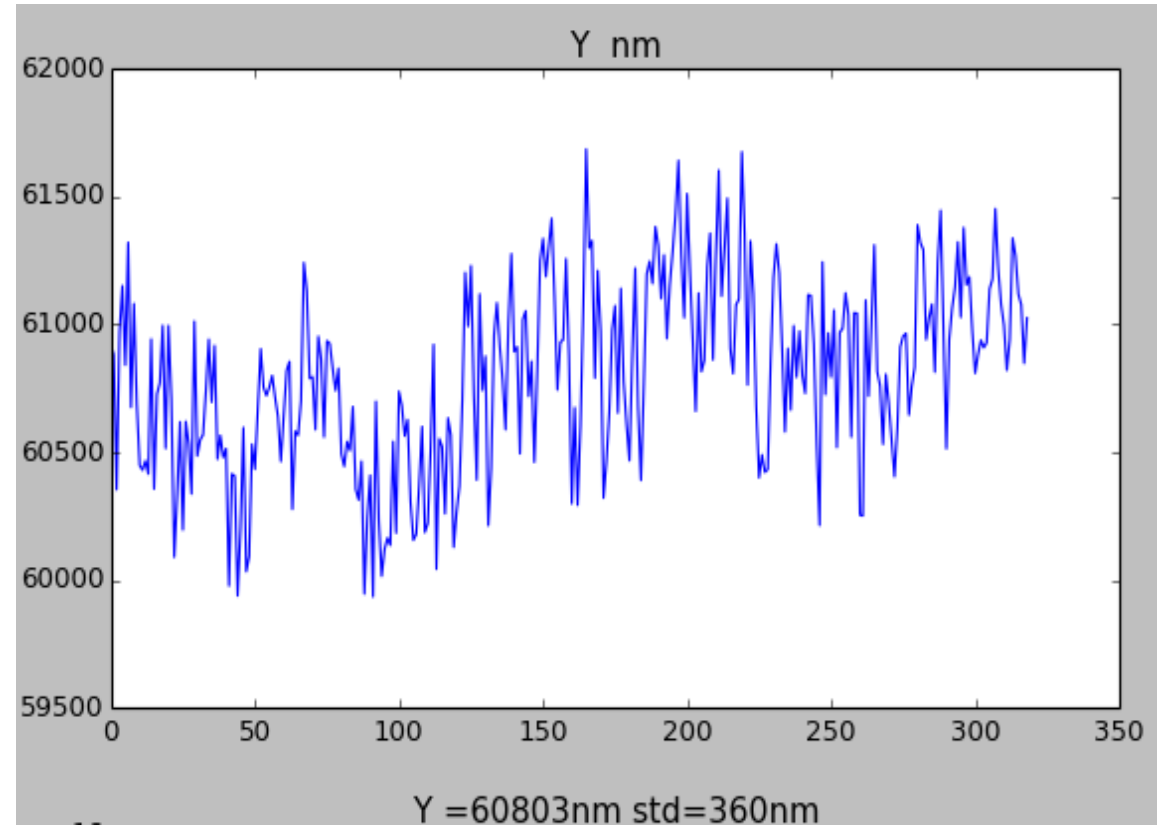
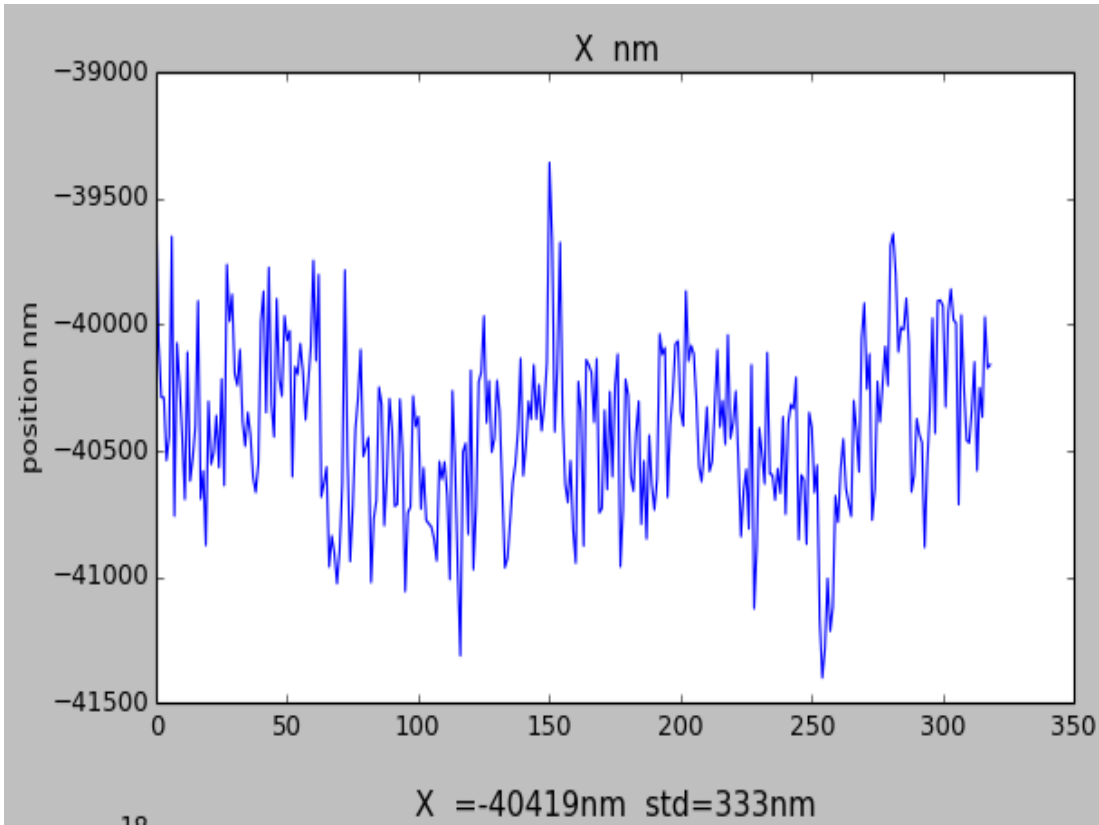


# FA results in laboratory





# SA results in laboratory



Thank you for your  
attention!

Institute of High Energy Physics, CAS, China

