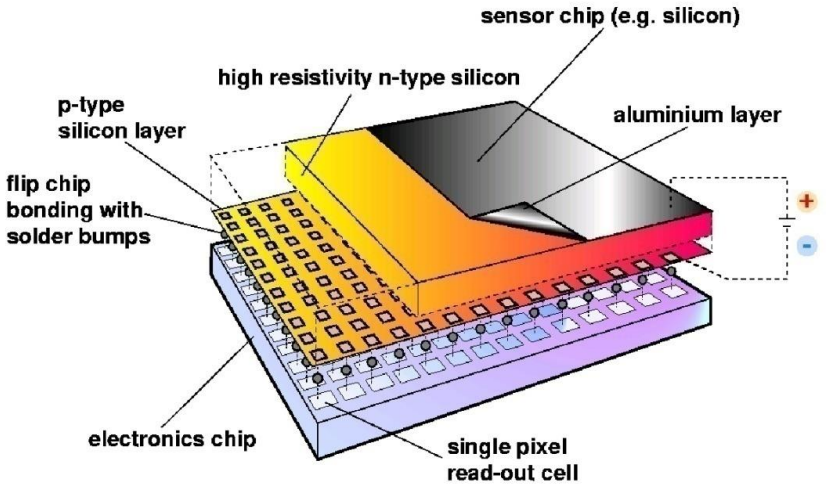
MALTA and LAPA developments

Roberto Cardella, CERN EP-DT-DD

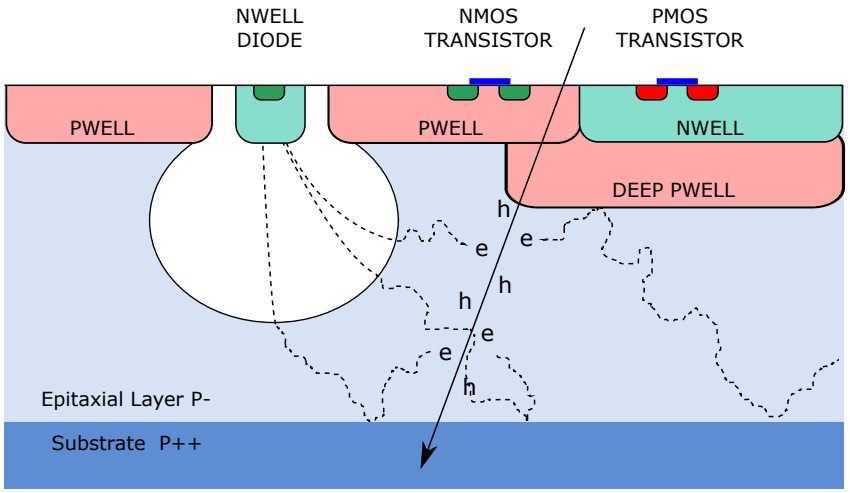
A. Andreazza, A. Calandri, M. Benoit, I. Berdalovic, B. Blochet, J. Bronuzzi, R. Casanova, V. Dao, N. Egidos, F. Ehrler, F. Ferraz, E. Gamberini, S. Gonzalez, S. Kuehn, T. Kugathasan, A.Mapelli, C. Marin Tobon, S. Monzani, M. Moreno Llacer, K. Moustakas, I. Peric, H. Pernegger, P. Riedler, J. Rousset, C. Riegel, R. Schimassek, E.J. Schioppa, B. Schlager, A. Sharma, L. Simon Argemi, W. Snoeys, C. Solans Sanchez, E. Vilella, T. Wang, N. Wermes, E. Zaffaroni

Silicon Pixel Detector

Hybrid

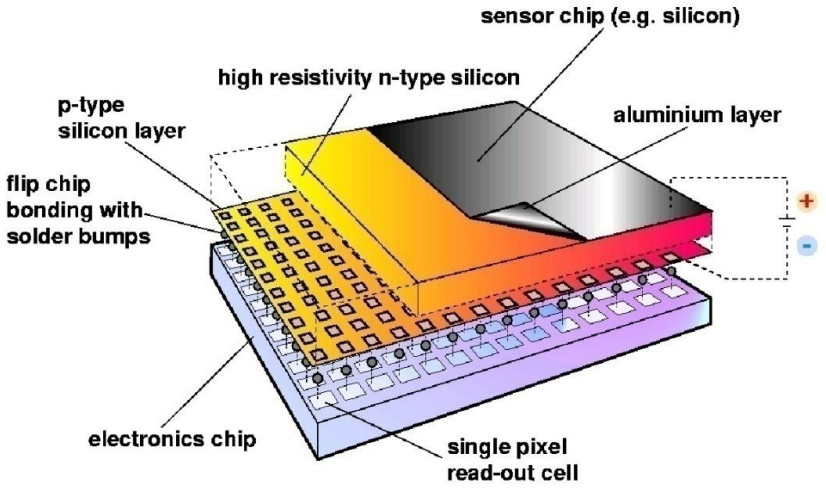


Monolithic

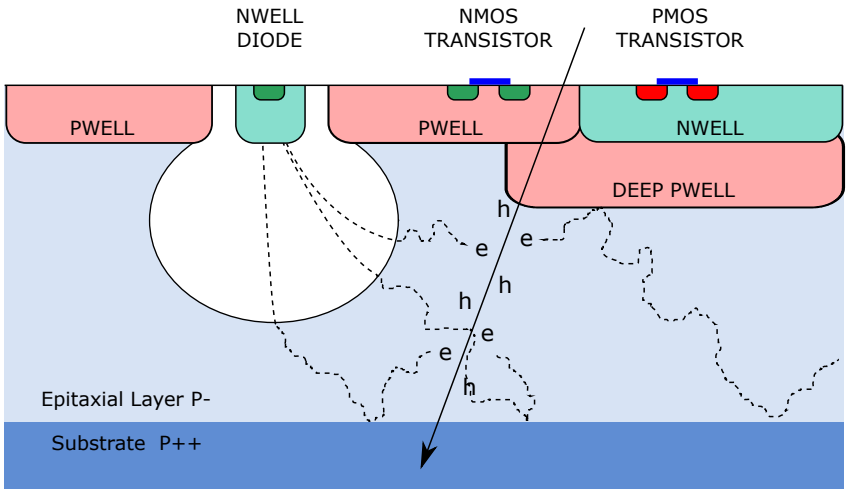


Silicon Pixel Detector

Hybrid

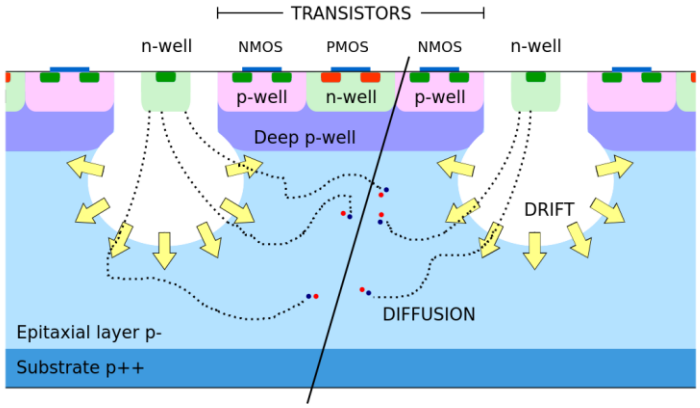


Monolithic

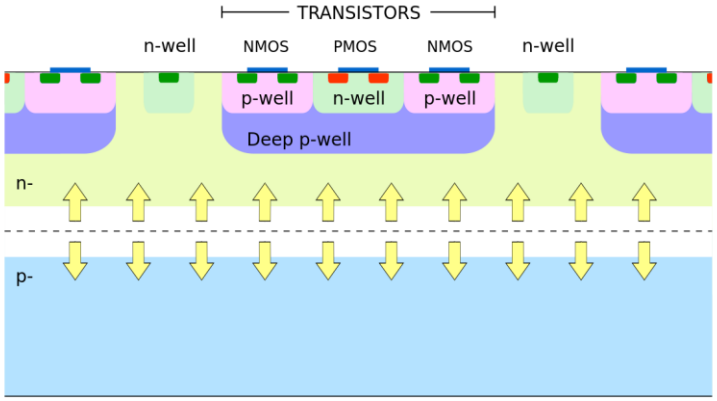


$$d \propto \sqrt{\rho V}$$

TowerJazz process



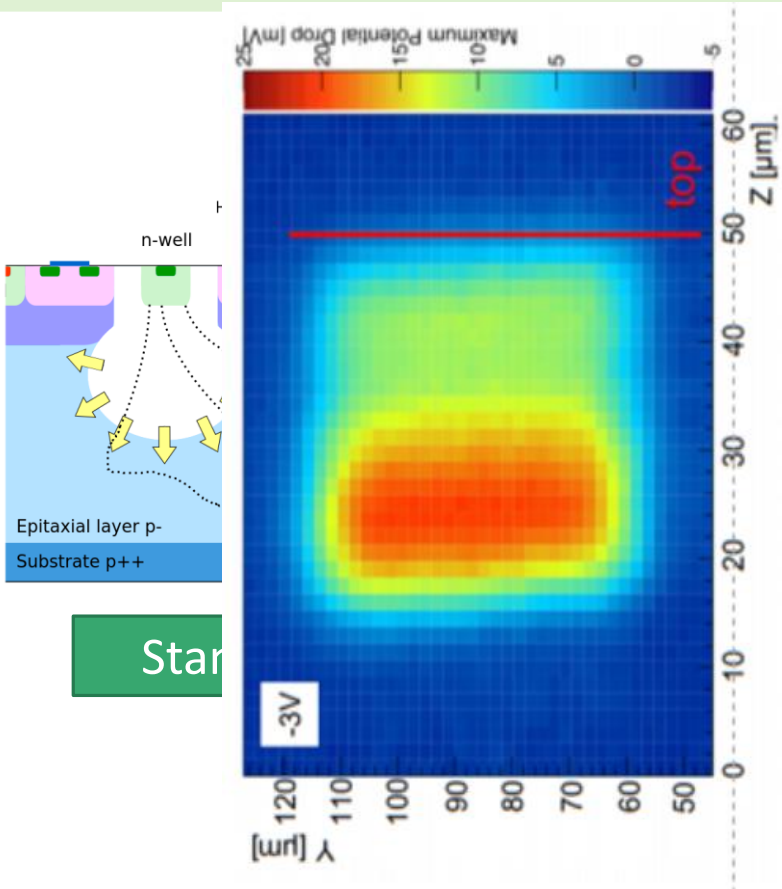
Standard TJ process



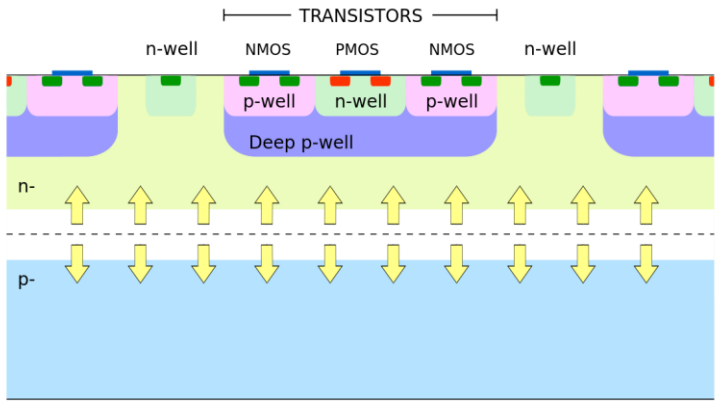
Rad hard TJ process

W. Snoeys et al., NIM A 871C (2017) pp. 90-96, DOI: 10.1016/j.nima.2017.07.046

TowerJazz process



Star



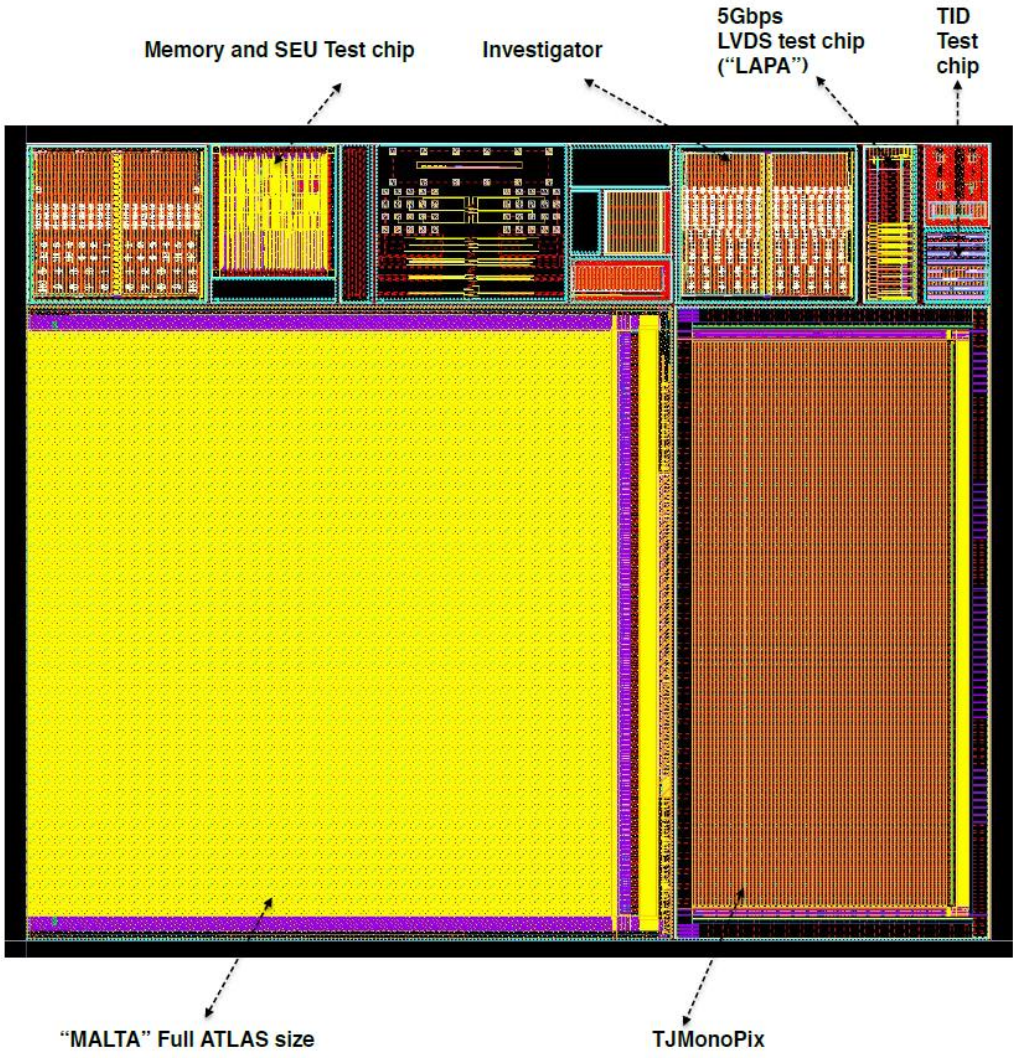
Rad hard TJ process

Expected full depletion and radiation hard up to 10^{15} n_{eq}/cm^2

http://iopscience.iop.org/article/10.1088/1748-0221/12/06/P06008/meta

DD SECTION MEETING

TJ large-scale demonstrators

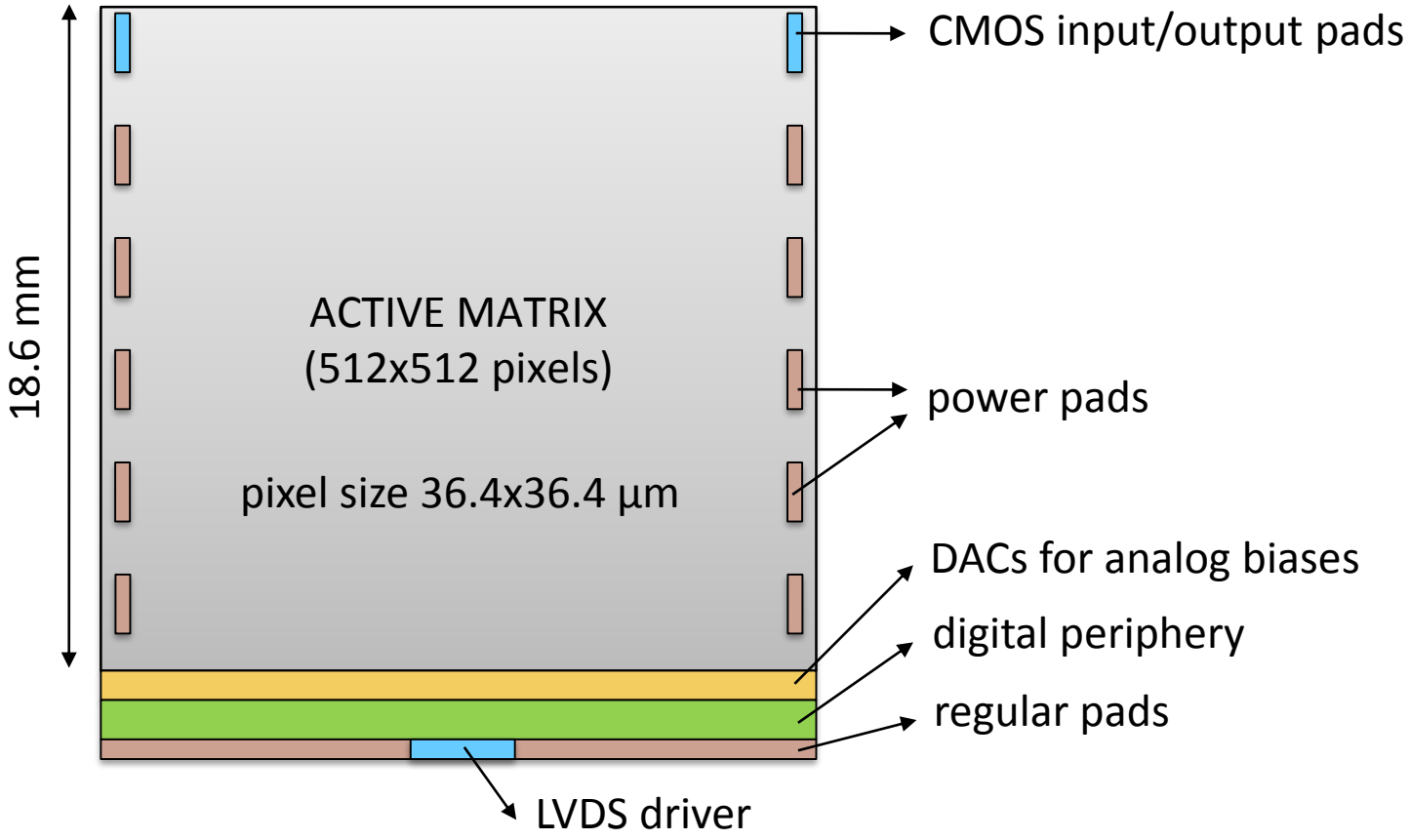


- The "TJ-Monopix" chip
  - Front-end similar to the "MALTA" chip
  - Uses the well-established column drain readout architecture (experience from LF-Monopix design)
- The "MALTA" chip
  - Analog front-end based on a previous design for the ALICE experiment
  - Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix

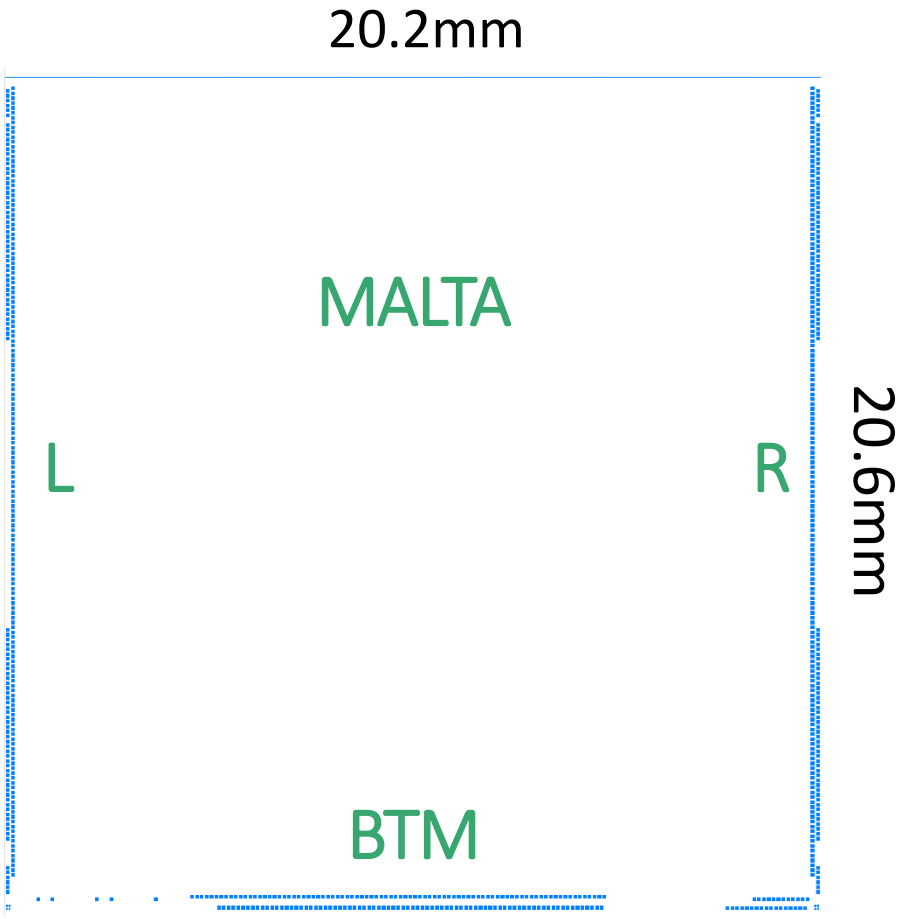
The “MALTA” chip

“MALTA” Monolithic from ALICE To ATLAS

- 8 sectors (different collection electrode size and deep PWELL spacing)



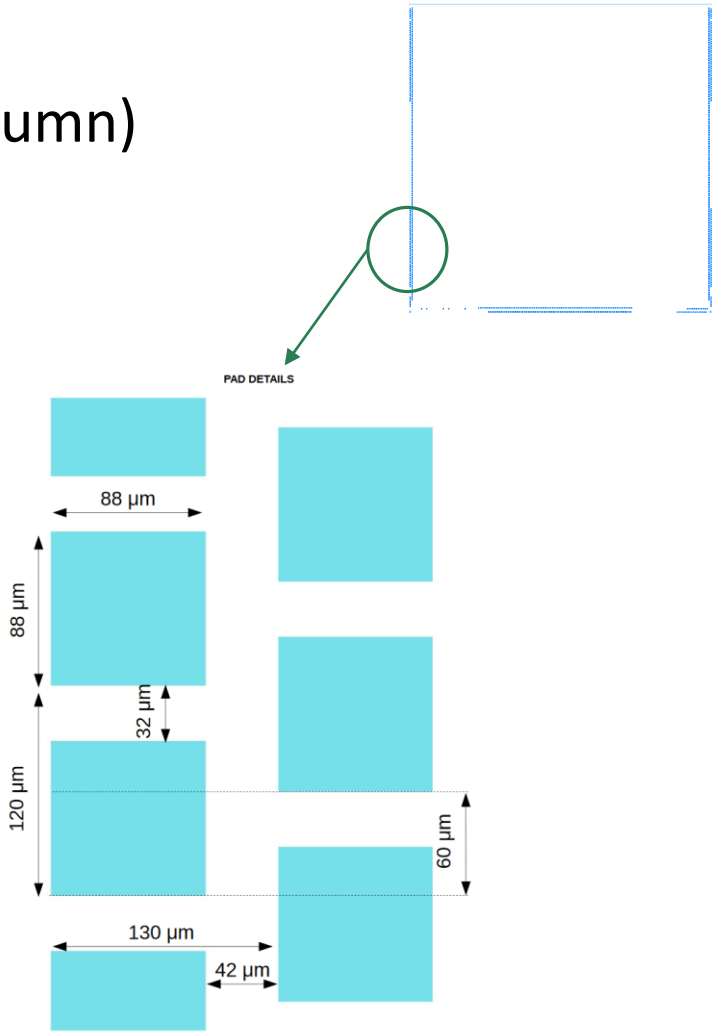
MALTA FOOTPRINT



738 pads with 120um pitch

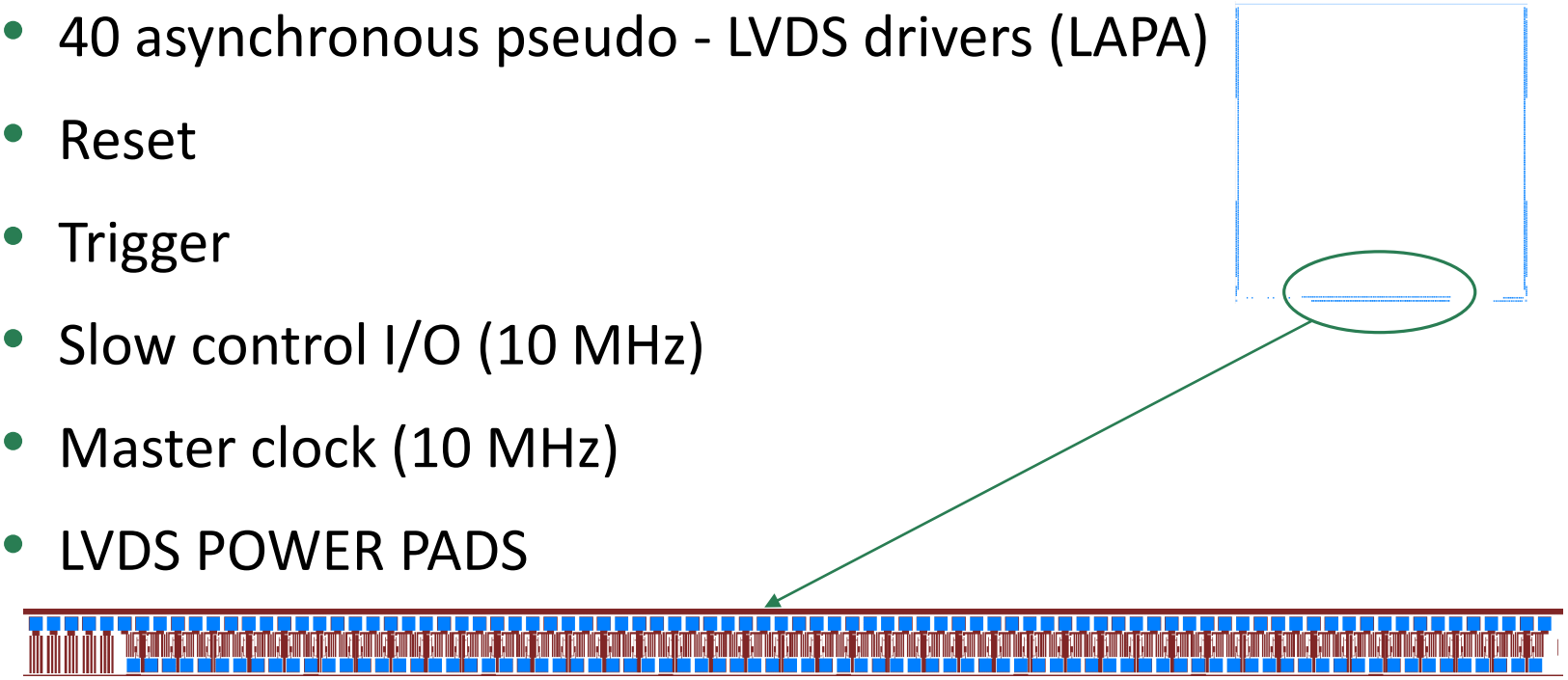
MALTA SIDE PADS

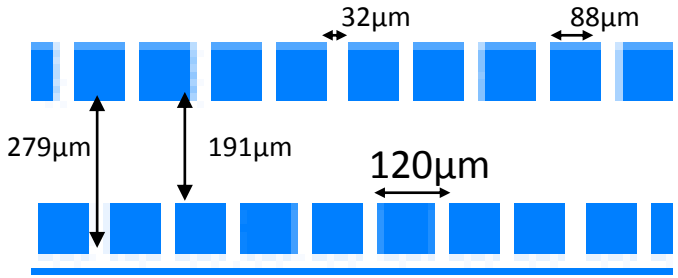
- Chip2Chip com. I/O CMOS (ext. column)
  - 40 Left top
  - 40 Left bottom
  - 40 Right top
  - 40 Right bottom
- Power pads (int. column)
  - DVDD
  - AVDD
  - DACVDD
  - SUB
  - PWELL



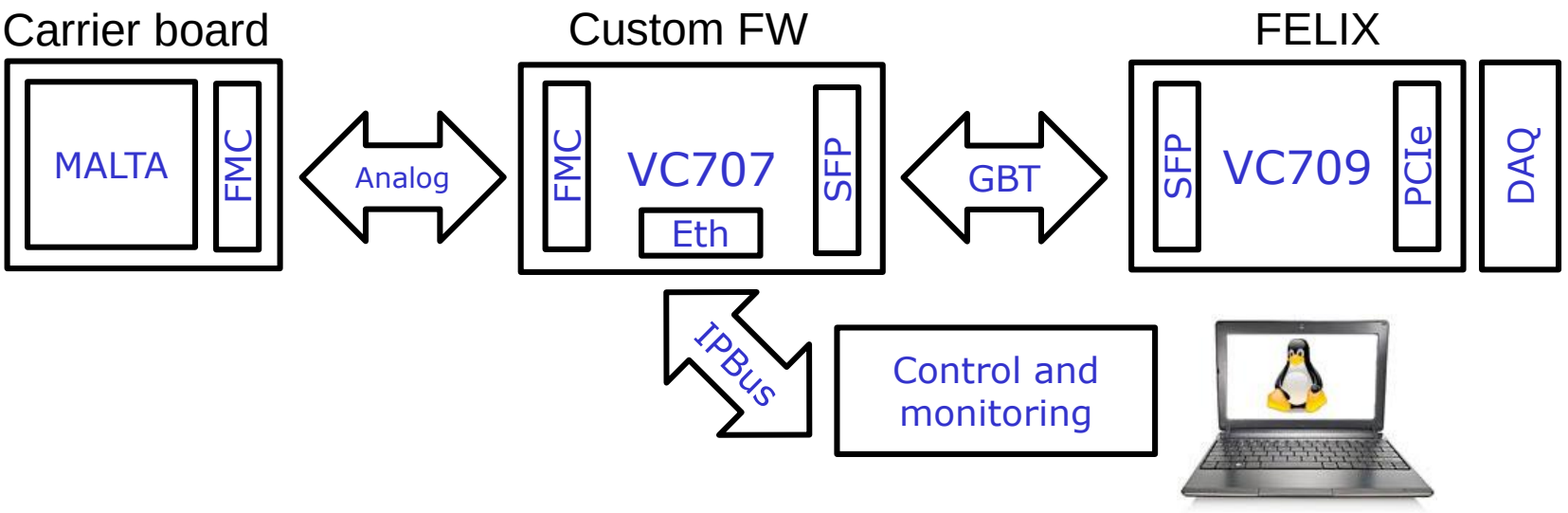
MALTA BOTTOM

- 40 asynchronous pseudo - LVDS drivers (LAPA)
- Reset
- Trigger
- Slow control I/O (10 MHz)
- Master clock (10 MHz)
- LVDS POWER PADS





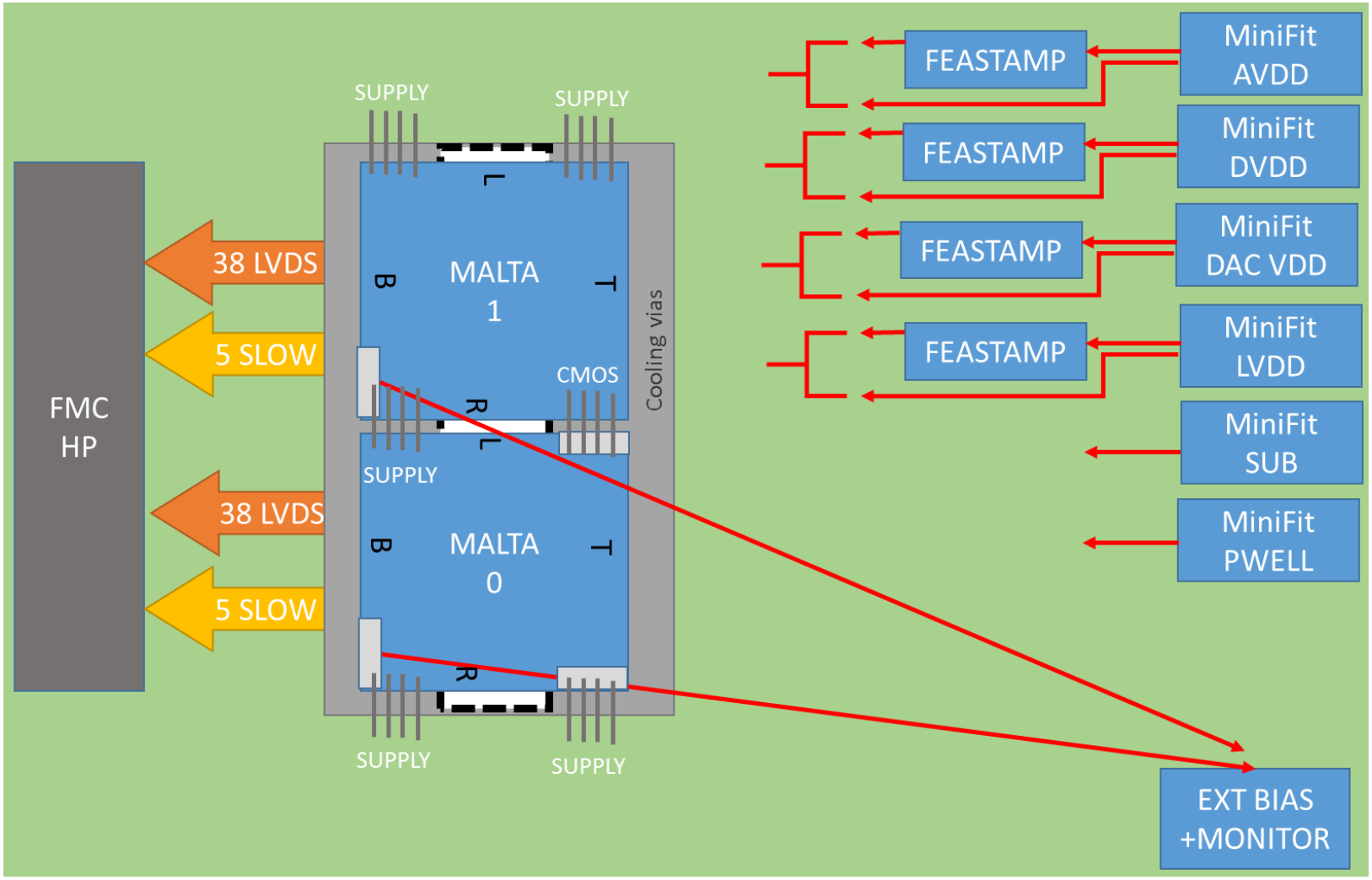
MALTA Read-out system



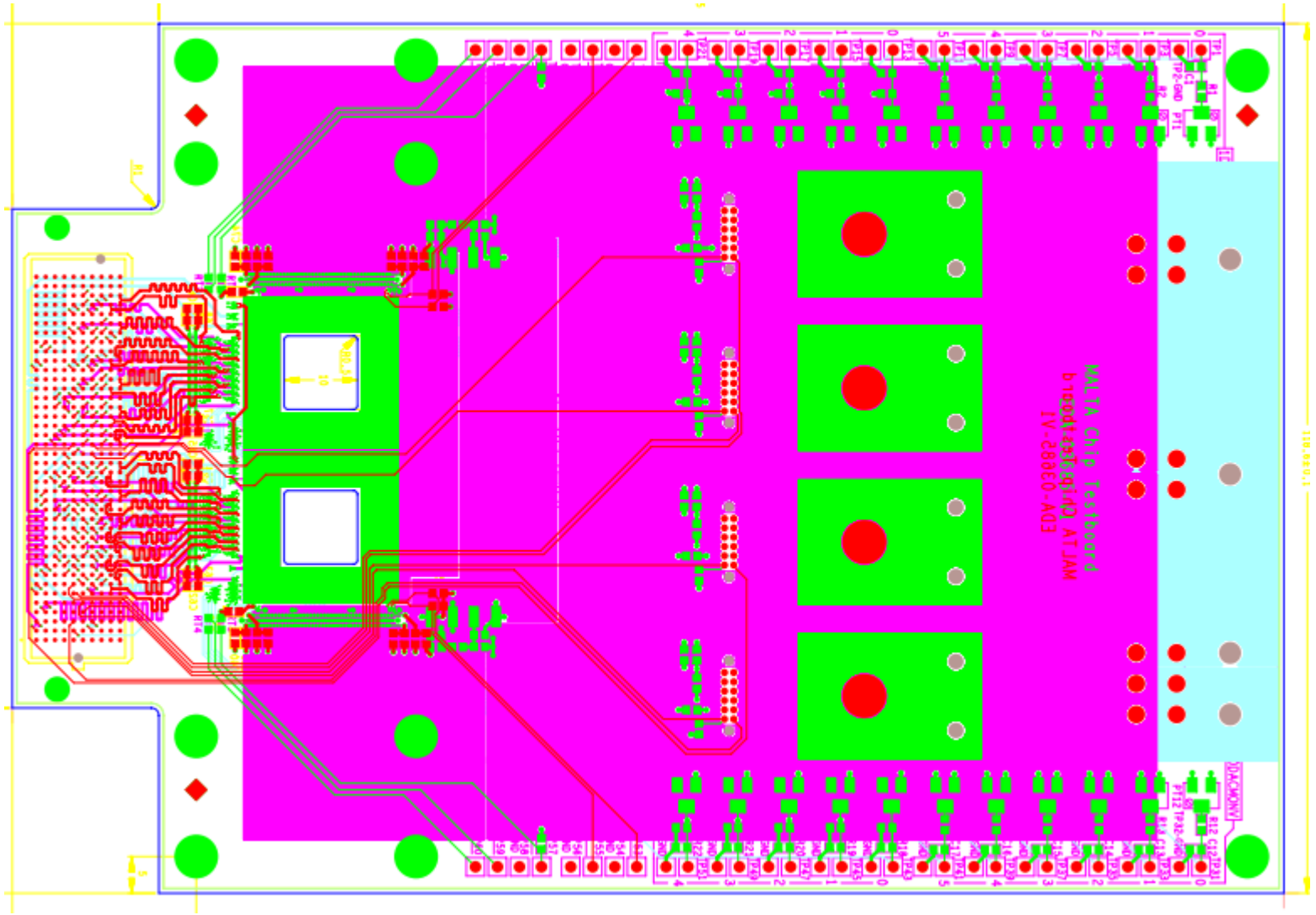
- Carrier board for two MALTA chips with FMC interface
- Asynchronous oversampling on Xilinx VC707 board
- Slow read-out through IPbus ethernet to Linux PC running SLC6
- Fast read-out through GBT optical link with FELIX + ITK SW

R. Cardella, V. Dao, C. Marin Tobon, E.J.Schioppa, B. Schlager, L. Simon Argemi, C. Solans Sanchez

Carrier board - Dual chip



Carrier board - Dual chip

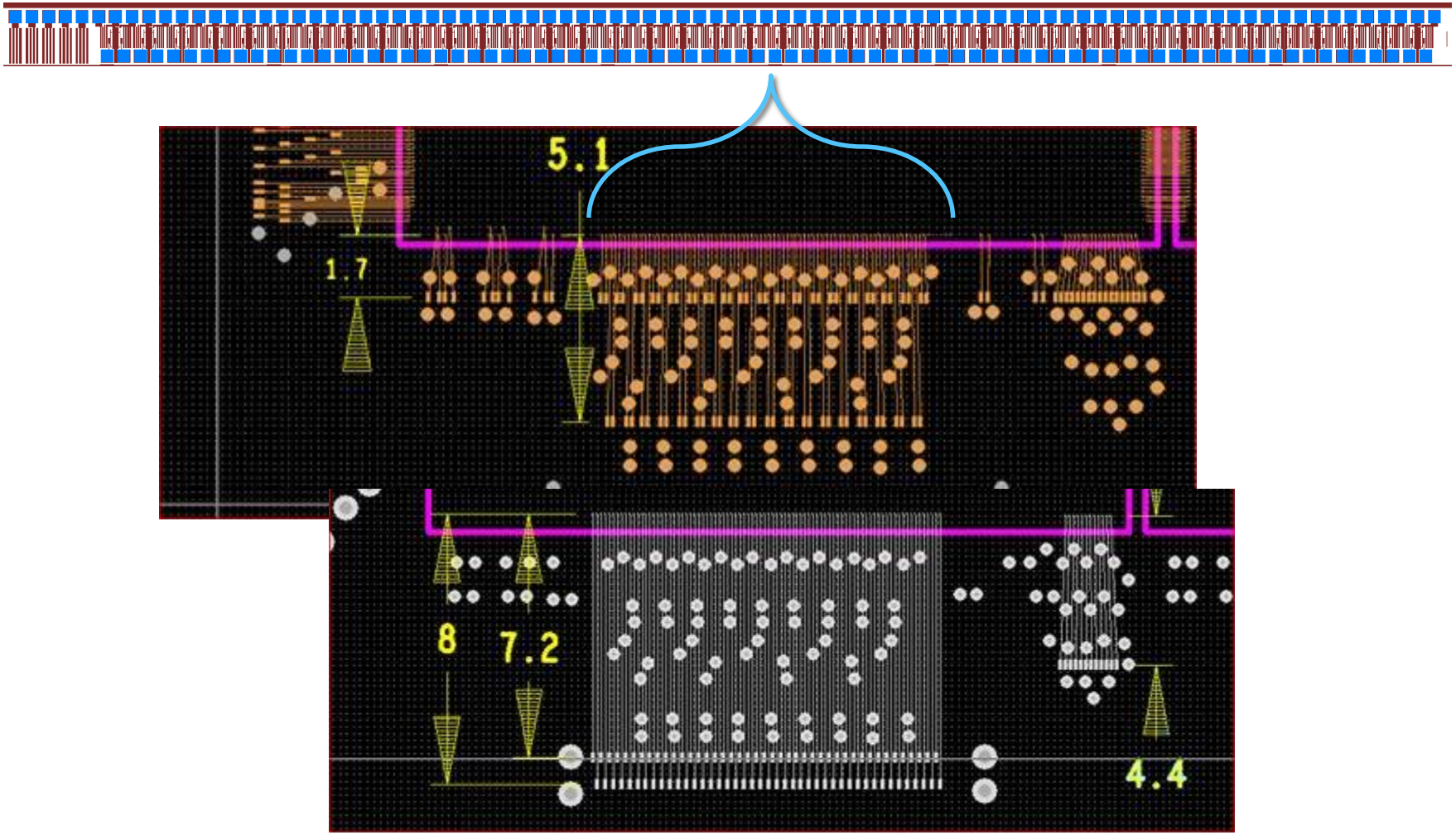


P. Vulliez, W. Billereau – EDA service

MALTA output challenges

40 Pad at 120 µm pitch

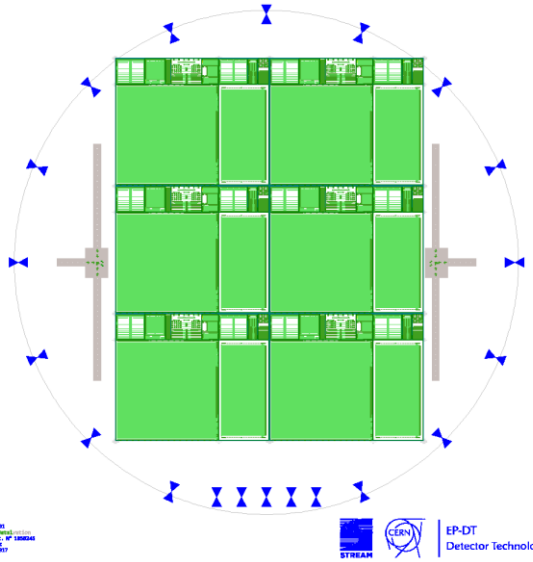
MALTA LVDS wiring



Thanks to I.Mcgill and F.Manolescu for feedback

Assembly test - MALTA carrier board

- Dummy wafer production at CMI, with EP-DT group.
  - 10 wafer of 4” , 6 reticles of TJ STREAM submission.
  - Modified Top internal connection Left-Right for CMOS pads.
  - Pad opening.
  - Thinned to 100um.
- ~70% of the chips available for connection tests.
- 3 wafer already diced.



J. Bronuzzi, A. Mapelli, P. Riedler

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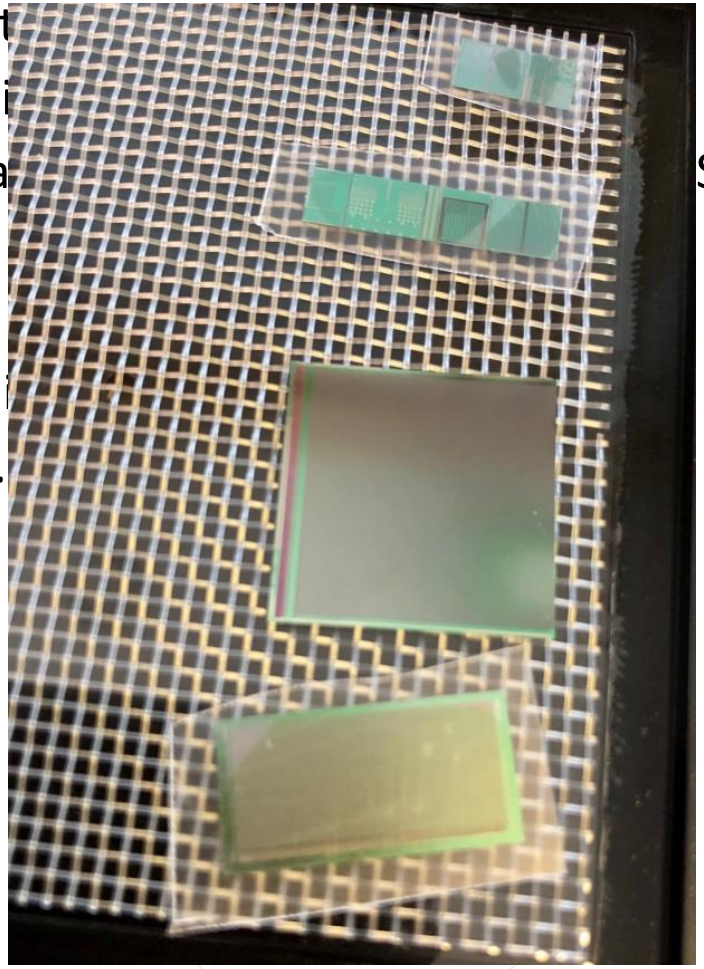

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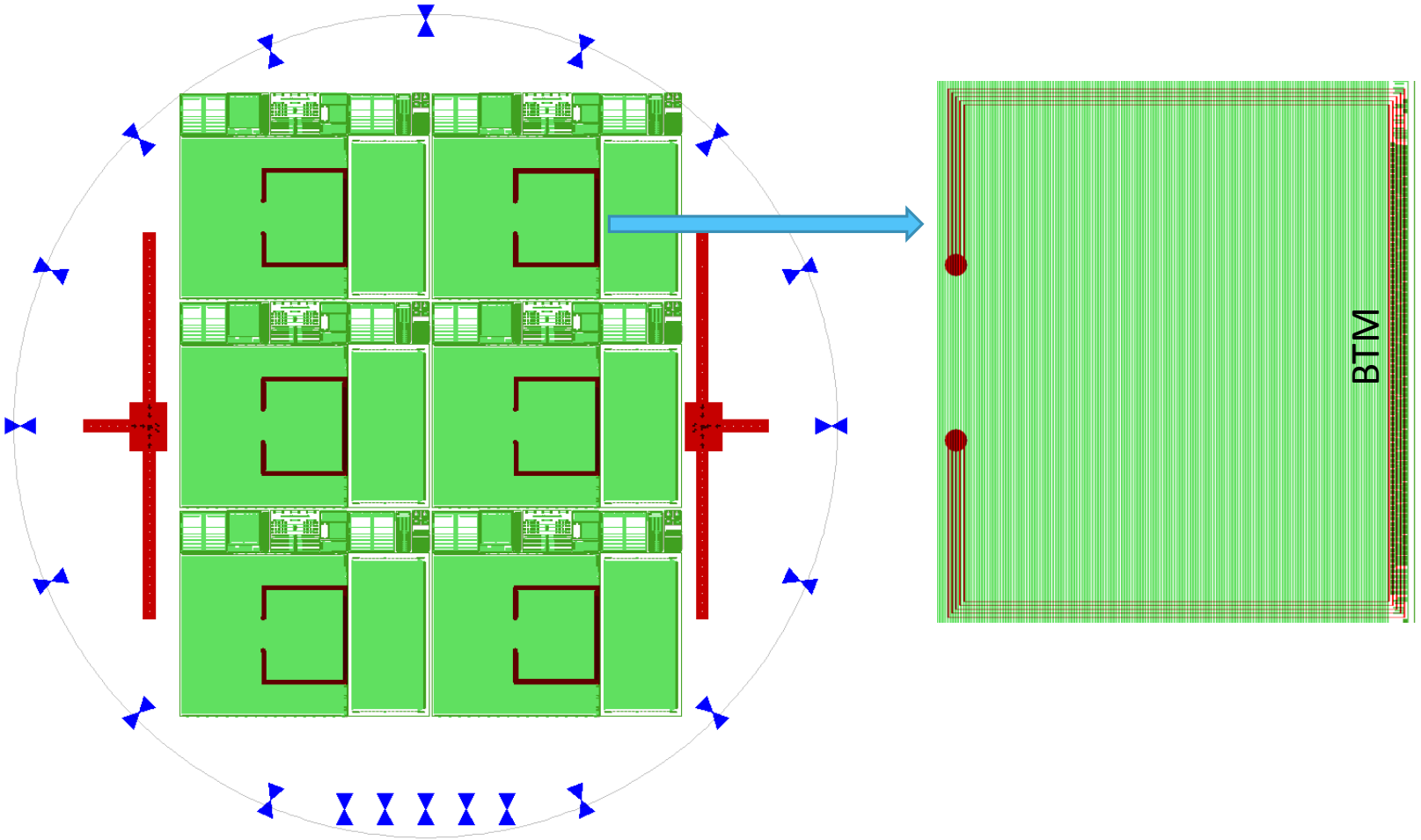
CMOS and Microchannel



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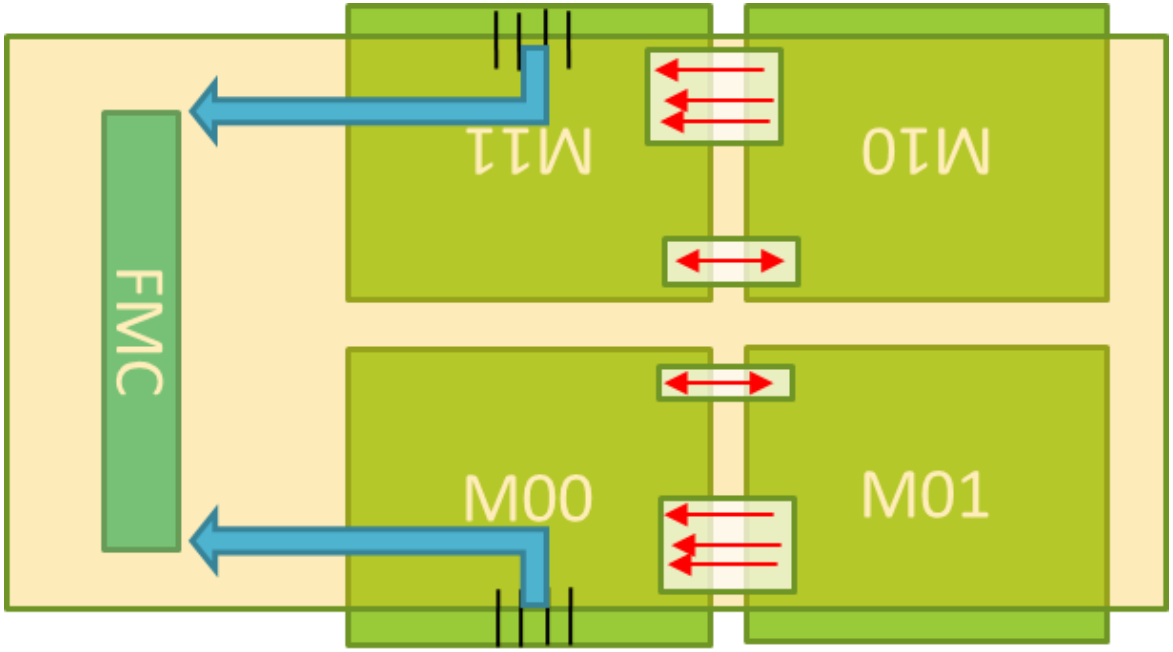
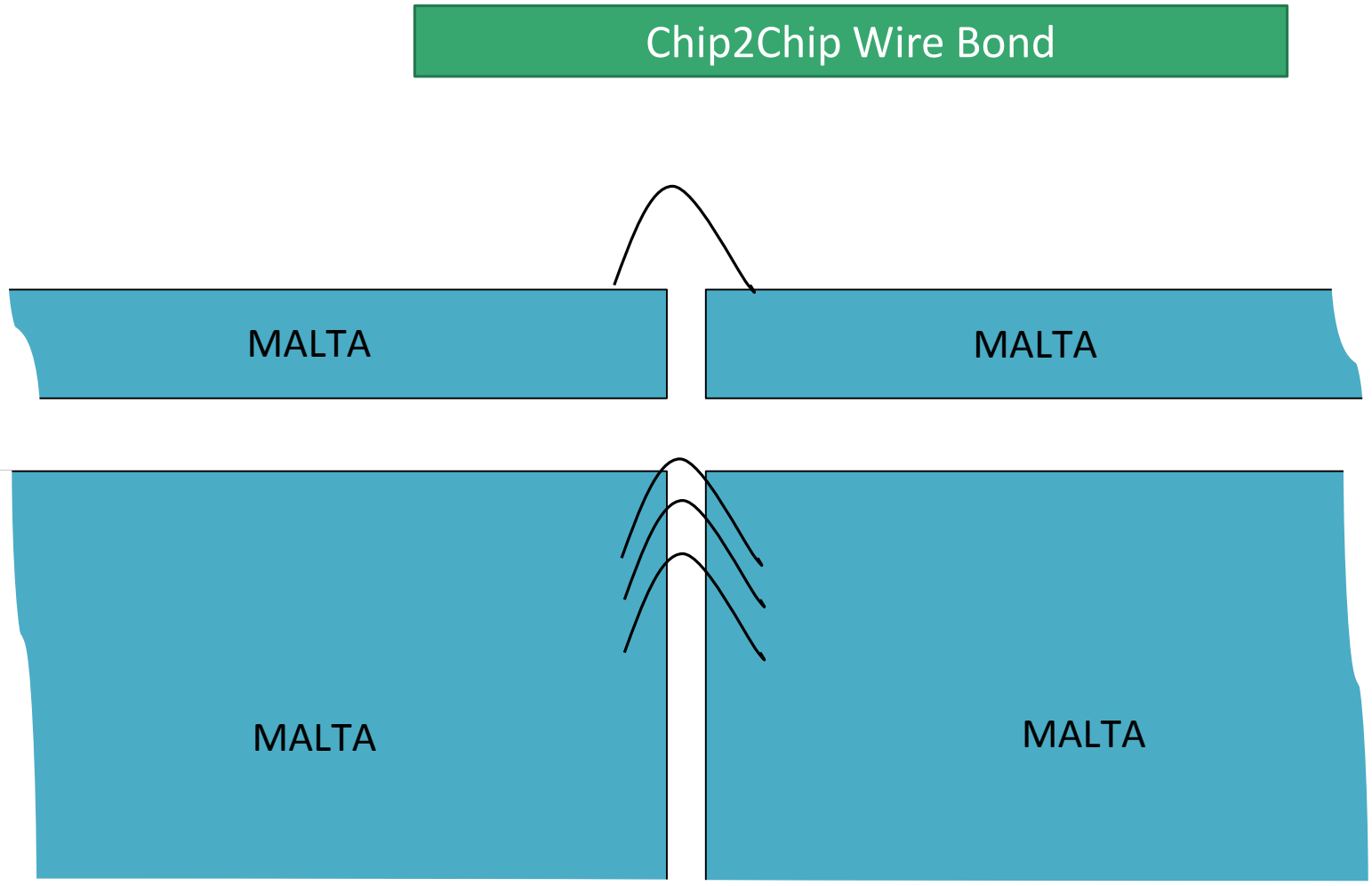
MALTA quad module

- 4 MALTA chips with one flex circuit
- fully matching ATLAS pixel envelope, compatible with L5



Design started with University of Milano

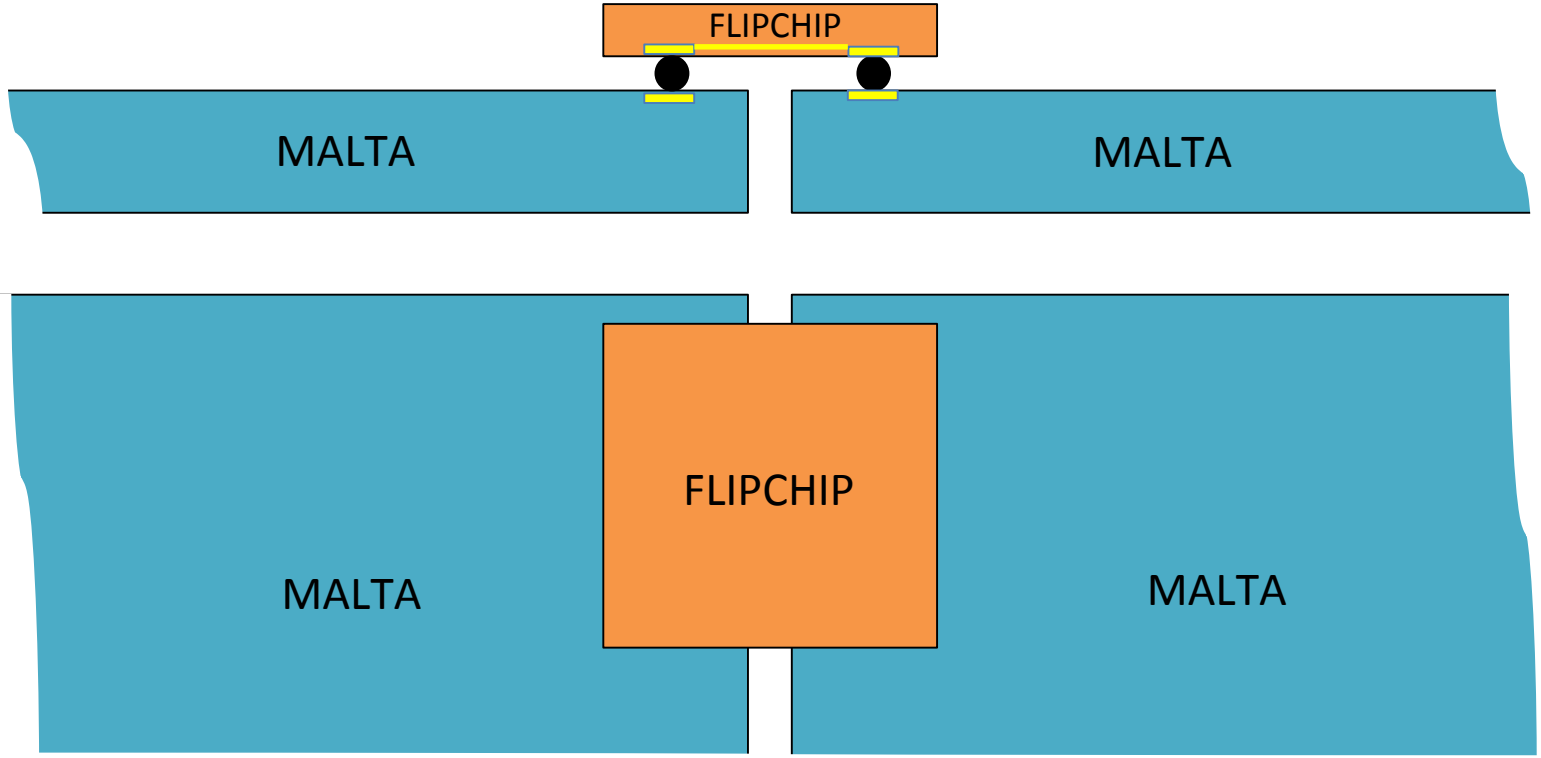
Chip2Chip Communication



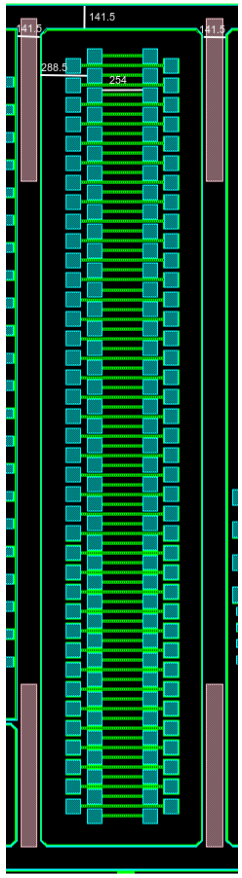
Chip2Chip Communication

Exploring other techniques, such as flip chip bonding

- Possibility to include additional circuitry
- Mechanical connection
- Very precise alignment



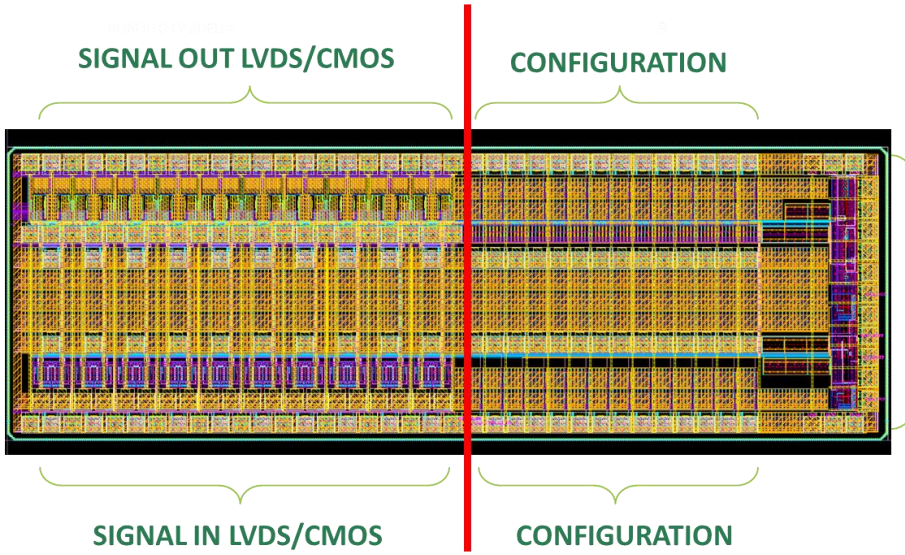
FLIPCHIP



LAPA TEST CHIP

- 10 data transmission channels
  - CMOS/LVDS selectable in
  - CMOS/LVDS selectable out
  - 5 Gb/s LVDS I/O
- Output common mode feedback lock
- Selectable input 100 Ω termination resistor

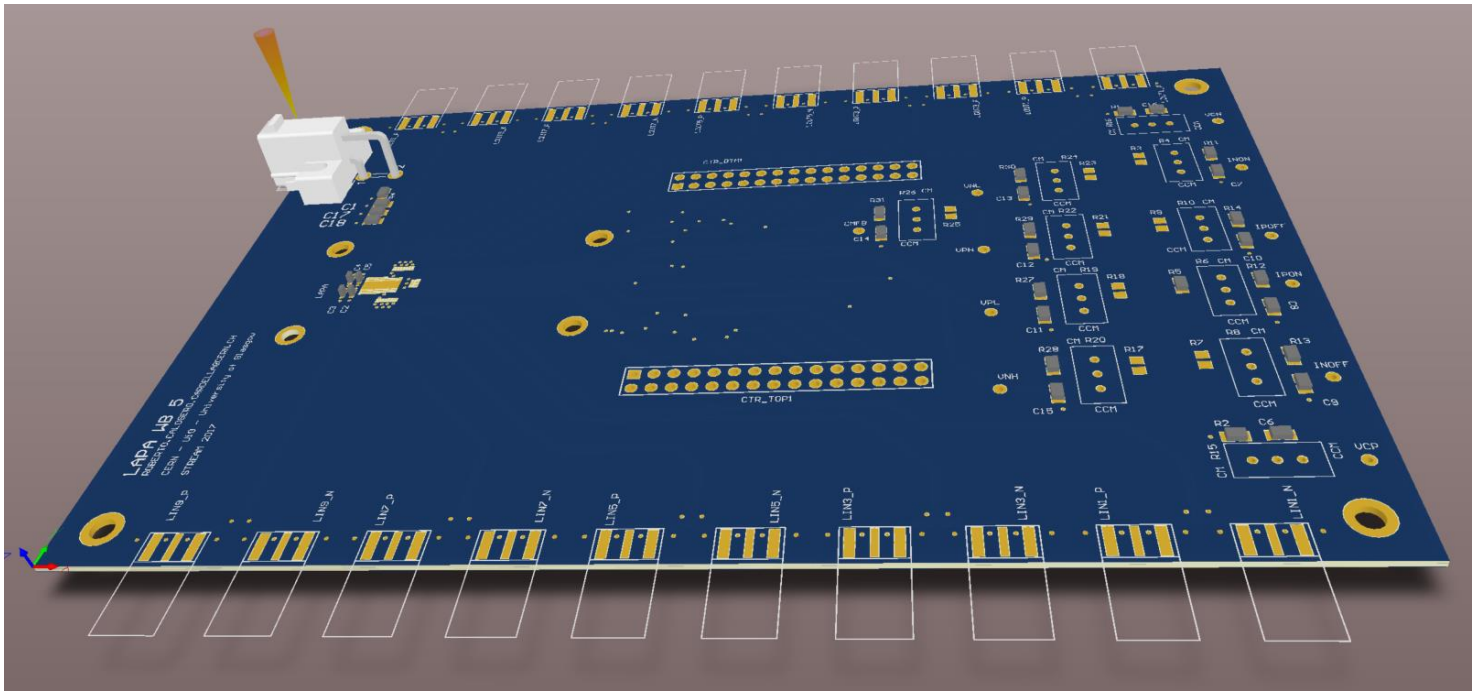
DD meeting March 2017



DD SECTION MEETING

LAPA TEST CHIP

- Designed in collaboration with Glasgow
- Under production from two suppliers
- Will be assembled and tested at CERN and in Glasgow
- Dummy Chip for wire bond test at the end of the year



R. Cardella, M. Dima, L. Flores Sanz De Acedo, L. Simon Argemi

Conclusions

TJ MALTA

Read Out
Getting ready

- Carrier board under design
- Dummy chips ready
  - Wirebond Test
  - Microchannel Test
  - First modules
- Readout firmware
- FLEX under design
- Flipchip interconnection being explored

TJ LAPA

Read Out
Getting ready

- Carrier board submitted
- Dummy chips ready
  - Wire bonding test

Plans for system tests, long chain

TJ Wafers in January – Stay tuned

Thank you for the attention