# TCT for the characterization of silicon interfaces obtained by CMOS compatible wafer bonding

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EP-DT-DD meeting 01 December 2017



- CMOS compatible wafer bonding for the fabrication of silicon detectors
- Electrical characterization of Si-Si bonded interfaces
- Proof of principle of electrical injection TCT



### Silicon pixel detectors

### Hybrid



### Monolithic



L. Rossi et al., Pixel Detectors: From Fundamentals to Applications, *Springer*, 2006. P. Riedler, Monolithic silicon pixel sensors and technology challenges of the ALICE ITS, 2015, https://indico.cern.ch/event/352490/attachments/1155083/1659960/DT\_training\_seminar15092015.pdf



# Bonding of monolithic detectors

- Motivation: possibility of choice of different bulks type
  - High resistivity silicon for sensing
  - Low resistivity silicon for CMOS circuit
- CMOS compatible wafer bonding for monolithic pixel detectors:
  - Thinning of CMOS wafers
  - Bonding with sensing bulk
    - Low temperature (<400°C)
    - Silicon bulk fracture strength reached
    - Oxide-free interface
- Conduction properties of the bonding interface to be characterized







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### Two investigation approaches



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#### TCT on Schottky diodes





### INVESTIGATOR for bonding interface characterization

Standard INVESTIGATOR from ALICE ITS:

- Different layouts tested
- Epitaxial layer (> 1 kΩ cm) on low resistivity silicon wafer
  Bonded INVESTIGATOR (fabricated by G-ray):
- Thinning of back side of ITS wafer
- Surface preparation

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 Bonding to different types of silicon wafers

Test list	
Bottom wafer	Thickness
High resistivity silicon bulk > 5 kΩ cm	700um
	90um
	55um
Epitaxial silicon Epi > 1 kΩ cm	Epi 20um, Bulk 700um

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- 1. Drift: charges in the depletion region are collected by the corresponding n-well
- 2. Diffusion: charges diffuse in silicon. If they reach a depletion they are collected.
  - Charges generated from one particle can be collected by different n-wells (charge sharing)
  - Diffusing charges are reflected by low resistivity silicon bulk



#### Measurements on bonded INVESTIGATOR chips – Fe55 Normalized Counts Cluster 700 um 90 um multiplicity 55 um Standard (number of pixels collecting charges per event) < 206 0.4 0.2 0 8 9 2 3 5 6 7 10 4 Absence of Cluster Size [# pixels] charge sharing Normalized Counts — Standard EPI There should 0.6 Charges pass be charge Charges are 0.4 through the sharing for absorbed by the interface and 0.2 interface epitaxial silicon diffuse in the bulk 2 3 5 7 8 9 10 substrates 4 6 Cluster Size [# pixels] 01 EP-DT CERN cea December J. Bronuzzi - EP-DT-DD meeting **Detector Technologies** ÉCOLE POLYTECHNIQUE ÉDÉRALE DE LAUSANNE

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8

### Measurements on bonded INVESTIGATOR chips – Sr90



- Weak charge sharing observed
- Consistent with the hypothesis of not conduction through bonding interface



### SEM analysis of bonded INVESTIGATOR

#### **INVESTIGATOR** cross section

Metal layers
Epitaxial silicon
High ρ silicon

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### Two investigation approaches



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#### TCT on Schottky diodes





### TCT for bonding interface characterization

Amorphous silicon at the bonding interface can be modeled as a layer with a trap density 1e16 cm<sup>-3</sup> Analytical modeling of TCT transient current for bonding interfaces, 2 cases:



J. Bronuzzi et al., "Principle and modelling of transient current technique for interface traps characterization in monolithic pixel detectors obtained by CMOS-compatible wafer bonding", JINST, 11 P08016, 2016.



### TCT for bonding interface characterization

#### **Traps not detected**

- Low voltage: depletion region does not reach traps layer
- Presence of both donors and acceptors in same quantity: ionized traps will result is neutral charge
- **Presence of acceptor**: ionized acceptors generate negative charge that do not give double peak electric field

#### **Traps detected**

- **High voltage**: depletion region reaches traps layer
- **Presence of donors**: ionized donors generate positive charge that gives double peak electric field

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### Test structures fabrication



CMOS compatible bonding of silicon wafers at CEA-LETI:

- Silicon wafers: 8 inches, magnetic Czochralski Ptype, ρ > 5000 ohm.cm
- Thinning (tolerance 1  $\mu m$ ), to have interface close to surface, and bonding (pressure 30 kN)
- Downsizing from 8 inches to 4 inches through laser cut (Sil'Tronix)
- Bonding parameters:
  - Top wafer thickness: 20 μm, 50 μm
  - Surface preparation: hydrophobic, hydrophilic
  - Annealing temperature: 400 °C, T amb
- Fabrication of Schottky diodes on top of wafers at the Center of Micronanotechnology (CMi) at EPFL, to be studied with TCT

CMi: <u>https://cmi.epfl.ch/</u>



Start wafers	
<i>Thinning top wafer</i>	
Bonding	
Downsizing	
Schottky diodes fabrication	

# Validation of TCT on Schottky diodes CMI EPFL Center of MicroNanoTechnology

- Tests performed on structures fabricated at CMi
- 4 inches wafers
- Resistivity > 2000 ohm.cm
- Float zone P-type
- Al for schottky contacts
- Pt for ohmic contacts

Next steps:

- Schottky diodes fabrication on bonded wafers
- TCT measurements on Schottky diodes on bonded wafers



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CMi: <u>https://cmi.epfl.ch/</u>



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### **Electrical injection TCT**

- Instead of Schottky diodes, integrate TCT charge injection in silicon
- PiN Diode doping profile modified
- Nanosecond voltage pulse applied on the N-type well







### Physical principle

Thermionic emission

 $J_i/J_1 = e^{\frac{\phi_{B_1} - \phi_{B_i}}{kT}}$ 



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### Light and electrical injection



### Fabrication and measurements setup



Device fabricated at CMi



- Aluminum
- High resistivity silicon



- Silicon dioxide
- Spacing between n and p-type doped silicon

### Setup components





### Proof of principle of el-TCT

### Measurements: comparison electrical and optical TCT

Comparison TCAD simulations and measurements





### Proof of principle of electrical TCT



- Charge calculated as the integral of the transient current in time
- Measured charge has a behavior similar to simulated charge
- Measured charge follow the same physical principle of simulated charge, thermionic emission



### **Conclusions and outlook**



Direct wafer bonding is being investigated for an "hybrid" approach to manufacture monolithic pixel detectors.

- A model for TCT across silicon bonded interfaces has been developed.
- INVESTIGATOR wafers have been thinned and bonded to different types of substrates to study the bonding interfaces.
- Shottky diodes will be fabricated on already bonded plain wafers to study the interfaces with TCT at the beginning of 2018.

A new type of charge injection has been studied for TCT.

- Principle of electrical injection TCT (el-TCT) has been proven.
- EI-TCT will be evaluated for online measurements of radiation induced damage in silicon samples in IRRAD next year.



# Thank you for the attention Questions?



### Fabrication of monolithic pixel detectors

### **Electronics driven**

- Low resistivity silicon
- High performance electronics
- Low performance sensing (small depletion region)

### **Sensor driven**

- High resistivity silicon
- Difficult electronics design
- High performance sensing (large depletion region)

L. Rossi et al., Pixel Detectors: From Fundamentals to Applications, Springer, 2006.

