Abstract:

Modern detector science and technology has originated from High Energy Physics experiment needs in the ‘80’s of the past century, based on the achievement and knowledge of the silicon industry of the time. The first segmented array of diodes (a microstrip sensor) was developed to track vertices at the NA11 experiment at the SPS accelerator at CERN (Geneva, CH). During the following years, detector technology developed into a special branch of the huge silicon technology enterprise that has been arguably the biggest contributor to the evolution of most of the economical, social and scientific activities of mankind. If, and how, detector technology for science has kept the pace with the spectacular speed of evolution of mainstream silicon technology (namely, the microelectronics industry) is the object of this lecture, that will also point out the special requirements of detectors for science and how these can be linked to modern microelectronics trends.
OUTLINE:

• The revolutionary impact of silicon detectors in HEP
• Detectors and microelectronics, a powerful synergy
• Evolution of silicon sensors and electronics: overcoming every challenge, to date
• Modern microelectronics trends: too fast forward for sensors?
Collider physics requirements

Required performance for general purpose particle physics detectors:

- full solid angle coverage
- accurate momentum and/or energy measurement
- identification of all particles
- no dead time
- Vertices identification
Technologies for HEP detectors

Three major families:

- Gaseous detectors: sensing ionisation in gas (mip charge $\sim 90$ e/ion pairs cm$^{-1}$)
- Solid state detectors (mip charge $\sim 40$ to 160 e/h pairs µm$^{-1}$)
- Scintillating detectors (scintillating light detected by photon detectors)
Silicon for HEP detectors

Silicon:
- Widely available
- For Minimum Ionising Particles: ~ 40 to 160 e/h pairs µm⁻¹
- Fast signal formation
- Small feature size (high granularity)

Wide band semiconductors: for operating at non-cryo temperatures.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap, $E_g$ (eV)</td>
<td>1.12</td>
<td>1.43</td>
<td>3.03</td>
<td>3.26</td>
<td>3.45</td>
<td>5.45</td>
</tr>
<tr>
<td>Dielectric constant, $\varepsilon_r$</td>
<td>11.9</td>
<td>13.1</td>
<td>9.66</td>
<td>10.1</td>
<td>9</td>
<td>5.5</td>
</tr>
<tr>
<td>Electric breakdown field, $E_c$</td>
<td>300</td>
<td>400</td>
<td>2,500</td>
<td>2,200</td>
<td>2,000</td>
<td>10,000</td>
</tr>
<tr>
<td>Electric breakdown field, $E_c$ (kV/cm)</td>
<td>300</td>
<td>400</td>
<td>2,500</td>
<td>2,200</td>
<td>2,000</td>
<td>10,000</td>
</tr>
<tr>
<td>Electron mobility, $\mu_e$ (cm²/V·s)</td>
<td>1,500</td>
<td>8,500</td>
<td>500</td>
<td>80</td>
<td>1,000</td>
<td>1,250</td>
</tr>
<tr>
<td>Hole mobility, $\mu_h$ (cm²/V·s)</td>
<td>600</td>
<td>400</td>
<td>101</td>
<td>115</td>
<td>850</td>
<td>850</td>
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<tr>
<td>Thermal conductivity, $\lambda$ (W/cm·K)</td>
<td>1.5</td>
<td>0.46</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
<td>22</td>
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<td>Saturated electron drift velocity, $v_{sat}$ ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
<td>2.7</td>
</tr>
</tbody>
</table>
Silicon detectors

Silicon:
Tipically 100-500 µm thick segmented arrays (µ-strips) or matrices (pixels) of silicon diodes are the sensitive part of a detector system.
Silicon detectors

A complete detector is made of:

- Diodes (reverse biased)
- Analogue amplifiers
- Digital readout
Vertex identification, key to collider physics.

Needs for track reconstruction (late ‘80’s): high resolution, low mass (minimise multiple Coulomb scattering).


Example:
Mean decay length $B_s$ ($\tau \approx 1.5$ ps):
in $B_s$-frame: $c\tau \approx 450 \ \mu m$
in lab frame $\beta\gamma c\tau = \text{few mm}!$

$D_s$ ($\tau \sim 0.5$ ps):
in $D_s$-frame: $c\tau \approx 150 \ \mu m$
in lab frame $\beta\gamma c\tau = \text{few mm}!$
(lower mass $\Rightarrow$ more relativistic)
The Spectacular success of Silicon detectors

ASIC’s for silicon detector readout: 1988 (UA2 at the CERN/SPS): first collider experiment with silicon detectors with ASIC read-out, namely the AMPLEX, 16 channel, 3 μm Feature Size (S) CMOS chip for read-out and signal multiplexing (E. Heijne, P. Jarron).
Silicon detector systems have many ingredients, but a crucial element is that the improvement of silicon detectors is linked to the evolution of CMOS technology.
The Spectacular success of Silicon detectors

A virtuous interaction between technology and experiment needs: technology improvements allow better physics performance and experiment requirements push on the technology. **BUT:** CMOS technology evolution is driven by motivations outside physics.
Microelectronics: the Moore’s law

Mosfet Scaling in microelectronics enabled, together with R&D in the sensor (diode), the accelerated improvement of detectors for Physics.
Moore’s law in electronics for pixel sensors

<table>
<thead>
<tr>
<th>Name</th>
<th>D-OMEGA ION</th>
<th>LHC1</th>
<th>FE-I3</th>
<th>FE-I4</th>
<th>RD53A</th>
<th>RD53(B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>3 µm</td>
<td>1 µm</td>
<td>0.25 µm</td>
<td>0.13 µm</td>
<td>65 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Node</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chip size</td>
<td>8.3x6.6 mm²</td>
<td>8x6.35 mm²</td>
<td>10.8x7.6 mm²</td>
<td>10.2x19 mm²</td>
<td>20x10 mm²</td>
<td>20x20 mm²</td>
</tr>
<tr>
<td>Pixel size</td>
<td>75x500 µm²</td>
<td>50x500 µm²</td>
<td>50x400 µm²</td>
<td>50x250 µm²</td>
<td>50x50 µm²</td>
<td>50x50 µm²</td>
</tr>
<tr>
<td>Pixel array</td>
<td>16x63</td>
<td>16x127</td>
<td>18x160</td>
<td>80x336</td>
<td>400x198</td>
<td>400x396</td>
</tr>
<tr>
<td>Transistor count</td>
<td>???</td>
<td>800k</td>
<td>3.5M</td>
<td>80M</td>
<td>311M</td>
<td>600M</td>
</tr>
</tbody>
</table>


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Silicon detectors and Readout Electronics arrangements

Sensitive diode, Analogue circuit and Digital circuits are the ever present elements.

The hybrid solution

Amplified diode and Analogue/Digital readout

Monolithic solution

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Amplified diode solution

Monolithic solution
Silicon detectors and Readout Electronics arrangements

Sensitive diode, Analogue circuit and Digital circuits are the ever present elements.

The hybrid solution

Amplified diode solution

Monolithic solution

Most used
The diode signal and the electronics

Signal and electronics chain:
Examples and typical sizes of the different architectures

- **40 – 110 µm pitch, 1 – 4 cm long strips. Readout: Beetle chip, 0.25 µm CMOS.**

- **Pixel sensor (200 µm thick) and FE-I4 (400 µm thick) readout hybrid (bump-bonded) assembly. 130 nm CMOS, 20x18.8 mm², 26880 pixel, size 50x250 µm²).**

- **Monolithic solution

Monolithic solution

MAP sensor 50 µm thick, 80 x 80 µm². R&D for mu3e, 180 nm CMOS.**
### Manufacturing of sensors and electronics

Who makes sensors and who makes electronics

<table>
<thead>
<tr>
<th>Custom diode arrays foundries</th>
<th>Commercial large scale CMOS manufacturers</th>
</tr>
</thead>
<tbody>
<tr>
<td>HPK, CIS, CNM, CSEM, FBK, Micron, MPI, SINTEF, VTT, .....</td>
<td>IMEC, IBM, TSMC, AMS, TJ, LF, GF, .....</td>
</tr>
</tbody>
</table>
What Defines an Efficient detector?

An efficient detector (diode + readout electronics chain) allows for clear separation of the signal from minimum ionizing particles (mip’s) from the noise fluctuations. This is described by the quantity: S/N (signal over noise ratio).
What Defines an Efficient detector?
The signal over noise ratio (S/N)

Signal parameters:

The expected signal charge is a function of the detector

Depleted thickness:

Typical thickness: 100-500 µm

Most probable signal ~ 7600-38000
Noise of the detector/electronics chain:

\[ C_d = \text{detector capacitance} \]
\[ I_b = \text{bias current} \]
\[ R_p = \text{bias resistor} \]
\[ R_s = \text{strip resistance} \]
\[ V_{na}^2 = \text{Preamplifier noise} \]

\[ \text{Noise} = \sqrt{\sum (ENC_i)^2} \]

\[ ENC_{I_b}^{parallel} \approx 108 \cdot \sqrt{I_b(\mu A) \tau (ns)} e^- \]
\[ ENC_{R_p}^{parallel} \approx 24 \cdot \sqrt{\tau (ns)/R_p(\Omega) e^-} \]
\[ ENC_{R_s}^{series} \approx 24 \cdot C_{tot} (\text{pF}) \cdot \sqrt{R_s(\Omega)/\tau (ns)} e^- \]

+ front end electronics: \( ENC_{fe} = a + bC_d \)
What can silicon detector do?

Measure position:

Measure energy/momentum:

Measure time:

For \( N \) equidistant measurements:

\[ \sigma(P) = \frac{\sigma(x)P}{0.3BL^2 \sqrt{N + 4}} \]

(R.L. Gluckstern, NIM 24 (1963) 381)
Silicon detectors and ever more difficult challenges from experiment’s requirements

- Interaction rates
- Position resolution
- Reduced mass
- Reduced power
- Timing capabilities
- Radiation tolerance

ATLAS 120 pile-up collisions
**Interaction rate challenge**

**Example: the ALICE (A Large Ion Collider Experiment at CERN)**

Very High Multiplicity every bunch crossing (25 ns).
Drives requirements to small individual channel area, fast repetition rates. Specifications for the sensors:

<table>
<thead>
<tr>
<th></th>
<th>Inner</th>
<th>Outer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor thickness (μm)</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Spatial resolution (μm)</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Dimensions (mm$^2$)</td>
<td>15 × 30</td>
<td>15 × 30</td>
</tr>
<tr>
<td>Power density (mW cm$^{-2}$)</td>
<td>300</td>
<td>100</td>
</tr>
<tr>
<td>Time resolution (μs)</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Detection efficiency (%)</td>
<td>99</td>
<td>99</td>
</tr>
<tr>
<td>Fake hit rate</td>
<td>10$^{-5}$</td>
<td>10$^{-5}$</td>
</tr>
<tr>
<td>TID radiation hardness (krad)</td>
<td>2700</td>
<td>100</td>
</tr>
<tr>
<td>NIEL radiation hardness</td>
<td>1.7×10$^{13}$</td>
<td>10$^{12}$</td>
</tr>
</tbody>
</table>
Interaction rate challenge

**ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade NIM A, Volume 824**, 11 July 2016, Pages 434-438

Author links open overlay panel [M. Mager](#)

On behalf of the ALICE Collaboration

ALPIDE $1.5 \times 3 \text{ cm}^2$ Monolithic Active Pixel with $512 \times 1024$ (row×column) $28 \times 28 \mu \text{m}^2$ pixels that are read out in a binary hit/no-hit fashion. It combines a continuously active, low-power, in-pixel discriminating front-end with a fully asynchronous, hit-driven combinatorial circuit.
Interaction rate challenge

Need to move away from optimal shaping time choices
Position resolution challenge

Small pixel size also results in better spatial resolution: With binary readout the resolution is Pitch/sqrt(12). Interest in going towards very small pixels.

\[ \sigma_x = \frac{\text{pitch}}{\sqrt{12}} \]
Position resolution challenge

Position reconstruction with good analogue output

If a particle passes between two strips the deposited charge flows to the nearest strip. Due to transverse diffusion (~10 $\mu$m) and track angle the charge can be shared between readout electrodes.

$$\eta = \frac{Q_R}{Q_R + Q_L}$$

Ideally: linear relation $\eta$ and $x$

$$x = x_L + \eta(x_R - x_L)$$

Need good S/N (detector thickness), heavy on data readout.
Reduced mass challenge

Monolithic

One of the main feature of MAPS

Can be very thin (~25 µm of silicon in total) and still fully efficient!
A charged particle undergoes many “small–angle” scatters. Mostly Coulomb interactions and some strong interactions (for hadrons).

The width of the cumulated angular deflection in the $xy$-plane is:

$$\theta_{\text{rms}} = \theta_0 = \frac{13.6 \text{MeV}}{p \beta c} \sqrt{\frac{L}{X_0}} \left[ 1 + 0.038 \ln \left( \frac{L}{X_0} \right) \right]$$

$$s_{\text{rms}} = \frac{L \theta_0}{4 \sqrt{3}}$$

$$s_{\text{rms}} = \frac{\Delta p_{MS}}{p} \approx 0.05 \frac{1}{B \sqrt{LX_0}} \quad \text{(independent of } p\text{!)}$$

$$\frac{\sigma(P_\perp)}{P_\perp} = C_{\text{meas}} P_\perp \oplus C_{\text{MS}}$$

Multiple scattering scales with the amount of material traversed. (beam-pipe, detectors, magnet,..)

Thus for precise measurement momentum, should also have as little material as possible in the tracking detectors. (also important for precise energy measurement in the calorimeters.)
Reduced power challenge

Electronics outside the collection well:
- very small capacitance so low noise, low power
- collection by drift and diffusion

Electronics inside the collection well:
- higher capacitance so higher noise, power and cross-talk
- faster collection by drift

Besides: small feature size electronics, with lower Vdrive, has lower power consumption per operation
Timing challenge (4d Tracking)

Great position resolution (10 μm) combined with < 50 ps time resolution.

Noise and signal are key in term of timing performance.

\[ \sigma^2_T = \sigma^2_{TW} + \sigma^2_j + \sigma^2_{TDC} \]
\[ \sigma^2_{TW} \propto V_{TH}/S \]
\[ \sigma^2_j \propto (S/N)^{-1} \]
\[ \sigma^2_{TDC} \]

Not considered
Radiation tolerance challenge

Radiation Background Simulation: LHC and HL-LHC

At inner pixel radii - target survival to $2\cdot3\times10^{16}$ $n_{eq}$/cm$^2$
Future Circular Collider

Work supported by the European Commission under the HORIZON 2020 projects EuroCirCol, grant agreement 654305; EASITrain, grant agreement no. 764879; ARIES, grant agreement 730871; and E-JADE, contract no. 645479.
## Hadron Collider Parameters

<table>
<thead>
<tr>
<th></th>
<th>LHC / HL-LHC</th>
<th>HE-LHC (tentative)</th>
<th>FCC-hh</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Initial</td>
<td>Ultimate</td>
<td></td>
</tr>
<tr>
<td>Cms energy [TeV]</td>
<td>14</td>
<td>27</td>
<td>100</td>
</tr>
<tr>
<td>Luminosity ([10^{34} \text{cm}^{-2}\text{s}^{-1}])</td>
<td>1 / 5</td>
<td>28</td>
<td>5</td>
</tr>
<tr>
<td>Machine circumference</td>
<td>27</td>
<td>27</td>
<td>97.75</td>
</tr>
<tr>
<td>Arc dipole field [T]</td>
<td>8</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Bunch charge</td>
<td>1.15 / 2.2</td>
<td>2.2</td>
<td>1</td>
</tr>
<tr>
<td>Bunch distance [ns]</td>
<td>25</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Background events/bx</td>
<td>27 / 135</td>
<td>800</td>
<td>170</td>
</tr>
<tr>
<td>Bunch length [cm]</td>
<td>7.5</td>
<td>7.5</td>
<td>8</td>
</tr>
</tbody>
</table>

Target survival \(1 \times 10^{17} n_{\text{eq}}/\text{cm}^2/\text{Y}\)
Radiation with protons/neutrons

**Surface damage:** ion trapping in SiO$_2$, leading to charge on Si-SiO$_2$ interface. Sensor design must be robust against this (not discussed here).

**Bulk damage:** displacement of Si atoms within the crystal leaves vacancies and interstitials (defects).

- Energy needed to displace atom from lattice = 15eV
- Damage energy dependent
  - $< 2$ keV $\Rightarrow$ isolated point defect
  - 2-12 keV $\Rightarrow$ defect cluster
  - $>12$ keV $\Rightarrow$ many defect clusters
- This damage is called: **Non-Ionizing Energy Loss (NIEL)**
  - Results scaled to 1MeV neutrons
    - (e.g. ATLAS ID up to $\approx 2 \times 10^{14}$ n$_{eq}$cm$^{-2}$yr$^{-1}$)
- Electrons and photons don’t make defects!

Orthogonal to most of the above solutions to the other challenges
Surface damage

• This effect is due to the presence in the SiO$_2$ and SiO$_2$-Si interface of positive charges
  1. Fixed charges $\rightarrow$ from production process
  2. Mobile positive impurity ions $\rightarrow$ same as 1.
  3. Trapped holes $\rightarrow$ from irradiation

• The trapped holes (less mobile than electrons) are generated by ionization
  - Heavy charged particles $\rightarrow$ high ionization density $\rightarrow$ high recombination
  - Electrons/photons $\rightarrow$ low ionization density $\rightarrow$ low recombination $\rightarrow$ dominates

• This charged layer changes the electric properties of the segmented side of the detector
  - Increases the interstrip capacitance ($C_{\text{int}}$)
  - Increases the surface current
  - Reduce the breakdown voltage

• Depends on the crystal orientation
• Important for Linear Collider and Xfel experiments
The damaged lattice ‘zoo’

These can:
- donate electron/holes
- capture electron/holes (trapping)
- increase leakage current (two-step transitions valence to conduction band)
- act as recombination centres

Damaging effects on Silicon detectors:
- increased leakage currents
- type-inversion (change of effective doping type)
- reduced charge collection efficiency and charge carrier mobility
Increase of the $V_{FD}$

Reduction of the charge collection efficiency

$$Q_{e,h}(t) = Q_{0e,h} \exp\left(-\frac{1}{\tau_{eff\,e,h}} \cdot t\right)$$

$$\frac{1}{\tau_{eff\,e,h}} = \beta_{e,h}(T, t) \Phi_{eq}$$

Increase of the reverse current
More relevant method: analogue readout with LHC speed electronics

Mip signal from $^{90}\text{Sr}$ source

Analogue information from the Alibava board (equipped with Beetle chip)
Results with proton irradiated 300 μm n-in-p Micron sensors (up to $1 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$)

Irradiated with reactor neutrons

RED: irradiated with 24GeV/c protons
Other: 26MeV protons

Look at the voltage scale!!
The onset of Charge Multiplication breaks a few rules, like the proportionality of the signal with thickness.....

Charge degradation vs fluence for silicon sensors with different thicknesses
Different detector structure: 3D Detectors

- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30µm:300µm)
- Benefits
  - $V_{\text{depletion}}$ (Electrode spacing)$^2$
  - Collection time $\propto$ Electrode spacing
  - Reduced charge sharing $\propto$
- More complicated fabrication - micromachining

**Planar**

**3D**

Proposed by S. Parker and C. Kenney of the University of Hawaii in 1995.

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3d Sensor radiation hardness

- 3D pixel detectors bump bonded to ATLAS FE-I4 show > 98% efficiency after $3 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$.
- Modern electronics with small feature size show very good radiation tolerance by technology.
- This is also been shown with dedicated irradiation runs with 65 nm circuits (not yet on full assemblies).
Mitigation of sensor degradation

One essentially needs:

- Very high Electric field (voltage)
- Low noise

At intermediate radiation damage one can play other tricks:

Choice of bulk resistivity
Choice of bulk type (impurity content)
Applying High Voltage to D-CMOS
Applying High Voltage to D-CMOS: Top biasing

Figure 5.8: Absolute electric field strength of H35DEMO for resistivities 20 (a), 80 (b), 200 (c) and 1000 Ωcm (d), biased from the top at −120 V for the standard layout.
Applying High Voltage to D-CMOS: Backside biasing

From Lingxin Meng PhD thesis.

It is possible, with careful design, to apply HV to D-CMOS devices

**Figure 5.10:** Absolute electric field strength of H35DEMO for resistivities 20 (a), 80 (b), 200 (c) and 1000 $\Omega$cm (d), biased from the back at $-120$ V for the standard layout with back side process.

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A few results with D-CMOS

Other relevant metrics!

Non irradiated sensor for mu3e.

Figure 10 Layout of a) the MuPix7 chip and its measured performance b) hit detection efficiency and c) time stamping resolution (from [12]).
Radiation hardening of D-CMOS

M. Benoit et al., Characterization Results of a HVCMOS Sensor for ATLAS, NIMA

Max irradiation $5 \times 10^{15} \text{n}_{eq} \text{ cm}^{-2}$.

Figure 11 The measurement results of CCPDv4 devices a) track detection efficiency for different neutron dose, threshold and bias b) time stamping resolution (from [14])

M. Benoit et al., Test beam measurement of ams H35 HV-CMOS capacitively coupled, JINST 13 (2018) no.12, P12009
A look at the electronics

• Is electronics still evolving at Moore’s law speed?
• Can we just take the most advanced development of micro-electronics and used it in detector technology?
Short channel effects limit scaling of CMOS!

Past predictions (2001)

In 2001:
CMOS extendible down to $14 \text{ nm}$ for High-Performance logic
and $35 \text{ nm}$ for low power applications

Characteristics of a transistor:
• ON/OFF sharp characteristics
• Off current $\approx 0 \text{ A}$
• High On current ($1\text{mA}/\mu\text{m}$)
• Small $V_{\text{drive}}$ (for power, $P = C*V_{\text{drive}}^2$)

From A. Marchioro Seminar, May 2019
Short channel effects:
Velocity saturation
Drain Induce Barrier Lowering (DIBL)
Gate oxide leakage current
CMOS industry

Short channel effects:
Velocity saturation

- Beyond a certain value of the electric field, electrons (and holes) are not further accelerated by an increase in the $V_{DS}$ voltage

From A. Marchioro Seminar, May 2019
Short channel effects: Velocity saturation

Figure 2. Effective hole mobility versus effective field measured from p-MOSFETs on dual-channel heterostructure on SGOI substrate ($\chi = 0.3$, $\gamma = 0.6$), dual-channel on bulk-SiGe virtual substrate ($\chi = 0.3$, $\gamma = 0.6$) and that on the CZ-Si control. The mobilities were derived from drain currents at a small drain bias of $-25$ mV. Subthreshold characteristics are shown in the inset.
Drain Induce Barrier Lowering (DIBL)

Intel’s Revolutionary
22 nm Transistor Technology

Mark Bohr
Intel Senior Fellow

Kalazad Mistry
22 nm Program Manager

May, 2011

Gate engineering: Transistor operations

Transistor Current-Voltage characteristics

Intel’s Revolutionary
22 nm Transistor Technology

Mark Bohr
Intel Senior Fellow

Kaizar Misty
22 nm Program Manager

May, 2011
Gate engineering: Transistor operations

Transistor Gate delay

![Graph showing the relationship between operating voltage (V) and transistor gate delay for different technologies.](image-url)

- **32 nm Planar**
- **22 nm Planar**
- **37% Faster**
- **18% Faster**

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Gate oxide leakage current

Gate oxide:
Thickness down to 2 nm (65 nm) and going lower!!

High K material bring great improvement
CMOS and detectors today

State-of-the-art

RD53 65 nm CMOS pixel readout chip for extreme data rates and radiation levels (V. Re et al., CERN/RD53 collaboration)

Advanced readout chip for the pixel layers of ATLAS and CMS Upgrades at CERN

Expected position resolution > 15 µm.
Thanks to small (65 nm) feature size, 600M transistors in total, most in the digital section. The analogue area needs much larger transistors!!

The pixel size cannot scale down with the technology feature size.
Moore’s law is broken in sensor evolution.

- Reduction of the transistor channel length (feature size, S) over the years.

- Feature size exploited for mixed signal pixel devices for particle detection.

For mixed signal devices, there is little gain from going beyond the 65 nm process, signalling a stop in the evolution of mixed signal ASICs.
Moore’s law is broken in sensor evolution.

- Reduction of the transistor channel length (feature size, S) over the years.

- Feature size exploited for mixed signal pixel devices for particle detection.

A point of attention: the overcoming of small channel effects to carry on Moore’s law **DOES NOT HOLD** for analogue performance!

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Sensor trends: CMOS and sensors tomorrow?

- The hybrid solution
- Amplified diode solution
- Monolithic solution

Most used
Sensor trends

The hybrid solution

Amplified diode solution

Monolithic solution

Most used

... and the winner is ......
Sensor trends

The hybrid solution

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... is it? .......
How does see it industry?

Sony's Stacked CMOS Image Sensor Solves All Existing Problems in One Stroke

In conventional CMOS image sensors, the pixels (sensors) and circuits (logic) are formed on the same silicon substrate. Like oil and water, this coexistence of two conflicting elements makes it difficult to optimize their characteristics and also imposes other constraints.

The "stacked CMOS image sensor*1", a new generation of the back-illuminated CMOS image sensor, developed by Sony solves these problems in one stroke. Stacking the pixel section and the circuit section enables compact size, high image quality, faster speeds and flexible integration of versatile functions. Through this technology, Sony has created functions that will enable differentiation of final products to provide new ways of enjoying images.

*1: See press release at: http://www.sony.net/SonyInfo/News/Press/201201/12-009E/

http://www.sony.net/Products/SC-HP/cx_news/vol68/pdf/sideview_vol68.pdf#page=1
Sensor trends: CMOS and sensors tomorrow?

- The hybrid solution
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Most used

This is the most powerful solution technically available (given a number of conditions).
Silicon tracker detectors have been developed to serve the needs of Particle Physics collider experiments and had an accelerated evolution over the years. A key component of this success has been the spectacular improvements of CMOS. The detector systems have overcome all the extreme challenges posed by HEP experiments over the years, from very high multiplicities, high interaction rates, extreme radiation tolerance, high position resolution demand, .... Several new concepts have been introduced in the technology, like n-side readout and 3D geometries for radiation tolerance, low mass sensors, monolithic sensors, 4D devices, .... HEP sensors have also found their ways in many other scientific endeavours or technology applications.

The technology and the synergy between the sensor part (diode) and the electronics has seen a departure from the parallel evolution. This is mainly due to the lack of analogue performance quality in the most extreme (< 65 nm) CMOS technologies. So, if the last few years trend was to move the technology more towards monolithic devices, the current best guess for enhanced performance in the next few years is to separate the analogue tier from the digital one, in order to use different CMOS nodes (very small in the digital node for increase readout and computational local capabilities and larger nodes like 130/65 nm for analogue electronics). Interconnectivity (bump bonding will not be envisaged at these scales) is an issue, already solved in industry. But, in the future, new ideas could surface to change again the detector field. And, meanwhile, HEP is preparing experiment ideas that are pushing again the detector science to extreme territories (radiation, low mass, speed).