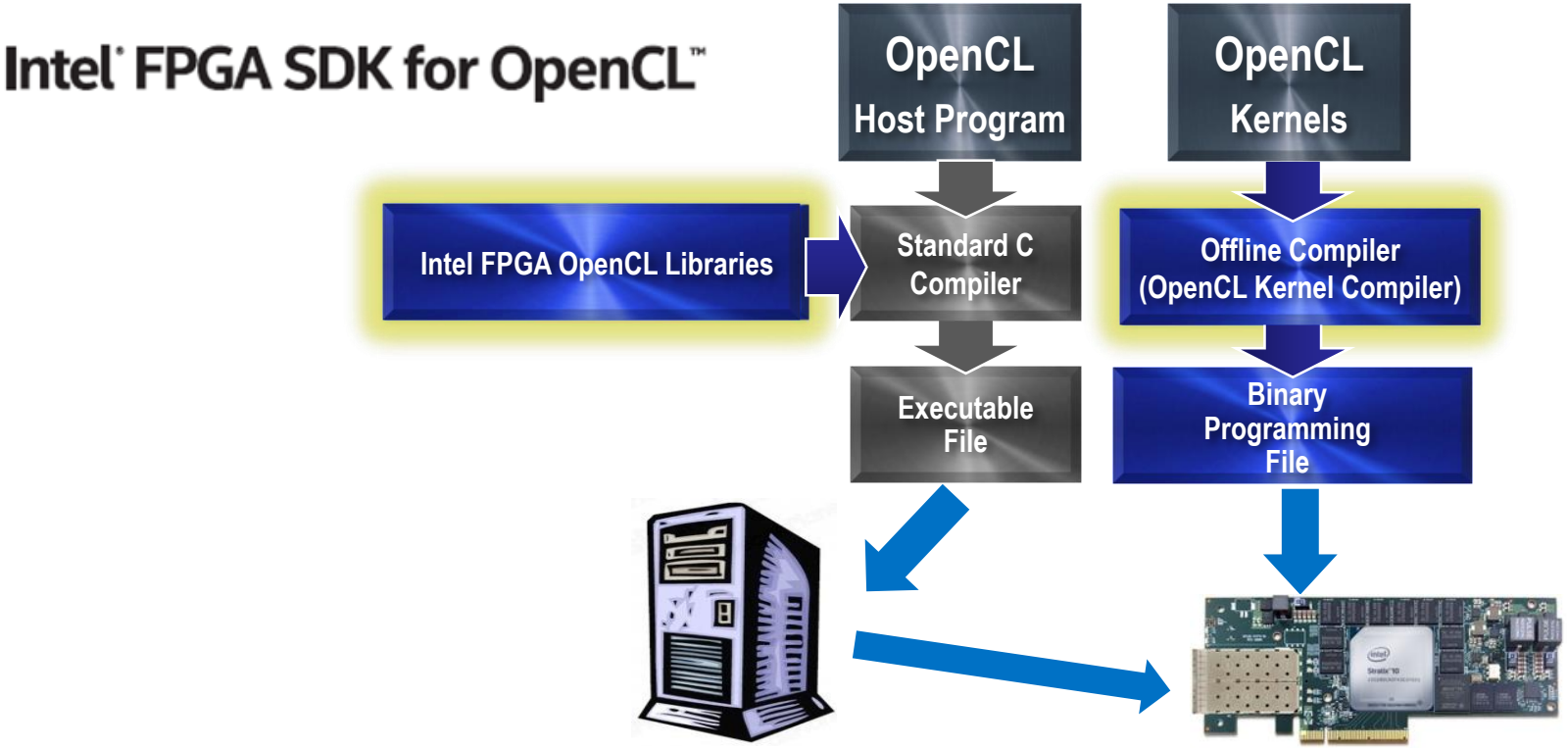
INTEL® FPGA SDK FOR OPENCL™

May 2019

Intel® FPGA SDK for OpenCL™ Usage



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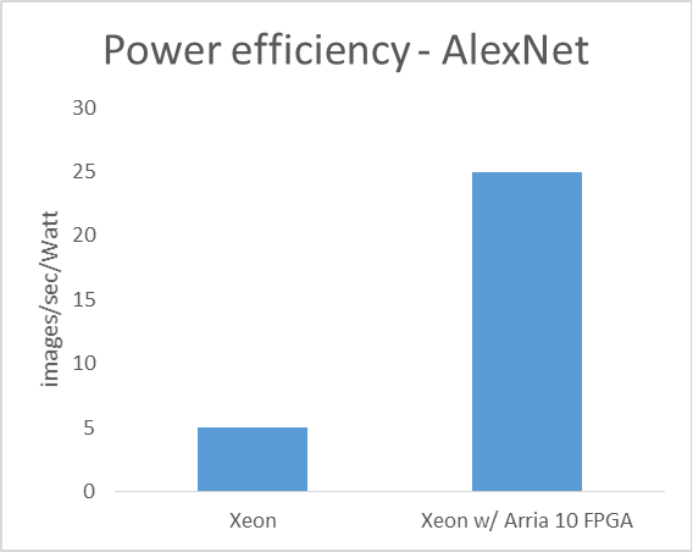
Intel® FPGA Performance / Watt Advantage

Performance per Watt Leadership

- Up to 10 TFLOPs performance
- Dedicated IEEE 754 hard floating point
- Arbitrary precision arithmetic

Power Efficiency

- 80% power reduction for DNNs like Alexnet



Exceptional Power Efficiency

High Throughput
Low Latency

The FPGA Data Movement Advantage

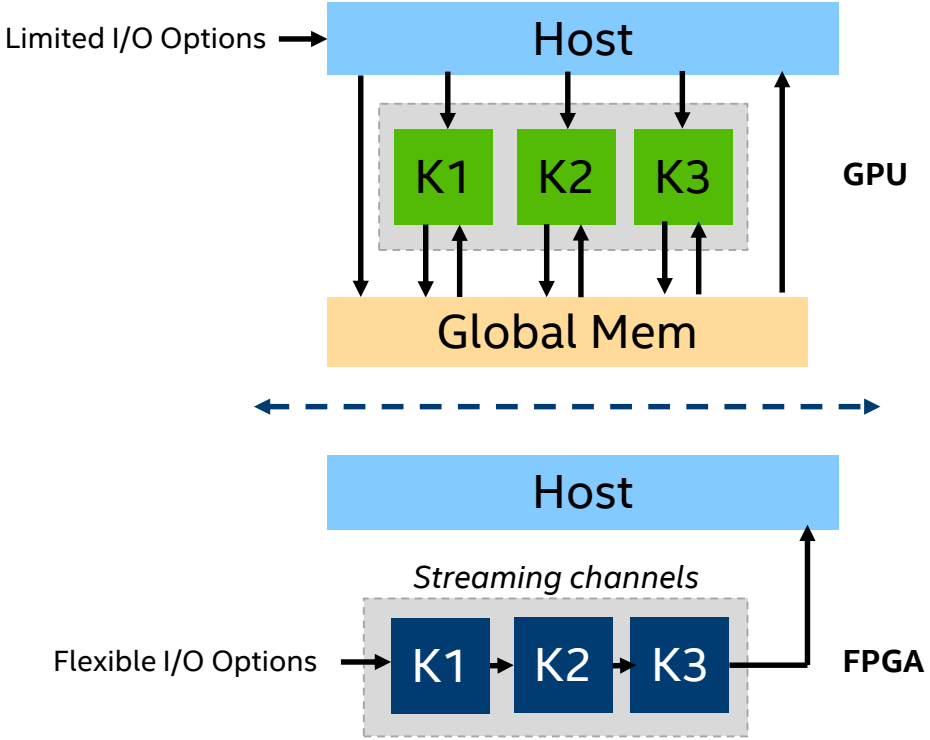
OpenCL common assumptions

- Host initiates all data transfers
- Data level parallelism exists

FPGA accelerators Offload Host CPU

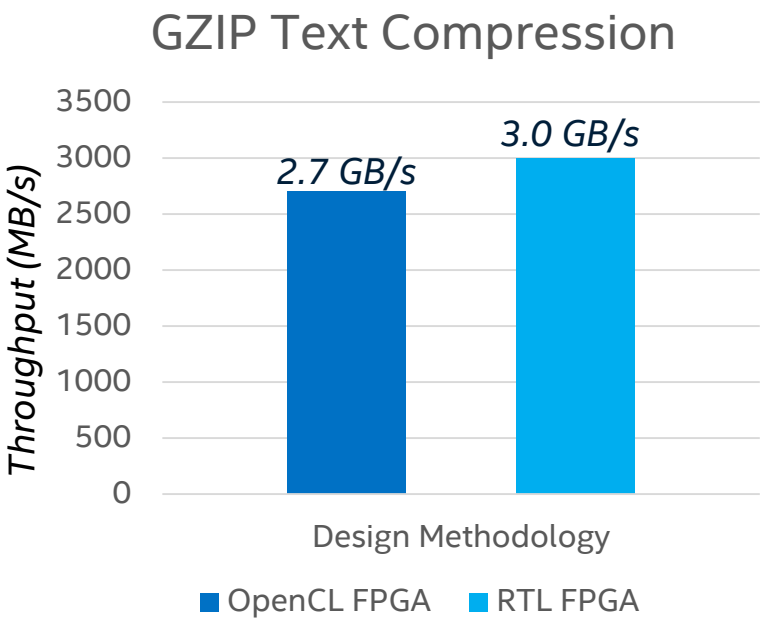
- Direct connection to I/O
- Host independent Kernel to Kernel communication

User defined I/O flexibility



OpenCL vs RTL Example: GZIP (Text) Compression

Metric	OpenCL	RTL
Experience	Summer Intern	FPGA Eng
Design Time	1 Month	3 Months
Throughput	2.7 GB/s	3.0 GB/s
Area	12% larger	



OpenCL required much lower design effort and time

Intel FPGA OpenCL SDK Supported Platforms

Intel and Arrow Supported Platforms

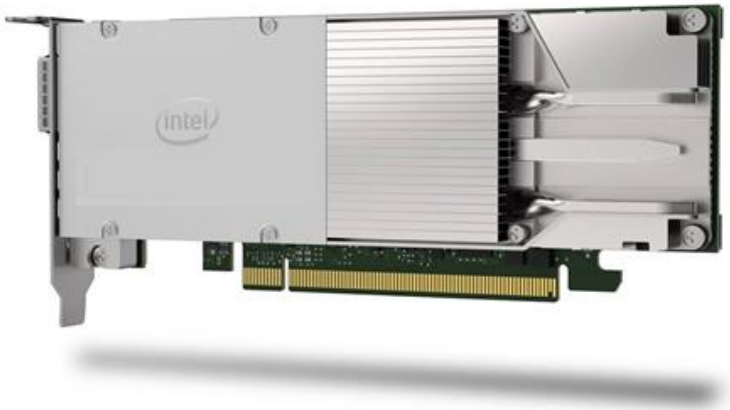
Company	Platform	FPGA
Intel	Programmable Accelerator Card(PAC)	Arria 10
Intel	Arria V SoC Development Kit	Arria V SoC
Intel	Arria 10 SoC Development Kit	Arria 10 SoC
Intel	Arria 10 GX Development Kit	Arria 10

Intel FPGA OpenCL SDK Preferred Platform Partners

PROGRAMMABLE ACCELERATOR CARD OVERVIEW

Rush Creek(PAC) – FPGA PCIe Acceleration Card with Arria® 10 GX FPGA

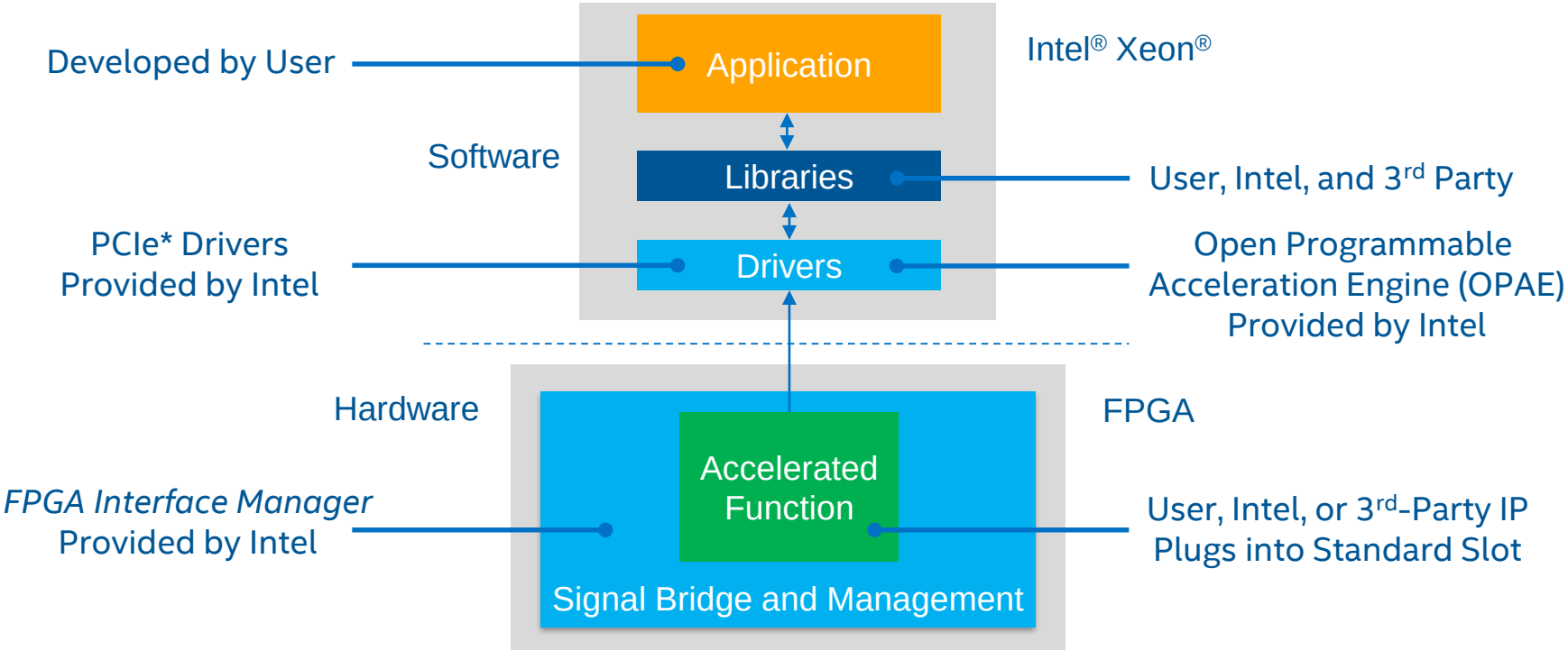
Intel's 1st versatile FPGA accelerator card that offers inline & look-aside acceleration for a versatile set of workloads



More info @ www.altera.com/PAC

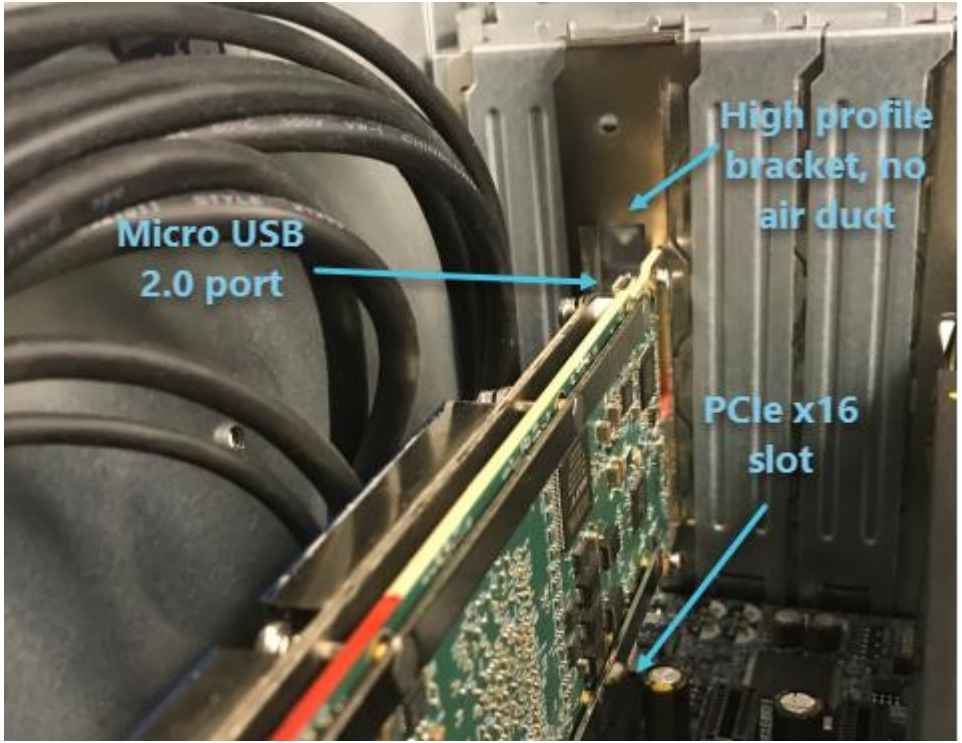
1st programmable solution to offer the Acceleration Stack for Intel® Xeon® CPU with FPGAs enabling broader FPGA adoption in data center

Intel® Xeon® + FPGA **Framework**



Simplifies the use of FPGAs

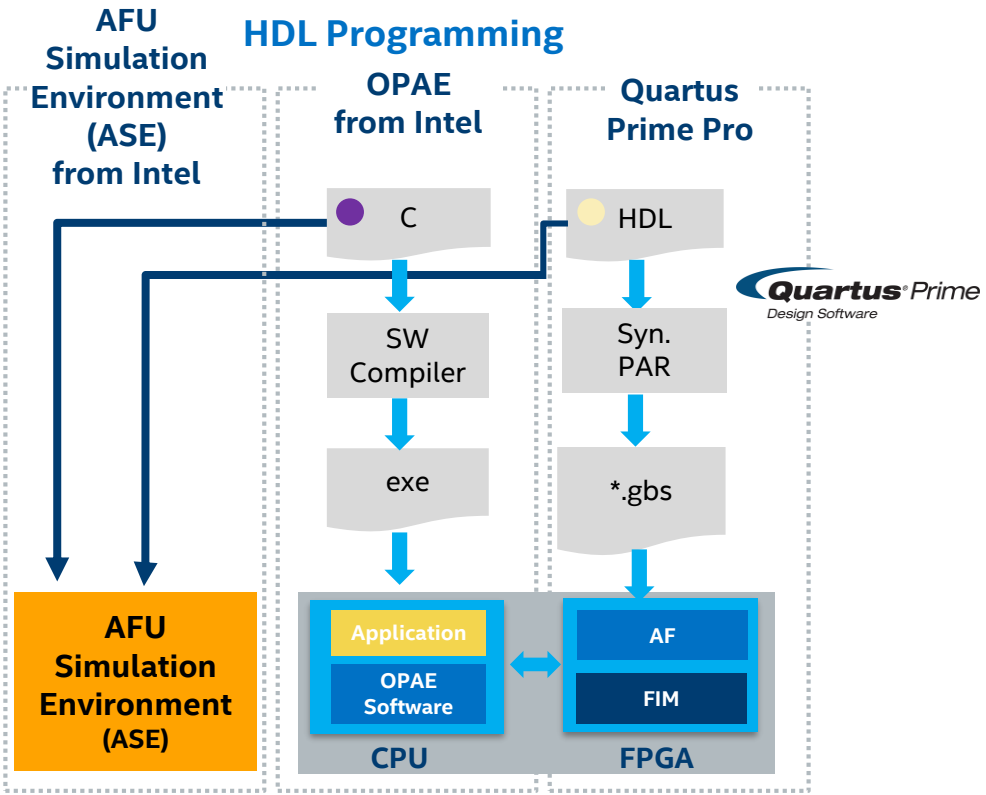
Installed Board



To access BMC, or using Quartus to program device, USB cable need to be plugged in (no cable in picture)

Standard profile bracket is shown

HW/SW Co-Design Approach using HDL



HW/SW Co-Design Approach using OpenCL

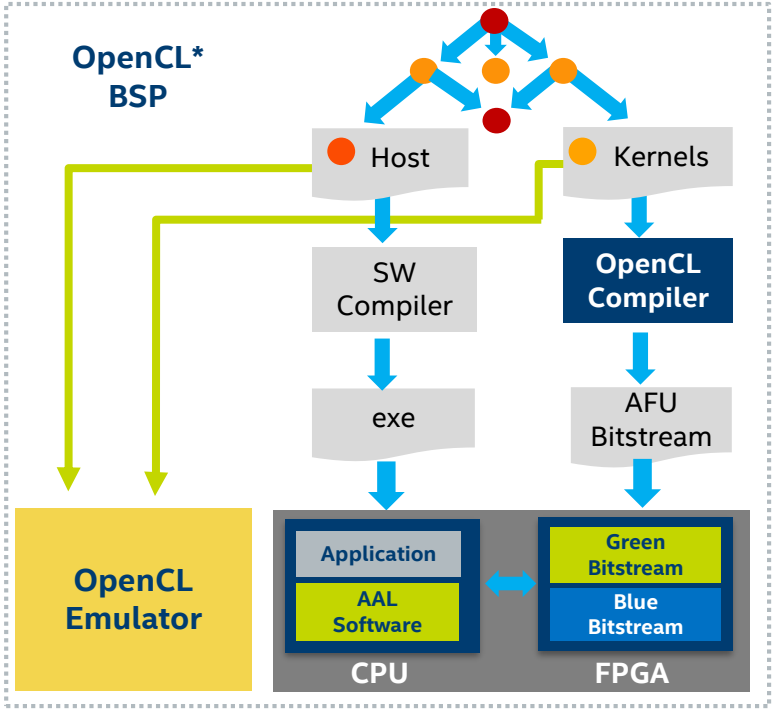
Common Development Environment

- OpenCL for both CPU Host and FPGA Accelerator
- Software centric design flow
- Consistent host management of FPGA

Intel provides heterogeneous processing

- CPUs, GPUs, FPGAs

OpenCL Programming



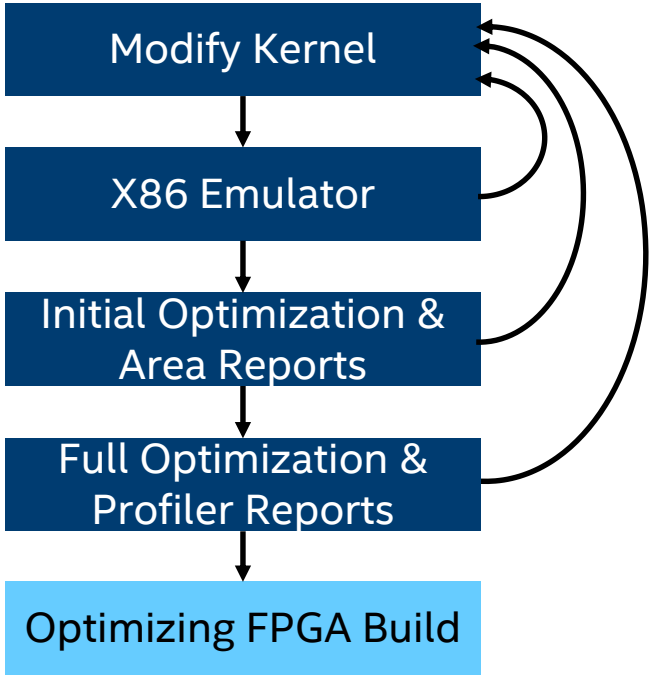
Intel FPGA SDK for OpenCL

Enables OpenCL for Intel FPGAs

- Easy implementation of applications into FPGAs
- Abstracts away complexities of FPGA design

Progressive Design Flow

- Emulation insures functional correctness
- Area and Performance reports drive efficiency



DATA CENTER/CLOUD

ADAS

OPENCL LAB OVERVIEW

Workstation Requirements

- HW
  - Support PCIe x16, min 48GB RAM, diskspace to fit OS+Quartus+work
  - BIOS support Intel Virtualization features VT-d, VT-x
- OS – RHEL7.4 / CentOS7.4
  - List of required packages/install profiles in Quick Start Guide
  - “sudo” administrator access required
- A10 PAC and DCP is supported with Quartus Prime Pro 17.0
- Machine used for test at EU RAE – HP Z620

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Cloud Acceleration Platform Access Manual

The Lab Exercises

- Exercise 1 :
  - In this exercise, you will practice writing an OpenCL™ host-side application including constructs to get the OpenCL platform and device; create an OpenCL context, command queue, and buffers. We will use the C++ OpenCL API in this lab.
- Exercise 2:
  - In this exercise, you will write an OpenCL™ kernel and launch it from the host-code
- Exercise 3 :
  - In this exercise, we will convert kernel that you created in exercise 2 into an NDRange kernel.

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