



5th

*Summer School on Intelligent signal processing
for FrontIER Research and Industry*

*Computing Labs CL2 / CL3
Fundamentals of Parallel Programming
using Intel® MIC Architecture*

Intel Modern Code Community

- UNESP Center for Scientific Computing (CSC)
 - Intel Modern Code Partner for Latin America
 - <https://software.intel.com/en-us/modern-code/live-workshops>

Latin America



Núcleo de Computação Científica - UNESP

The São Paulo State University - UNESP (Univ. Estadual Paulista), part of the state of São Paulo public higher education system, is one of the largest universities in Brazil, and its Center for Scientific Computing (CSC) operates two large Linux-based HPC clusters to support the university research

community. As high-performance computing moves toward the exascale era, many current scientific applications are unable to exploit modern, manycore computing environments. To tackle this challenge, UNESP CSC and Intel established a new partnership focused on code modernization and dissemination of improvements and innovations in parallel processing.

CL2 / CL3 Lab Sessions

- Hands-on activities split into two ~3-hour sessions
- Learner proceeds from one topic to the next at his/her own speed
- Lab Session 1
 - Starts with a short description on how to access the remote system
 - Continues with a high-performance test-drive, where the participant is guided to extract the maximum performance of the coprocessor
 - Finishes with the benchmarking of a basic scientific application (N-body simulation)
- Lab Session 2
 - Starts with an overview of task parallelism with OpenMP
 - Continues with an overview of process parallelism using MPI
 - Concludes with a step-by-step optimization of a real-world code example (N-body simulation)

CL2 - Lab Session 1

- 1. Introduction to the Intel Xeon Phi Processor (KNL)
 - Overview of the hardware architecture
 - Overview of Parallel Architectures and Programming
- 2. Compiling and running simple applications
- 3. Getting started on KNL
 - Cornell Univ. Virtual Workshop Training

CL3 - Lab Session 2

- 1. Task Parallelism with OpenMP
- 2. Process Parallelism: MPI programming models
- 3. Using Intel Math Kernel Library (MKL)
- 4. Running a basic N-body simulation

(available on 2nd week of the school)

Intel / Unesp servers for the labs

- Host Servers [total: 6]
 - Processor
 - ❑ Intel Xeon Phi Processor (KNL - model 7250F)
 - ❑ 1.40GHz, 68 cores, 16 GB High Bandwidth Memory
 - Main memory
 - ❑ 96 GB (6x 16GB DDR4)
 - Storage
 - ❑ 800 GB (Intel SSD)
 - Network
 - ❑ 2x 1 Gigabit Ethernet
 - ❑ Integrated Omni-Path Fabric

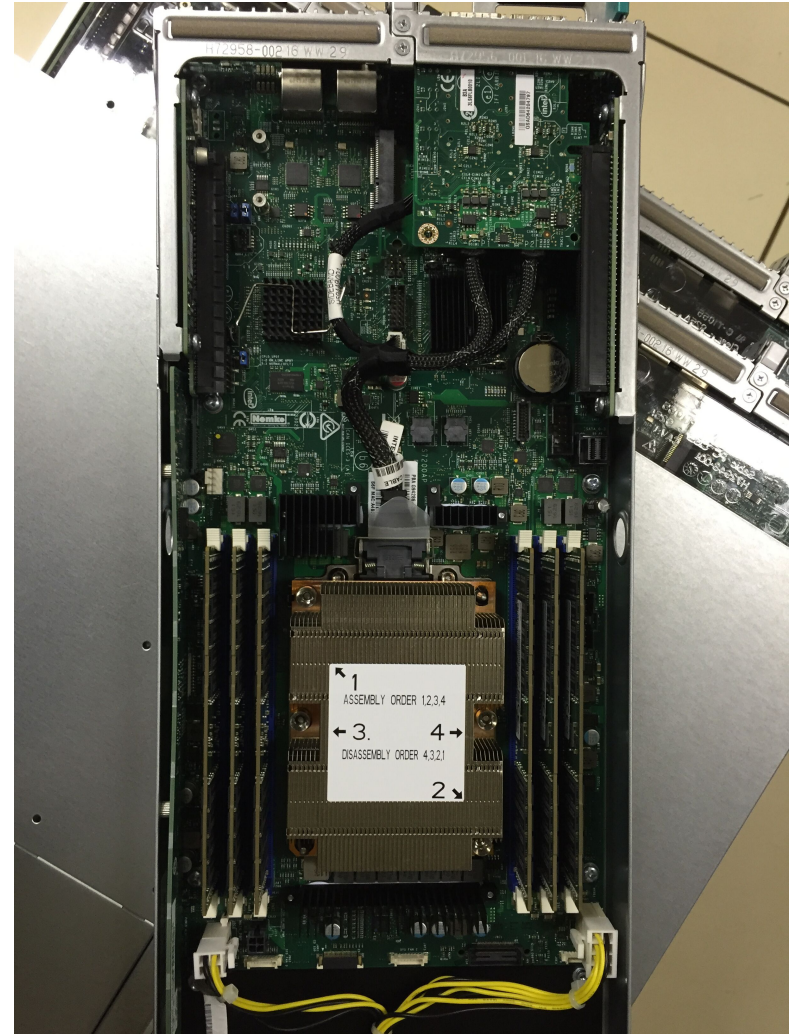
INTEGRATED

	Cores	Ghz ³	Memory	Fabric*	DDR4	Power
7290* Best Performance/Node	72	1.5	16GB 7.2 GT/s	Yes	384GB 2400 MHz	245W +15W fabric
7250 Best Performance/Watt	68	1.4	16GB 7.2 GT/s	Yes	384GB 2400 MHz	215W +15W fabric
7230 Best Memory Bandwidth/Core	64	1.3	16GB 7.2 GT/s	Yes	384GB 2400 MHz	215W +15W fabric
7210 Best Value	64	1.3	16GB 6.4 GT/s	Yes	384GB 2133 MHz	215W +15W fabric

Learn more: www.intel.com/xeonphi



Intel Xeon Phi KNL servers





Rogério Iope, Jefferson Fialho, Raphael Cóbe, Silvio Stanzani
São Paulo State University – Center for Scientific Computing

Thanks for your Attention!