SUPIX-2: Beam Telescope Oriented MAPs based on SMIC 0.18μm process @SDU

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Introduction

Since more and more high precision devices are being applied to high energy physics experiment, such as micro channel plate(MCP), charge coupled device(CCD), silicon drift chamber(SDC), silicon strip detector pixel detector and so on, the development of the beam telescope in China is under required. A beam telescope oriented project was set up by Shandong University(SDU) pixel group in 2018 and SUPIX-2 is the first beam telescope oriented monolithic active pixel sensor developed at SDU.

In order to achieve high spatial resolution and high performance of the detector, the geometry of the pixel sensor should be simulated in advance via TCAD for instance, the pixel pitch, the diode size, gap width etc.

Keywords: MAPs, pixel detector, beam telescope, TCAD, simulation

Sensor optimization via TCAD

About TCAD

Technology Computer Aided Design(TCAD) is a branch of electronic design automation that models semiconductor fabrication and semiconductor device operation.

The simulation tool we use is Sentaurus owned by SYNOPSYS Inc[1].

Characteristics of SMIC 0.18 μm process[2]

Tri-well: Nwell, Pwell, Dnwell

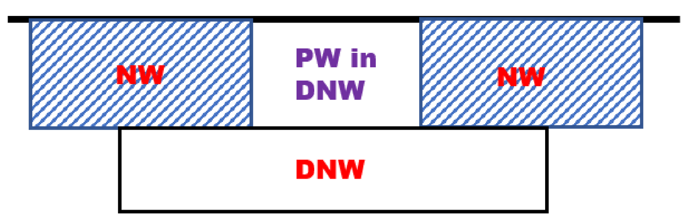
NO Epi-layer and 10 Ω·cm substrate

d ~ $\sqrt{\rho \cdot v}$

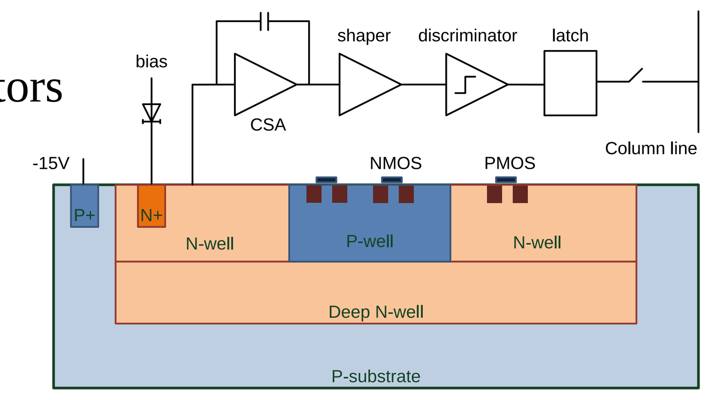
SMIC 0.18 μm process→ 15V

Circuits are realized mainly by NMOS Transistors

PMOS is coupled with collection electrodes



(a)



(b)

Fig. 1.Diagram of the sensor characteristics(a) and in pixel circuit(b)

Two Schemes of sensor geometry

There are two diode geometry design based on 50μm × 50μm pixel pitch as Fig.2 shows: 1) small diode with 8μm × 8μm Nwell, 3μm × 3μm DNwell and Pwell lays between diodes; 2) large diode with 33μm × 33μm Nwell, 30μm × 30μm DNwell, 16μm × 16μm Pwell.

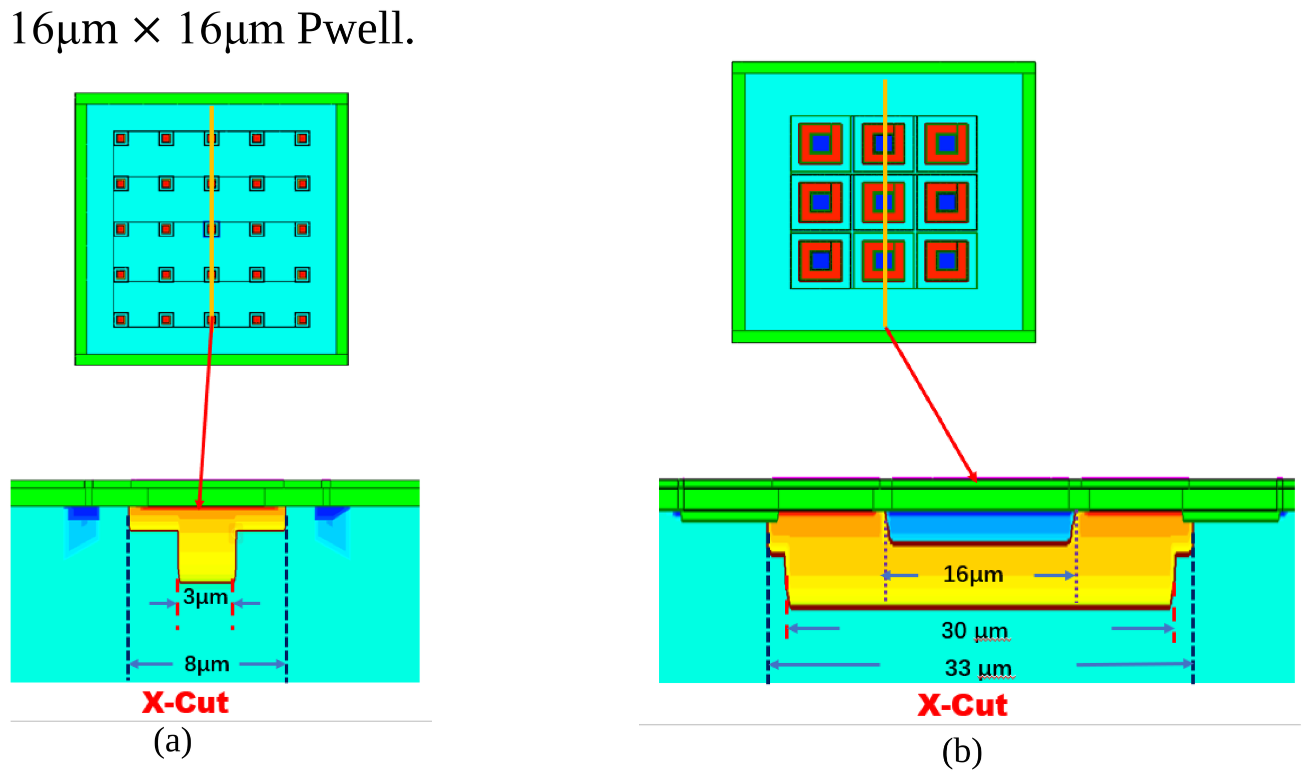


Fig. 2.Geometry of small diode sensors(a) and large diode sensors(b)

AC & DC coupled results

The diode capacitance of the sensor which partially dominates the detector noise also be simulated in advance with AC coupled and the leakage current for sensor at work could be simulated via DC coupled, more importantly the depth of depletion zone in the sensor could be calculated via simulation just as fig. 3 figures out.

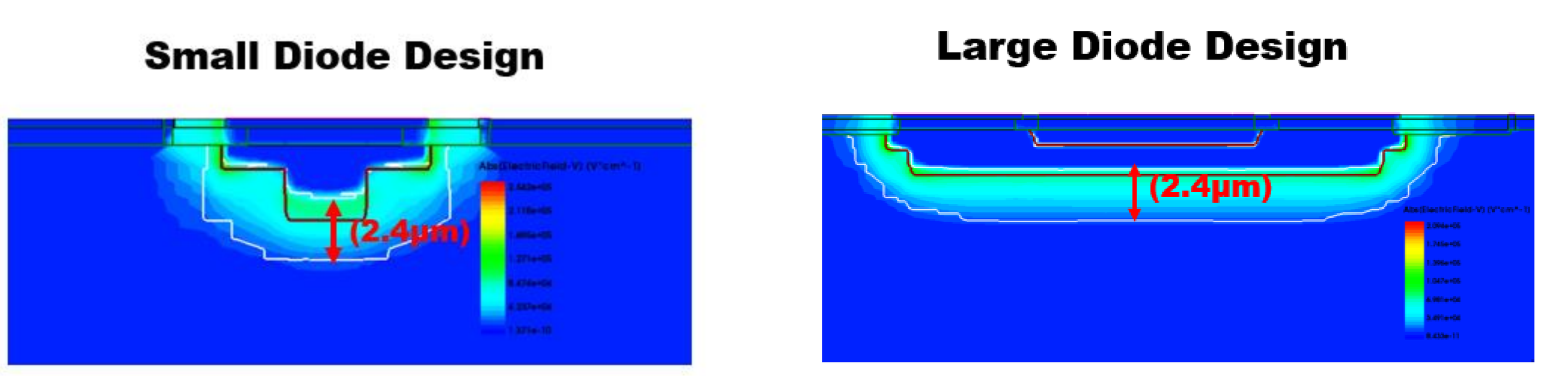


Fig. 3.Depth of depletion zone for small diode sensors(a) and large diode sensors(b)

The diode capacitance, leakage current and the depth of depletion zone were all simulated at the sensor bias of 15V according to the SMIC 0.18 μm process design rule.

Both of the designs got the depth of the depletion zone about 2.4 μm since the same resistance and bias voltage. Diode capacitance for small diode one and large diode one are 6 fF and 168 fF respectively, and for leakage are 86 fA for small one and 571 fA for large one.

MIPs model simulation results

The charge collection efficiency(CCE) could also be simulated via MIPs model. In this work, 2000 electrons was produced via MIPs model just as Fig. 4 shows, in which case the central pixel would be the hit pixel and seed pixel. The charge collection process could be illustrated in Fig. 5, and the total collected charge by small diode sensor was 1063 e^- and 1637 e^- for large diode sensor. And another property for sensor which is 90% collection time are 26.8 ns and 43.3 ns respectively.

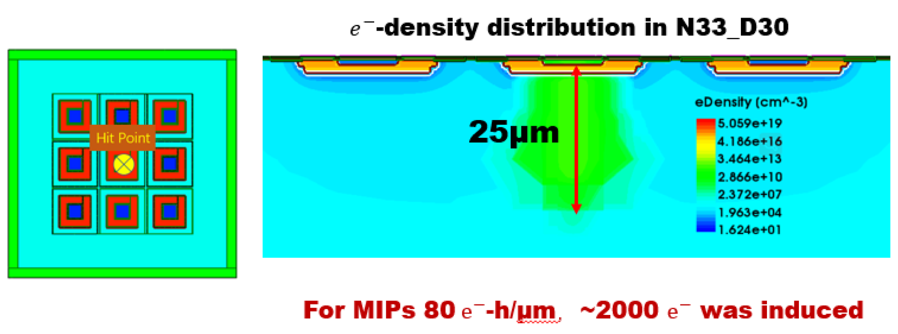


Fig. 4. Diagram of MIPs charge production mechanism

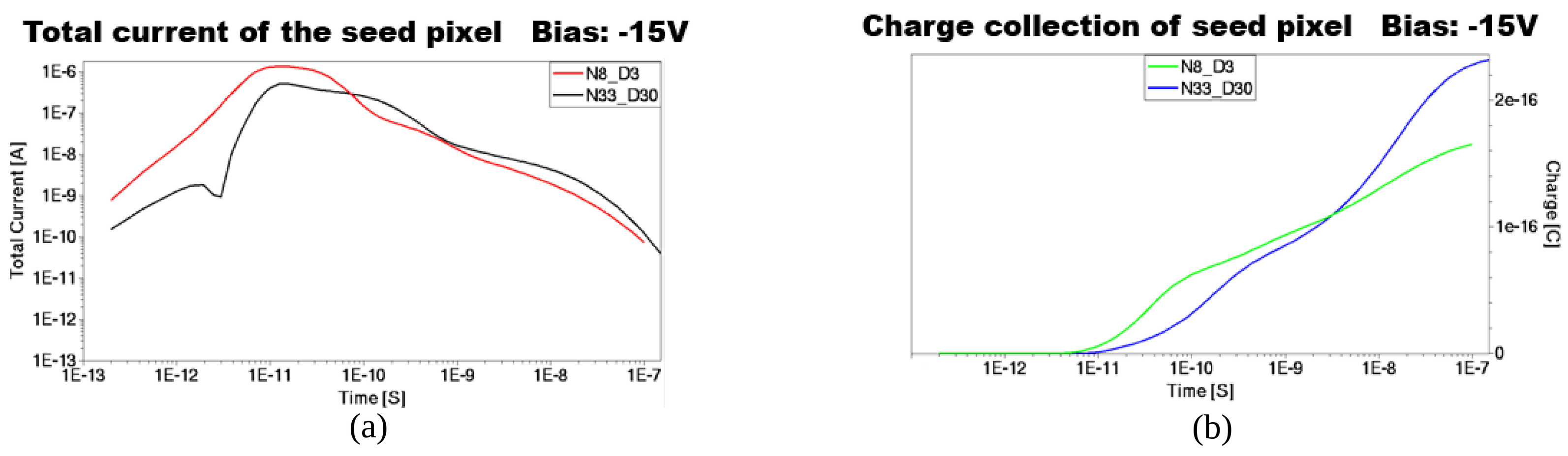


Fig. 5. Total current(electrons, holes) variation with time(a) and charge collection against time(b) for seed pixel

Charge sharing simulation results

It seems that each sensor design is reasonable: high CCE and short collection time, but when it comes to charge sharing, problems shows. Fig. 6 shows the procedure of charge sharing simulation. Problem is that when you get higher single point resolution, the threshold would be lower to achieve pitch/2$\sqrt{12}$ resolution, for small diode sensor 56 e^- would be hard to achieve considering the extra noise from the front end electronics, and 118 e^- is available for large diode sensor.

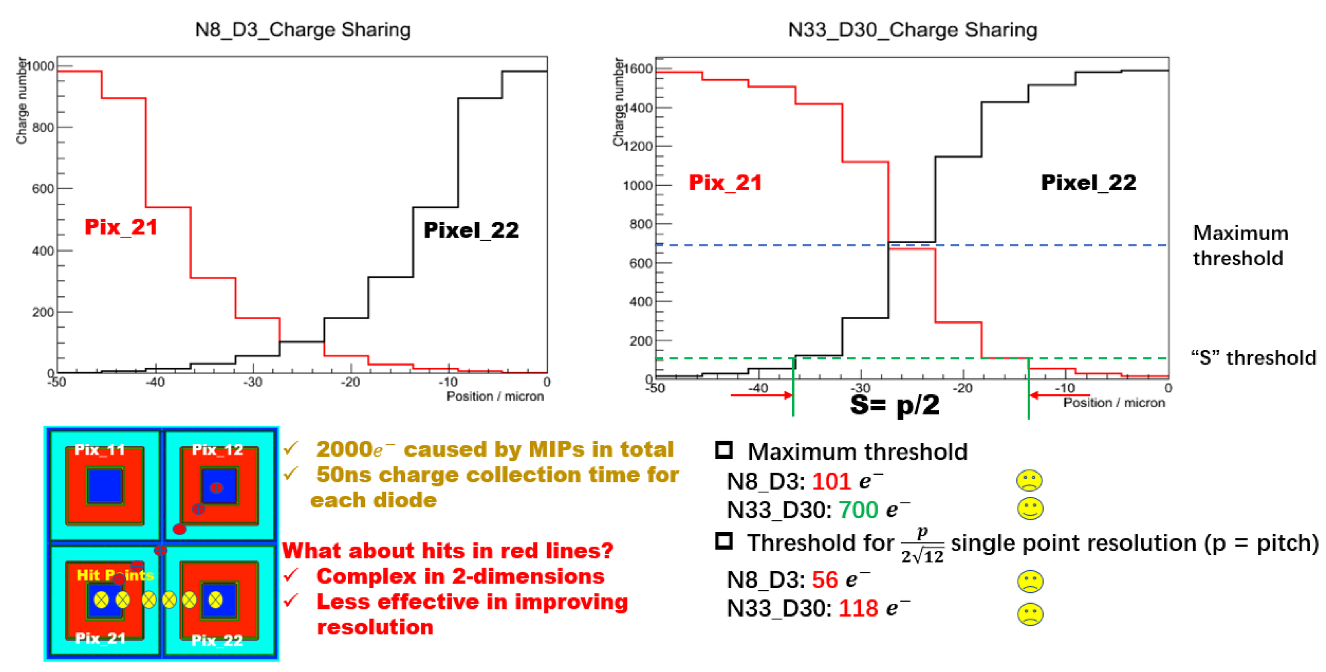


Fig. 6. Charge sharing simulation procedure with multi hit in 2×2 matrix of pixels and the charge sharing result for small diode(left) large diode(right)

Test system for SUPIX-2 prototype

In order to measure the performance of SUPIX-2 prototype, a chip test system was developed at SDU which based on commercial xillybus[3] ip core called "supix", illustrated in Fig.7 And Fig.8 gives a typical noise distribution of SUPIX-1 prototype.

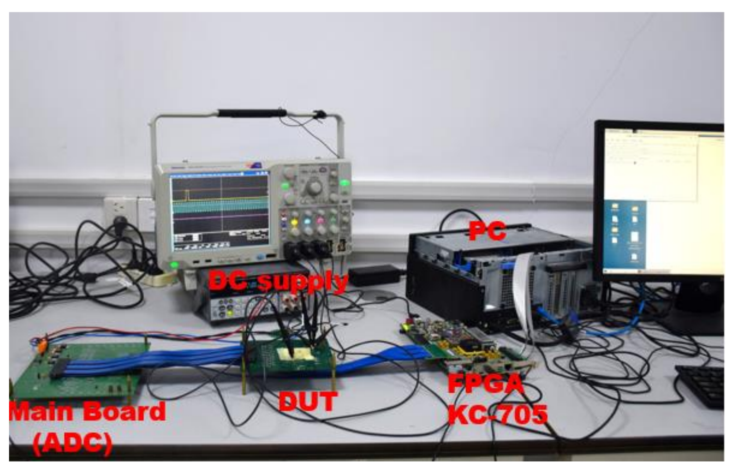


Fig. 7.Chip test system for SUPIX series

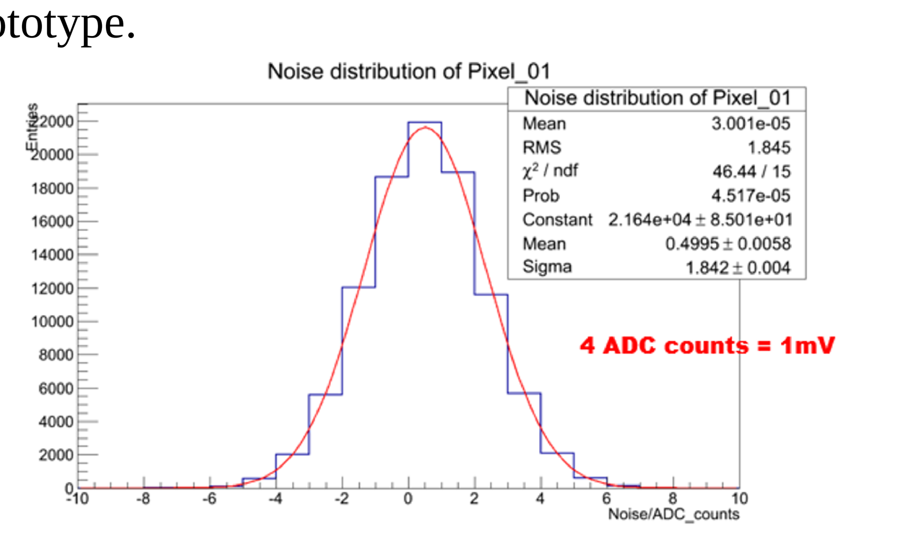


Fig. 8.Typical noise distribution for SUPIX-1 with supix test system

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