Discussion on the readout architecture of the CLICTD chip

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Outline

- Requirements
- Pixel architecture
- Slow control interface
- Configuration
- Readout
- Summary

Requirements

- Requirements for a monolithic chip for the CLIC silicon tracker *[1]*:
  - Single point resolution in one dimension $\leq 7\ \mu m$
  - Length of short strip/long pixel (strixel): $1\ - 10\ mm$
  - 10 ns time slicing, with a counter depth of 8-bits (Time of Arrival)
  - No multi-hit capability
  - Energy measurement (Time over Threshold): 5-bits resolution
    - Time walk correction
    - Particle identification (under study)
    - Study the signal development in the prototype
  - Silicon thickness $\leq 200\ \mu m$
  - Power consumption $< 150\ mW/cm^2$ (after power pulsing)

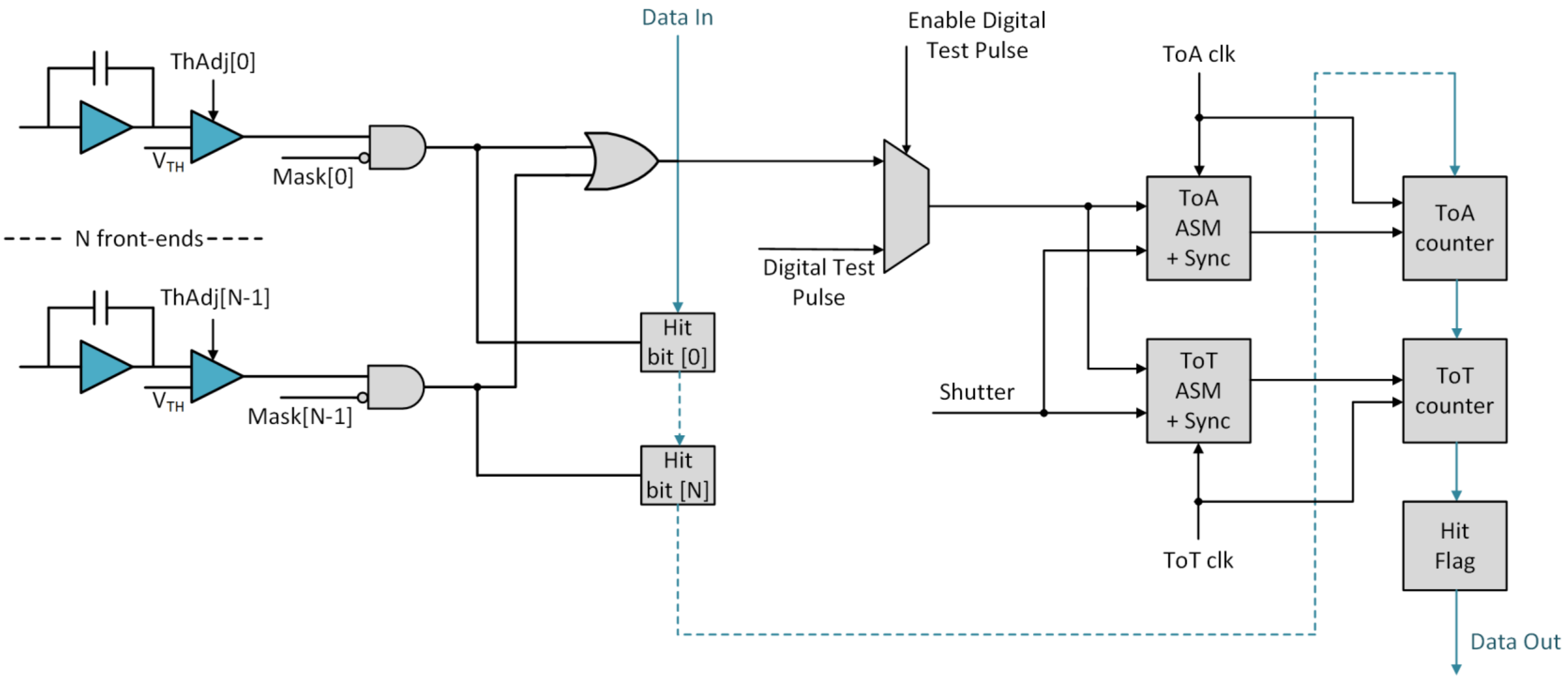
- Design of a cell measuring $30 * 300\ \mu m^2$ to be implemented for the first prototype
  - The cell will be segmented into sub-pixels ($\sim 30\ \mu m\ pitch$), to ensure prompt charge collection
  - A simultaneous 8-bit Time of Arrival (ToA) and 5-bit Time over Threshold (ToT) measurement is implemented
  - The pixel operates on a 100 MHz clock in order to provide the required 10 ns timestamping
  - The clock is enabled in the pixel only when there is a hit, and also during configuration/readout

- Note:
  - The matrix area for the first prototype will probably be $\sim 3 \times 3\ mm^2$. However, the design is foreseen to be scalable
  - The data rates in the next slides have been estimated assuming a full-size matrix, measuring $\sim 1.5 \times 1.5\ cm^2$

[1] D. Dannheim, A. Nürnberg: Requirements for the CLIC tracker readout (CLICdp-Note-2017-002)
https://cds.cern.ch/record/2261066

Pixel architecture

- The following architecture is followed for the CLICTD pixel design:
  - Each front-end will consist of a collecting diode, a charge sensitive amplifier and a discriminator
  - A 3-bit local threshold tuning DAC will probably be included in each front-end
  - A bit storing binary (hit / no hit) information is connected to each of the front-ends
  - The discriminated outputs are combined by means of a logic ‘OR’ gate
  - The combined output is then used as an input to the digital part
  - The proposed architecture has to be validated with simulations



Pixel architecture

- Each of the 10 front-ends will include a discriminator
  - A flag is raised for each front-end when a hit is detected
  - 10 bits are added in order to store the binary hit information for the 10 front-ends
  - The added bits can be used to shift additional configuration data in the pixel (similar to the ToA/ToT counter bits)

- The pixel can be programmed in 3 different modes of measurement

Mode	Description
Nominal	8 bits timestamping information (ToA) + 5 bits energy information (ToT)
Long counter	13 bits timestamping information (ToA)
Photon counting	13 bits photon counting (number of hits that are above the applied threshold)

- A compressed or uncompressed readout can be selected using a hit flag that goes high when there is a valid hit

Slow control interface

- A standard I²C interface *[2]* is used for controlling the CLICTD chip
  - 2 lines (SDA, SCL) are needed for the slow control
  - Support of multi-chip operation on the same bus can be added (if needed)
  - Nominal operating frequency: 400 kHz

- Status:
  - RTL taken from the C3PD slow control interface (implemented and silicon-proven)
  - A tri-state IO buffer will be needed → available from ALPIDE libraries

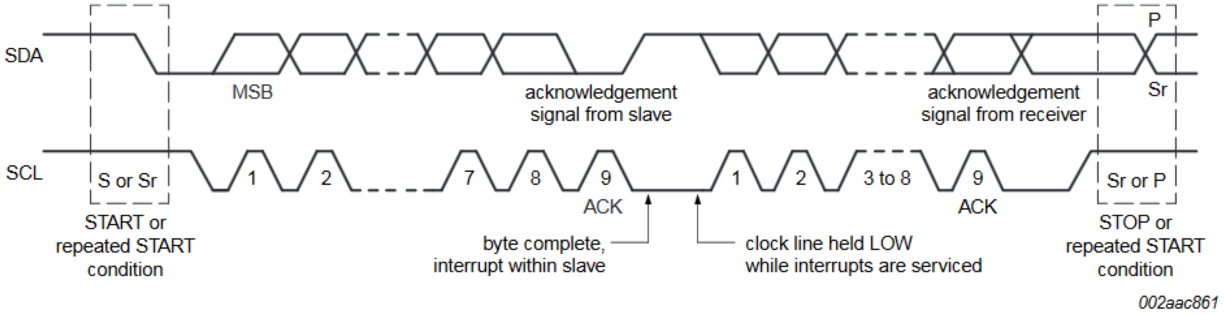
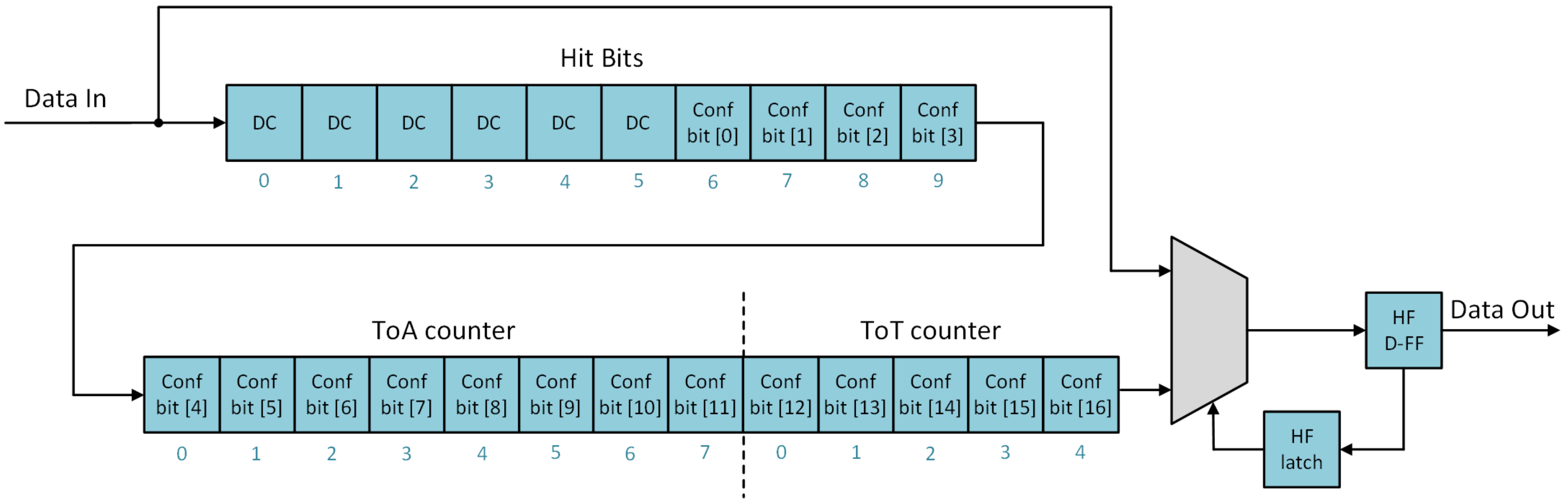

SDA
SCL
P
Sr
MSB
acknowledgement signal from slave
acknowledgement signal from receiver
S or Sr
1
2
7
8
9
ACK
1
2
3 to 8
9
ACK
Sr or P
START or repeated START condition
byte complete, interrupt within slave
clock line held LOW while interrupts are serviced
STOP or repeated START condition
002aac861

Fig 6. Data transfer on the I²C-bus

[2] *NXP, I2C-bus specification and user manual, 2014*
http://www.nxp.com/documents/user_manual/UM10204.pdf

Configuration

- A total of 51 configuration bits are assumed per pixel:
  - 5 configuration bits per front-end
    - Analog test pulse enable bit, mask bit, 3 bits for the local threshold tuning DAC
  - 1 enable bit for the digital test pulse injection (directly to the input of the digital part)
- The configuration bits can be shifted in the pixel in 3 stages, shifting 17 bits in the pixel for each stage
- Two signals are used in order to select between configuration, counting and readout:
  - count_readoutn: sets the counters to LFSR or shift-register mode. 1 for counting, 0 for configuration/readout
  - conf[2:0]: stays high during configuration. When it is set to low, the configuration data are latched. This is a 3-bit line, where each bit is used for one of the configuration steps
- Other configuration signals, common to all pixels, will be routed along the column using global lines
  - enable/disable photon counting, 13-bit long counter, compression scheme, ToT clock divider



Configuration

- The I^{2}C interface used for the slow control can also be used for configuring the matrix

- Configuration data are shifted into each column starting from the top

- The number of configuration bits per pixel is 51, and the user would need to fill the in-pixel registers 3 times in order to fully program it (3×17 configuration bits)
  - However, this requires to also write the "don't care" bits (DC), meaning that 24 bits need to be shifted into the pixel for each configuration stage

- The total number of bits needed to program the matrix, for a matrix area of $1.5 \times 1.5\ cm^2$ (500×50 pixels) , is:
  - $24\ bits\ \times 500\ columns\ \times 50\ rows\ \times 3\ configuration\ stages = 1.8\ Mbits$
  - A register with length equal to the number of columns can be loaded, shifting each time one configuration word (ie. one configuration bit per column)
  - Total configuration time: $\sim 5\ s$

- For each configuration stage, the configuration data that have been shifted into the pixel are latched in the corresponding configuration latches
  - A readout operation shall follow each configuration stage in order to shift zeroes in the matrix and reset all registers (and also to confirm that the correct data have been shifted into the matrix)

Requirements for the CLICTD readout

- During the CLICTD readout, the data stored in the pixel are shifted out in the following order (total 24 bits per pixel):
  - Hit flag (1 bit) + ToT counter value (5 bits, MSB first) + ToA counter value (8 bits, MSB first) + Hit bits (10 bits, MSB first)

- The data will be shifted out of the column, reading first the pixel at the lowest row and then the ones above
  - The End-of-Column block will count the number of bits that have been read out per pixel, as well as the number of pixels that have been read out (taking into account the compression scheme)
    - A flag will be raised once the column has been fully readout
    - Zeroes are shifted in the column during readout in order to prepare the pixel for the next acquisition

- The readout needs to be compatible with the existing data acquisition system (Caribou *[3]*)
  - In order to be compatible with the PLL in the FPGA, the data at the output of CLICTD will need to be transmitted at a frequency > 600 MHz

- The initial proposed architecture for the readout is similar to the one of CLICpix2
  - 8b/10b encoded output, based on the Ethernet standard
  - Two columns (double-columns in the case of CLICpix2) are read in parallel using a 320 MHz clock
  - The data are transmitted in double data rate (transmitting at both the positive and the negative edge of the clock), resulting to a transmission at a frequency of 640 MHz

[3] A. Fiergolski, A multi-chip data acquisition system based on a heterogeneous system-on-chip platform, 2017
https://cds.cern.ch/record/2272077/files/CLICdp-Conf-2017-012.pdf

Compression scheme

- Comparison between compressed and uncompressed readout
  - Assuming an occupancy of 3%, and a matrix area of $1.5 \times 1.5\ cm^2$ (500×50 pixels)
  - The readout time is calculated assuming a readout at 640 MHz
  - No compression:
    - 23 bits are read out per pixel (8 bits ToA, 5 bits ToT, 1 hit flag for each of the 10 front-ends)
    - Total: 575 kbits per frame
    - Readout time: 900 µs
  - Compressed readout at pixel level:
    - 24 bits are read out for the pixels that are hit (8 bits ToA, 5 bits ToT, 1 hit flag for each of the 10 front-ends, 1 hit flag for the pixel)
    - 1 bit is read out for the pixels that are not hit (hit flag for pixel)
    - Total: 42.25 kbits per frame (assuming 750 pixels hit – 3% occupancy)
    - Readout time: 66 µs
  - Compressed readout at pixel and column level:
    - 1 bit is read out for the columns that are not hit
    - Total: 36.9 kbits per frame (assuming 750 pixels hit – 3% occupancy, distributed randomly around the matrix) (average value over 1000 repetitions of the calculation, with a standard deviation of 342 bits)
    - Readout time: 58 µs
  - Target for readout time is: < 800 µs *[4]*

[4] P. Valerio, Electronic systems for radiation detection in space and high energy physics applications, 2013 *https://cds.cern.ch/record/1610583/files/CERN-THESIS-2013-156.pdf*

Discussion on CLICTD readout architecture

- A compressed readout at pixel level is proposed for the CLICTD chip
  - Compression at pixel **and** column level would require additional routing in the pixel (apart from the added complexity) for a small gain in readout time

- Distributing a 320 MHz clock along the column may be limiting for a 180 nm process

- An architecture where data from several columns are shifted out in parallel using a 100 MHz clock and then serialised could be suitable for the CLICTD chip

- Note: differential line driver/receiver is available
  - Receiver has been tested up to 40 MHz – simulations will need to be performed for higher frequencies
  - Driver has been tested for data transmissions up to 1.2 Gbps

Summary

- The CLICTD pixel will contain 24 bits that need to be read out
  - Each of the segments will consist of a collecting diode, a Charge Sensitive Amplifier (CSA), a discriminator and probably a 3-bit local threshold tuning DAC
  - Test pulse injection is foreseen for each front-end individually

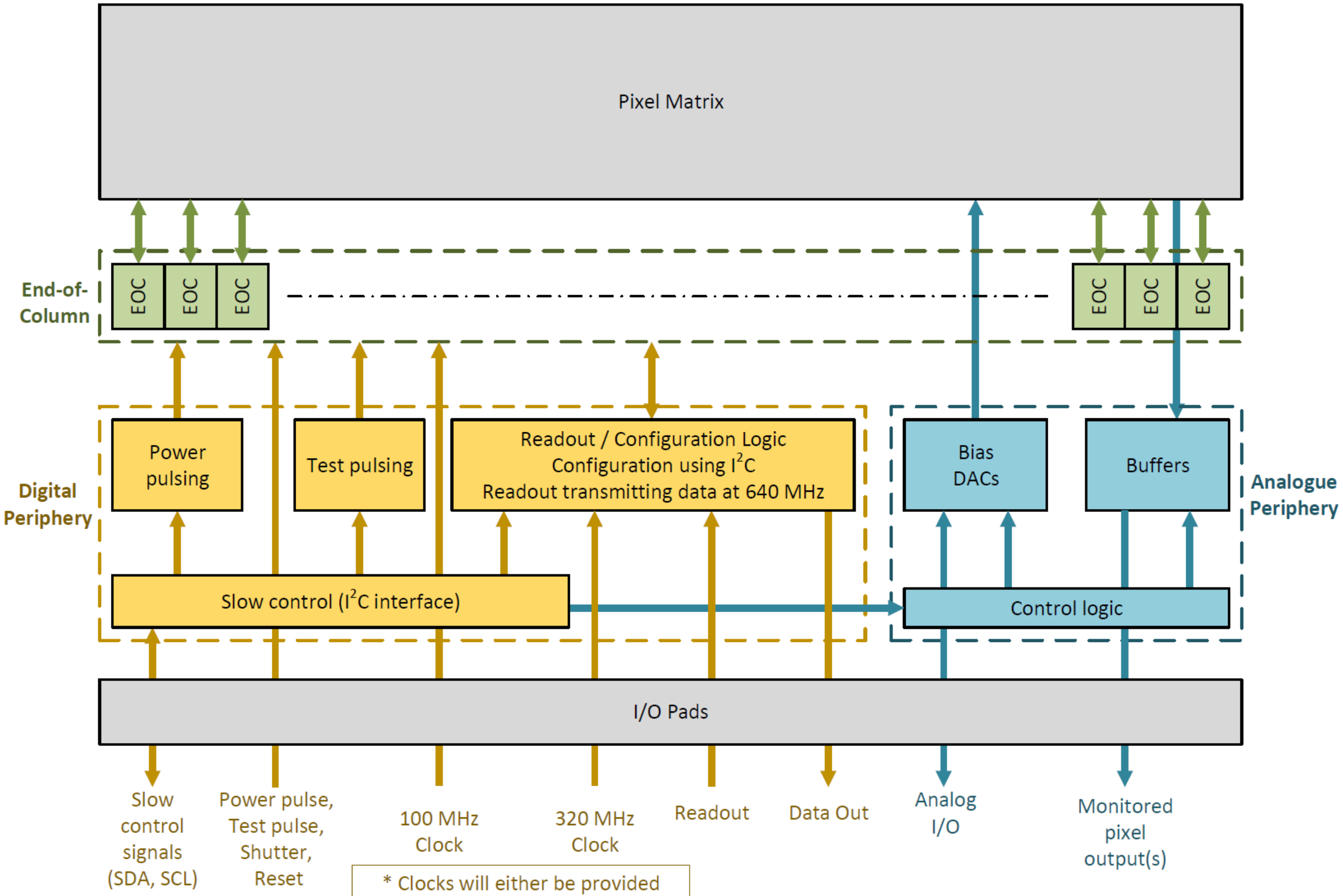
- I^2C interface will be used for the slow control of CLICTD
  - And probably for configuration
  - Configuring the chip using standard I^2C frequency (400 kHz) may take up to a few seconds (for a full-size chip)
  - However, configuration will be performed only once, at the beginning of each run

- The serial readout frequency should be > 600 MHz, such that compatibility with the existing data acquisition system will be kept

- A compression scheme using one hit flag per pixel is proposed
  - The pixel (24 bits) is only read out when there is a hit
  - If there is no hit, only the hit flag is read out

Additional slides

Chip integration – block diagram



* Clocks will either be provided externally, or generated internally using a PLL. In the case that a PLL is used, a 40 MHz reference clock will be provided externally to the chip