	LHCb UT DETECTOR Cooling Requirements		
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Requirements Document

LHCb UT DETECTOR
Cooling Requirements

This document lists the requirements for LHCb UT DETECTOR thermal management, in particular the CO_2 system for stave cooling. It gives the general requirements for its operation, expected heat loads, and temperature needs for the main cooling. It also gives the environment requirements and needs for inert gas flow.

This document is intended to form a basis for the LHCb UT DETECTOR cooling system construction, plant, distribution system and for the Process and Instrumentation Design (P&ID).

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History of Changes

Rev. No.	*Date*	*Pages*	*Description of Changes*
0	5/9/2014	**	Created
0	10/10/2014		Op. modes defined, powers settled, modularity half-plane defined
0	20/1/2015		Operation modes refined
1	26/2/2015		EDMS temporary
1	29/6/2015		Corrected after comments
2	6/8/2015	18	Editorial and structural modifications
2.1	4/9/2015	19	Addition of thermal figure of merit
2.2	1/10/2015	19	Corrections
2.3	3/7/2016	21	Addition of responses from Cooling EDR

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1. Executive Summary

The **Cooling System** for the **LHCb UT (Upgrade Tracker) DETECTOR** is needed to cool the detector during its operation, extracting the power dissipated by the electronics, the sensor self-heating and any other thermal power generated in the detector, whilst maintaining the nominal operating temperature for the silicon sensors and their associated read-out electronics.

The cooling system per se is comprised of the CO_2 cooling plant, the cooling fluid distribution, its controls, monitoring, and environmental gas. It also includes the CO_2 manifolds and connection pipes up to the UT box. The system is planned to be installed, commissioned and ready for detector operation during the 2018-2019 LHC shutdown.

The basics of the UT cooling system are summarized:

- Fluid: CO_2
- Cooling system: 2-Phase Accumulator Controlled Loop (2-PACL)
- Cooling power: Rated at 5000 W @ –35 °C

2. Brief Resume of the UT Detector

The basics of the baseline UT Tracker which are relevant to cooling issues are summarized in this section. The UT Tracker is designed for the LHCb Upgrade and is located upstream of the spectrometer magnet, as shown in Figure 1.

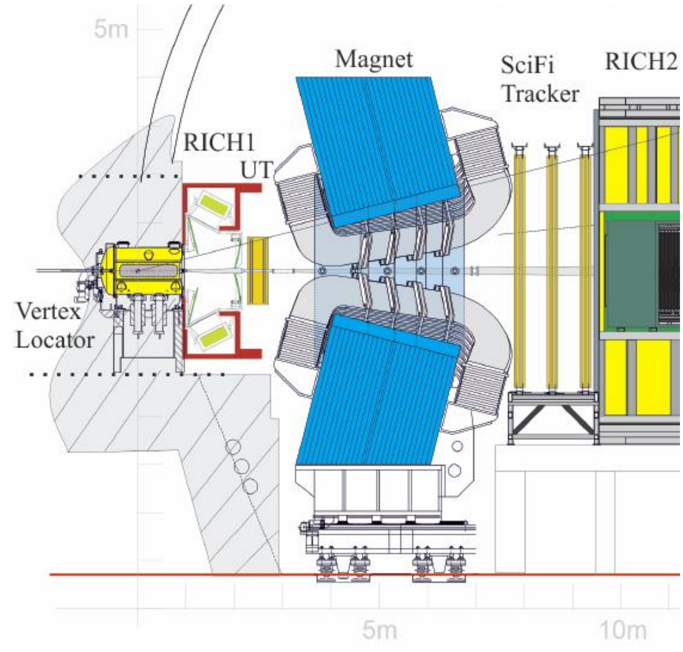


Figure 1. Schematic view of the LHCb Upgrade. The UT is located downstream of the RICH and upstream of the spectrometer magnet.

The LHCb UT DETECTOR [1] consists of arrays of silicon strip sensors, arranged in four planes which are oriented perpendicular to the beam-pipe. This arrangement is show in Figure 2. Each plane consists of vertical staves, providing the support for the sensors, readout ASICs and flex cables. These staves are mounted to an outer frame and all components are surrounded by an outer box.

The staves provide the mechanical support for the sensors and ASICs, and have an integrated cooling tube [2]. The number of staves in the upstream two planes is 16, and in the downstream planes is 18, giving a total of 68 staves.

For the staves the dissipated heat to be removed by the cooling system during operation is related to position in relation to the beam pipe. There are three different kind of staves: Type C staves, the central staves, operating on either side of the beam-pipe; Type B staves, adjacent to these moving outward, and Type A staves, comprising the remainder of the staves. For the most upstream plane UTAX, as shown in Figure 3, there are two Type A staves, two Type B staves, and twelve Type C staves. For the most downstream plane UTBX, the numbers are nearly the same, with two additional Type C staves.

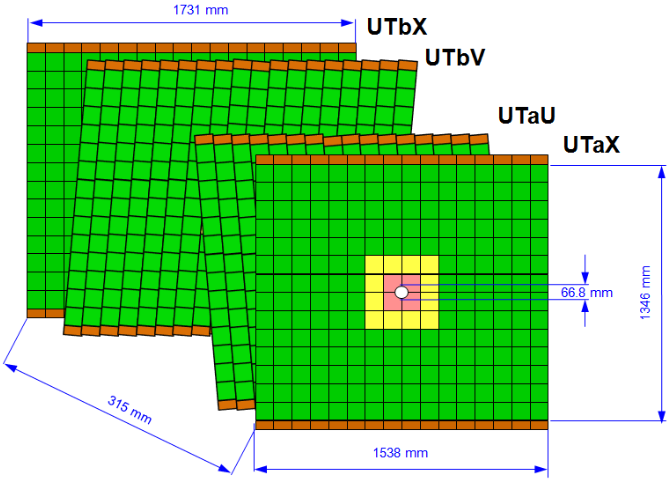
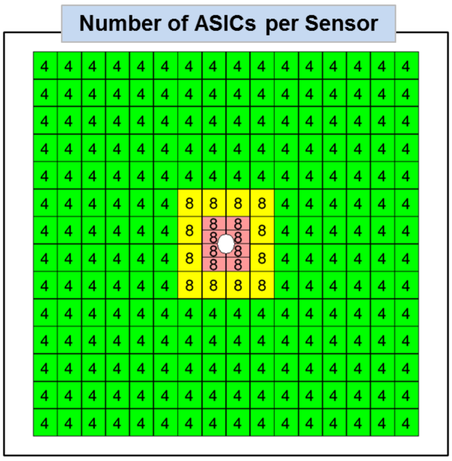


Figure 2. Conceptual view of the UT Tracker, showing the arrays of sensors for each plane.



4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
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4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4

Figure 3. Schematic of a single plane (UTAX) indicating the number of ASICs associated with each sensor in the plane. Type C staves are centered on the beam pipe, and Type A staves comprise the bulk of the staves.

Consequently, the number of ASICs varies by stave and by plane. For later consideration, the number of ASICs mounted on each type of stave is, respectively:

Stave Type C: 88 ASICs
Stave Type B: 72 ASICs
Stave Type A: 56 ASICs

So the number of ASICs on each plane is therefore:

UTaX / UTaU (16 staves each): 2 Type C + 2 Type B + 12 Type A = 992 ASICs
UTbV / UTbX (18 staves each): 2 Type C + 2 Type B + 14 Type A = 1104 ASICs

During and after assembly of the staves as a half-plane in the surface clean room at IP8, it is planned to conduct a series of tests that will check all possible aspects of the detector and its operation. We plan to test each stave as it is mounted on the frame, and all staves in a half-plane together. Will also test some group of staves in adjacent planes. The tests will include running the electronics and cooling in tandem, similar to the operational modes described below, in order to assess the performance of the cooling as well as the performance of the electronics.

Prior to this, and for the staves individually after construction but before assembly, it is planned to make a separate series of tests of the same character as described above. So a full program of testing and QA is envisioned for the staves individually and collectively in a half-plane.

One specific issue of interest is potential necessity of testing a stave under thermal shock. There is a question as to what specifically constitutes a “thermal shock”—here it is assumed to be an instantaneous change from room temp to –50°C, via a trapped slug of CO_2 as in ATLAS event.

If this is the scenario, we expect this not to harm the UT staves. A slug of CO_2 enters the manifold (a large volume at room temp), it begins to evaporate, and it distributes large vapor fraction fluid to 8 or 9 staves at once. Each stave is at room temperature, so residual liquid is evaporated completely within a short tube distance, and only cold gas flows through the stave. This would not be very efficient at cooling the stave. We estimate that the staves can handle a slug the size of several manifold volumes in this manner without appreciable harm.

It is planned to test all bare staves down to –50°C to make sure they can withstand the minimum possible temperature, but this is not a shock test. It is also planned to make similar tests on a fully-loaded stave.

3. General Detector Requirements on Cooling System

This section outlines the general functions of the UT cooling system required by the design details and expected operation of the UT Tracker.

The UT cooling scheme must remove the heat from the detector, so as to maintain the sensor operating below the temperature of –5 °C. The choice of evaporation temperature aims to keep the sensor temperature below this temperature during normal running, including after irradiation. The cooling system is expected to be capable of removing at least 5 kW of detector heat load during operation at any temperature. Additional cooling capacity shall be foreseen in order to take heat leaks on the distribution pipes and manifolds into account.

The cooling system is required to:

- Remove all heat produced inside the detector box by sensors, chips and service resistances.
- Maintain the silicon sensors at the appropriate temperatures for the different operating state.
- Allow for continuous operation at adjustable evaporation mean temperature inside the stave tube in the range of –35 °C to ambient temperature, about +15 °C (i.e., above the dew point).
- Not produce ice or condensation anywhere into the detector box and on the external surfaces.
- Comply with CERN safety regulations and LHCb safety.
- Interface to UT and DCS system, DSS systems and interlock system.

The overall design parameters of the UT cooling system are given in Table 1, and the expected environmental parameters are given in Table 2.

TABLE 1. DESIGN PARAMETERS OF THE UT COOLING SYSTEM

Property	Value	Units	Comments
GENERAL			
Cooling system	–	–	2-PACL
Cooling power	5000	W	total plus margin (see text and Table 3)
Fluid	CO_2	–	
Fluid filtration	needed	–	accessible, replaceable in technical stop
Emergency redundancy	needed	–	temporary share with VELO system
UPS connection	needed	–	minimal requirement: controls
Maximum design pressure (MDP)	110	bar	max for large volumes (safety valves)
Maximum design pressure (MDP)	130	bar	max for small volumes (burst discs)
Proof test pressure (PTP)	157	bar	test pressure for large volumes
Proof test pressure (PTP)	186	bar	test pressure for small volumes
δT_evap, Stability	0.5	°C	stability at stave (in time)
OPERATIONAL MODES			
T_evap, Normal operation	-30 ± 5	°C	cold, max power 5 kW
T_evap, Partial power operation	-30 ± 5	°C	cold, max power 2.6 kW
T_evap, Maintenance	-30 to +15	°C	cold or warm, max power 1.5 kW
DISTRIBUTION AND MANIFOLD			
Number of individual loops	68	–	one loop per stave
Control of loops	4+4	–	control at each half-plane
Manifold	in BOX	–	local, in UT BOX, connected to loops
Connection to manifold	flexible	–	needs to move with UT as box retracts
CONTROL			
Continuous T_evap control	remotely	–	controlled by 2PACL design
T_evap Set point	see mode	–	mode-dependent, common to all staves
T_evap Monitoring	stave input		at all stave inputs, plus module T readback
Plant to UT signals	as needed	–	will evolve with control design
Safety	several	–	over-pressure valves at strategic points

TABLE 2. ENVIRONMENTAL PARAMETERS RELATED TO THE UT COOLING SYSTEM

Property	Value	Units	Comments
INSIDE UT BOX			
Atmosphere (gas fill)	dry N2, Air	–	dry gas in UT BOX
Temperature, min	-50	°C	coldest possible point (CO_2 return lines)
Dew point, min	-60	°C	safety dew point
OUTSIDE UT BOX			
Atmosphere	Air	–	cavern
Dew point, typ.	14	°C	est., Kaan Vatansever beampipe simulation
Humidity, typ.	55–65	%	
Temperature, typ.	20–25	°C	

4. Specifics of Detector Requirements from Design Considerations

This section provides the specifics of the UT Tracker requirements, coming from the expected detector operational thermal field which is the driver for the local supports, stave design details, and for the cooling system coolant temperatures.

4.A. Major Detector Thermal Requirements

The main thermal requirements for the UT Tracker are stated here.

1. Temperature difference within a given sensor: Not to exceed ΔT of 5 °C

This is a constraint to limit both the deformation of the sensor due to thermal contraction, and the relevant stresses induced on the sensor by cooling it down.

2. Maximum temperature for any sensor: To be maintained below –5 °C

This is a functional requirement for the sensor operation under the worst conditions foreseen in the detector, after maximum irradiation, at the end of its life.

3. Maximum ASIC temperature: Not to exceed +40 °C

The electronics readout ASICs should be maintained at the lowest possible temperature compatible with other requirements of the system. The ASIC are the most powerful local heating source in the detector, so that their temperature is the maximum figure present in the detector.

4.B. Consequences of Detector Thermal Requirements

Consequences of the thermal requirement for the detector design and cooling system operational temperature are now discussed.

1. Temperature difference within a given sensor

This is driven by the local support (module) design. The heat dissipated by the ASICs creates a thermal flux toward the relatively colder sensor. The worst case is the sensor T3 on the central staves, having eight ASICs as readout and sitting directly over the power/data flex-bus cable. For this sensor, ΔT can be rounded to 10 °C to include a safety margin. However for the vast majority of sensors, the temperature difference ΔT should be less than 5 °C.

=> **Improvement in lowering this ΔT is possible only from modification of the local stave and module support structure.**

2. Maximum temperature for any sensor

a.) Cooling tube temperature

The calculated thermal field shows that the coolest part of the sensor is always several degrees over the external cooling tube temperature. The hottest part of the sensor is obtained by adding to this temperature the sensor ΔT.

Consequently the cooling tube temperature is required to be:

T (cooling tube) ≤ T_max (sensor) – ΔT (sensor)

≤ (–5 °C) – (10 °C)

≤ **–15 °C**

b.) Cooling tube wall ΔT

The cooling tube ID is 2 mm, with 0.1 mm wall thickness. It is a titanium tube and the internal and external pipe temperature difference is negligible for the thermal flux of interest in this configuration. Hence

$$\Delta\mathbf{T}\ \textbf{(tube wall)} = \mathbf{0\ °C}$$

c.) CO_2 internal convective ΔT

To obtain the required coolant evaporation temperature, the internal convection temperature drop need to be considered. This is a function of the thermal flux on the internal surface of the pipe and of the heat transfer coefficient (HTC). The worst case, with maximum internal convection temperature drop, comes from the central stave with a snake pipe having 80 W on a heated length of 1.6 m. The thermal flux for this pipe is in the range 10000 W/m^2 (= 1 W/cm^2).

HTC for CO_2 evaporating in the range of interest is around 5000 W/m^2K. So

$$\begin{aligned}\Delta\mathbf{T}\ \textbf{(conv)} &= \text{thermal flux / HTC} \\ &= (10000\ W/m^2) / (5000\ W/m^2K) = \sim 2\ °C\end{aligned}$$

Taking into account safety margins, a value of 5 °C can be used for an estimate. Hence the cooling fluid temperature is required to be

$$\begin{aligned}\textbf{T (fluid)} &\leq \textbf{T (cooling tube)} - \Delta\textbf{T (tube wall)} - \Delta\textbf{T (conv)} \\ &\leq (-15\ °C) - (0\ °C) - (5\ °C) \\ &\leq \mathbf{-20\ °C}\end{aligned}$$

And finally, putting a 10 °C safety margin on this yields

=> **Set point for CO_2 cooling inlet temperature in nominal operation is**

$$\textbf{T (}\mathbf{CO_2}\ \textbf{inlet)} \leq \mathbf{-30\ °C}$$

This final margin is intended to cover not only uncertainties in the simulation, but also uncertainties in construction, which have been shown during prototyping to have variations from expectation of this order.

Comments on the cooling inlet temperature. *Exactly how much it is possible to operate correctly at the lower end of the margin threshold (from colder CO_2) needs to be optimized because at lower temperatures there is a trade-off between:*

- *the benefits to the sensors operating at lower T; and*
- *the detriments to the mechanics due to thermal induced deformations and related mechanical stresses.*

The mechanical "life" of the cooling components is related mainly to:

- *the coolest temperatures in the system = max stress induced; and*
- *the number of thermal cycles, between ambient and minimum T*

In the stave, the inlet temperature and outlet pressure will be set. The temperature along the cooling tube follows the saturation fraction from the isotherm at the inlet to the pressure setpoint at the outlet, so the stave components from inlet to outlet will in general show decreasing temperatures. For clarification, see the Mollier diagram.

3. Maximum ASIC temperature

The cooling system, which is designed to maintain the sensor in the temperature range discussed above, will automatically retain the ASIC temperature in an acceptable range. From the FEA simulation, the ASIC temperature is expected to be 21°C higher than the cooling tube temperature, in the worst case.

Having fixed the T (cooling tube) ≤ –15 °C,

=> **Expected ASIC max temperature is ≤ +5 °C.**

Note. *All the considerations made on the cooling system foresee that the system will be working in the correct evaporation regime, with* CO_2 *fully boiling in the stave cooling tube channel and avoiding the dry-out. This working condition is imposed by a correctly designed inlet-outlet cooling connection system and by the proper mass flow-rate and inlet temperature/enthalpy of the coolant from the cooling plant.*

5. Baseline Heat Loads

The main heat loads for the UT Tracker are: the ASICs, the cables power dissipation, and the silicon sensors self-heating. The ASICs are presently in the design stage and so the power consumption can only be estimated. **The power consumption of the ASIC chip is estimated to be 6 mW/channel, giving 0.768 W/ASIC.** This figure is herein assumed in order to calculate the detector power dissipation and the needed cooling power. Detailed numerology of the staves and ASICs can be found in Section 2.

5.A. Readout Chips (ASICs)

An estimate of the total power dissipated by the detector electronics is now presented. The detector has the following **total number of ASICs**:

UTaX + UTaU + UTbV + UTbX: 2 * 992+ 2 * 1104 = **4192 ASICs.**

And so the estimated power dissipation from all ASICs for the detector is:

Power dissipation by ASICs = 4192 * 0.768 W = **3220 W.**

This is the major contribution to the total UT power dissipation.

5.B. Sensor Self-Heating

The silicon sensors become radiation damaged as a function of time in the LHC environment, and this results in their standing reverse bias current increasing non-uniformly with time. This causes increased Joule heating, which decreases effective resistance, which causes a further increase in bias current, which in turn causes increased heating, and so on again, in a positive feedback loop known as thermal runaway. This increasing power consumption is detrimental to stable detector operation, and the increasing bias current introduces noise. This effect is a function of radius from the beamline, and drops off as particle flux, roughly as $1/r^2$.

The power density is a function of radius for a given temperature. For expected operational conditions, this corresponds to ~400 mW for the innermost sensors, ~60 mW at intermediate r = 250 mm, and <20 mW in the outer region r > 500 mm. That is,

4 planes * 4 innermost sensor * 0.4 W = 6.4 W
4 planes * 12 intermediate sensors * 0.06 W = 2.9 W
4 planes * 936 outer sensors * 0.020 W = 7.5 W

The sensor self-heating estimated power for the detector is therefore:

Power dissipation by sensor self-heating = 6.4+2.9+7.5 W ≈ **17 W.**

This contribution is negligible in comparison with the margins put on the system cooling power.

5.C. Power/Data Cable Dissipation

To take into account the power dissipation into the power and data flex cables, 10% of the power transported is taken as an estimate, being the design value of the cables in progress. So, this estimate yields an estimate for the detector of:

Power dissipation by cables = 10% * 3220W ≈ **322W**.

5.D. Total Baseline UT Heat Load

These three contribution give the total power dissipated by the detector itself:

Total baseline power dissipation = 3220 + 17 + 322 = **3560 W**.

To this total internal heat load, the heat pickup load due to imperfect UT box detector insulation should be added. An exact calculation of this contribution is in progress, and need to be based on expected thermal environment conditions around the UT box, its mechanical design and insulation foreseen. For now, the convective load from the environment is estimated to be 500 W.

A margin is taken on the total baseline power dissipation plus the environmental load, rating the total cooling power requirement as:

Total UT Tracker heat load = 5000 W.

5.E. Non-Baseline Heat Loads

There has recently been some discussion of using a power regulator at the front end, near the ASICs. In consideration are an LDO regulator integrated into the SALT ASIC itself, or a FEAST DC/DC converter located on the module hybrid external to the ASIC. **This choice does not represent not the baseline** but the implications are severe and so are mentioned here for reference.

The additional heat load introduced by the external converter would be a function of the efficiency of the device in operation: 0.8 W for 80% efficiency (best case), or 1.3 W for 70% efficiency (likeliest case). Since one of these devices would be needed for each four ASICs, this would increase the overall heat load to nearly 1.5 times the presently anticipated level for the ASICs alone. This would raise the overall power requirement of the UT from 5 kW to 7 kW, maintaining a 20% margin.

The additional heat load of an internal regulator integrated in the ASIC would depend on the specifics of the design, and so can only be guessed at present. For reasonable efficiency, this would increase the ASIC heat load by 25%. Hence the overall power requirement of the UT would rise from 5 kW to 6 kW, maintaining a 20% margin.

Either of these increases can be handled by a more powerful cooling plant. However in the case of the converter, the spatial distribution of these new heat load points would require a major redesign of the stave, with all attendant work required, making this choice undesirable.

6. UT Operational Modes

6.A. Definition of Operational Modes

The power dissipation for each of the anticipated operational modes of the UT Tracker is summarized in Table 3. This uses the full and partial heat loads calculated in the previous section. Nomenclature used for the state of the UT box in these modes is: the position of box halves may be retracted or joined, and the condition of box as gas enclosure may be sealed or unsealed. (The use of the term “open” is ambiguous.)

1. UT NORMAL OPERATING (DATA-TAKING) MODE,

COLD: T_op = –30 ± 5 °C

Conditions. Box halves joined and sealed, electronics fully powered, full cooling to maintain the sensors temperature under –5 °C. For normal data-taking.

2. UT PARTIAL-POWER (STAND-BY) MODE,

COLD: T_op = –30 ± 5 °C

Conditions. Box halves joined and sealed, with electronics on but operating at partial power, i.e., from 10% to 50% of nominal power. For electronics testing of digital readout alone, analog readout alone, power distribution, and slow control.

Note. The sensors should be kept at a nominal temperature, under –5 °C. Although the temperature remains the same here as in normal operating mode, the power load is less. Hence the cooling power required is less, and the mass flow rate can be reduced, if needed, based upon the actual power load in the range given above.

3. UT MAINTENANCE (INSTALLATION/COMMISSIONING) MODE,

COLD OR WARM: T_op = –30 °C TO +15 °C (Room Temp., above Dew Point)

Conditions. Box halves retracted and sealed (or retracted and unsealed), electronics and cooling on for one half-plane at a time only (refers to in-pit, not on-surface operational modes). For maintenance/commissioning in pit.

Parenthetically, an additional operational mode for the UT Tracker is the bake out mode, but this is not of interest for the cooling system. During the beam pipe bake-out the box halves are retracted, the electronics is off, the cooling is off. The detector will be switched off together with the cooling with a temperature controlled transient from the cold operative condition to the ambient temperature condition.

Note. The case in which one or two staves in a half-plane are entirely powered off should be covered by the modes above. The power load is less, so the flow rate can be adjusted as needed. The stave temperature approaches the operating temperature, which should not be a problem for the stave for short periods, and also not a problem for the sensors if the environment is sufficiently dry.

TABLE 3. EXPECTED HEAT LOADS DURING VARIOUS OPERATIONAL MODES

Property	**Value**	**Units**	**Comments**
UT NORMAL OPERATING (DATA-TAKING) MODE			***T_op = –30°C ± 5°C***
Conditions: Box halves joined+sealed, electronics fully powered, full cooling (normal data-taking mode)			
SALT ASIC power	0.768	W/ASIC	assumption of 6 mW/ch
	761.9	W/plane	for each plane UTAX and UTAU
	847.9	W/plane	for each plane UTBX and UTBV
	3219.5	W/UT	total ASIC heat load
SENSOR self-heating	12.2	W/UT	worst case total, after 50 pb-1
DATA-FLEX power dissipation	321.9	W/UT	est., 10% of power carried
UT BOX load (est. convective, radiative)	500.0	W/UT	est. convective load from environment, assumed minimal, due to box insulation
BEAM-PIPE load (est. convective, radiative)	50.0	W/UT	est. max convective load from beampipe heaters
TOTAL POWER LOAD	**4103.6**	**W/UT**	load for this operational mode
	4924.3	**W/UT**	with 20% margin
	5000.0	**W/UT**	est. max expected with all loads included
UT PARTIAL-POWER (STANDBY) MODE			***T_op = –30°C ± 5°C***
Conditions: Box halves joined+sealed, electronics on partial power, cooling reduced (sensors kept at –5°C), for electronics testing of digital readout, analog readout, power distribution, and slow control			
SALT ASIC power	1609.7	W/UT	ON at 10% to 50% power (50% calculated)
SENSOR power	12.2	W/UT	worst case total, after 50 pb-1
DATA-FLEX power	161.0	W/UT	est., 10% of power carried
UT BOX load	500.0	W/UT	flat est.
BEAM-PIPE load	50.0	W/UT	flat est.
TOTAL POWER LOAD	**2332.9**	**W/UT**	load for this operational mode
	2799.5	**W/UT**	with 20% margin
	3000.0	**W/UT**	est. max expected with all loads included
UT MAINTENANCE (INSTALLATION/COMISSIONING) MODE			***T_op = –30°C to +15°C***
Conditions: Box halves retracted+sealed (or retracted+unsealed), electronics and cooling on for one half-plane at a time only, for maintenance/commissioning in pit (not on surface)			
SALT ASIC power	847.9	W/UT	ON for a half-plane (e.g. UTBX A-side)
SENSOR power	1.6	W/UT	ON for a half-plane
DATA-FLEX power	84.8	W/UT	est., 10% of power carried
UT BOX load	500.0	W/UT	flat est.
BEAM-PIPE load	0.0	W/UT	no load from beam-pipe
TOTAL POWER LOAD	**1434.3**	**W/UT**	load for this operational mode
	1721.1	**W/UT**	with 20% margin
	2000.0	**W/UT**	est. max expected with all loads included

N.B. The term "OPEN" is ambiguous:

- Position of box halves: retracted/joined
- Condition of box as gas enclosure: sealed/unsealed

6.B. Discussion

Some discussion of details related to the operational modes is given here.

1. Maximum acceptable downtime

We distinguish two different cases for the downtime issue:

During maintenance periods, we can tolerate on the order of 1 wk/yr (MAX) at room temperature. After sufficient irradiation, this is the period of beneficial annealing, beyond which further annealing will harm the sensors.

During data-taking periods, we can tolerate NO appreciable downtime, since data will be lost. Any integrated downtime would have to remain under the limit specified above.

2. Temperature ramping

During the prototyping phase, the stave was cooled at a rate of ~40°C/60-90 mins without any observable ill effects. It was left to warm at the natural rate given by interaction with ambient temperature.

For now, we take this rate (0.5°C/min) as the maximum cooling rate. The warming rate can be more relaxed, perhaps twice this. Further tests with the Milano system will be made to refine this number in due time.

7. Thermal Figure of Merit

To compare and quantify the thermal performance of detector designs, a Thermal Figure of Merit (TFoM) may be constructed. The stave resistive Thermal Figure of Merit is:

$$\mathbf{TFoM = \Delta T / P \quad [°C \cdot cm^2/W]} ,$$

where:

P = thermal power flux [W/cm^2], and

ΔT = max temperature difference between cooling tube and power dissipation source [°C].

This quantity is meaningful only when power is dissipated (P is not zero).

In the UT stave, the regions where P is most important are the areas underneath the ASICs. In this region, the thermal power flux P is calculated from the ASIC power and its footprint:

$$P = 0.768\ W / 0.62\ cm^2 \approx 1.25\ W/cm^2 .$$

Thermal FEA simulations have been used to study the temperatures in the conductive materials that are put in the thermal flow from the ASIC to the cooling tube. The maximum temperature difference between the ASICs and the cooling tube ΔT depends on the details of the stave design under consideration and the position of the ASIC on the stave. However in general, the largest differences are not far from 20 °C. So the typical range is taken as:

$$\Delta T \approx 20\text{–}23\ °C .$$

The relevant Thermal Figure of Merit for the UT is therefore calculated as:

$$\mathbf{\Rightarrow\ TFoM = \Delta T / P \approx 16\text{–}18\ °C\ cm^2/W} .$$

A more detailed TFOM can be evaluated for each design choice, and for each ASIC sensor position, since local power is not a uniform over the UT stave. From an engineering point of view, this range is sufficient to quantify the thermal aspects of the design as acceptable, and this is perfectly aligned with similarly-designed detectors already built.

For example, the ATLAS IBL stave has a similar design, with their ASICs mounted on the sensors. The relevant TFoM are in the same range as above. The power over the IBL stave can be considered uniform, and so the TFoM may be used as a characteristic stave parameter. For the UT, the power distribution is not uniform over the stave, hence a global TFoM is less meaningful in characterizing the stave in the UT case.

Comment on practical limitations. *Simulations are good design indicators, very useful to to compare and validate different design solutions, but it is important to remember that they refer to ideal cases. For example, the FEA models have perfect bondings of glued surfaces, with precisely uniform glue layers of constant thickness. Real glue layers, composites cables conductivities, and geometries could be different from the ones used in the FEA simulations. So a reasonable margin is always needed. This is also true for derived quantities like the TFoM, which should be interpreted with this in mind.*

8. Environmental Requirements

The detector box needs to have environment control on both the internal volume and the external surfaces, to avoid condensation and icing phenomena, induced by the low temperatures and the presence of water humidity in the air.

The two detector half boxes shall be filled and flushed with nitrogen (or dry air). For safety reason the requirement is that the dew point shall be kept below –60 ◦C in the box at all times when the detector is run cold. The relevant admissible maximum content of water humidity in the controlled volume is then about 10 ppm (vol).

The Detector boxes shall be designed to be airtight both when: (1) joined and sealed in the nominal position, and (2) retracted and sealed, using temporary covers.

For safety, an over-pressure limiter on the boxes through an material-appropriate bubbler is required.

9. Safety

The cooling system must meet all relevant EC standards and comply with CERN safety regulations.

In particular:

- The cooling system shall avoid liquids trapped in closed off section, include safety relieve valves where required. **This point is very important.**
- Test pressures in all sections of the cooling system, shall respect engineering standards in compliance with maximum possible fault pressures.
- The distribution system and all on-detector shall be protected from contamination by accessible filter stages.
- The detector box shall be connected to an exhaust bubbler system.
- Controls of the cooling system (plant, distribution, monitoring) need to be connected to UPS in order to retain control during a power cut.

10. References

[1] LHCb Upgrade Silicon Tracker TDR.
https://twiki.cern.ch/twiki/bin/view/LHCb/SiliconStripTracker#TDR

[2] UT Mechanical Requirements Document v3b (2013).
https://twiki.cern.ch/twiki/bin/view/LHCb/SiliconStripTracker#Mechanics

[3] Summary of the Thermal and Mechanical FEA Analysis for the Design and Optimization of the Detector Stave, EDMS Document 1517621 v.1.
https://edms.cern.ch/document/1517621/1

Appendix. Detector Thermal Studies: Reference

The design of the detector local supports follows the thermal requirement described in this document. Detailed thermal simulation have been done, see Ref.3 for details.

Herein are shown extracts of the ANSYS models used for thermal simulations. Central stave sensors, with 8 readout ASICs per sensor are the more powerful and critical for the system design. Local hot spots on the sensor has been minimized through a careful design of the substrates and cooling pipe routing. Some details are shown in Figure 4, and simulations are exemplified in Figure 5.

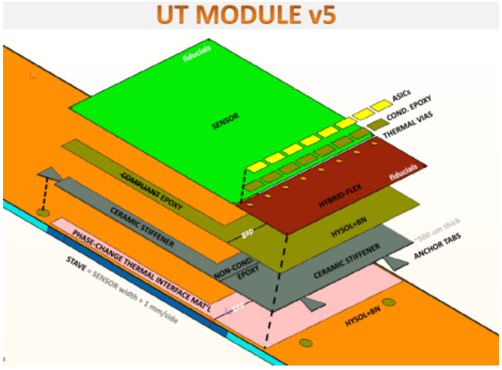

Figure 4. "Exploded" view of a module, showing the support and thermal contacts for a sensor and its readout ASICs.

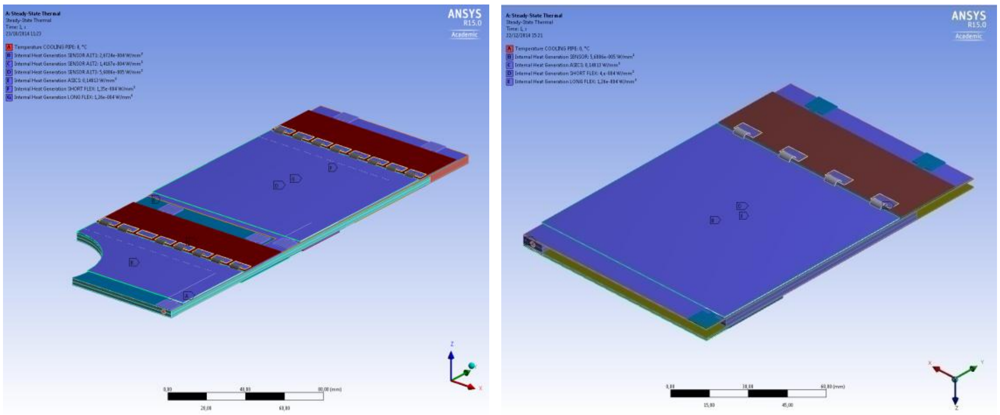

Figure 5. ANSYS finite element analysis models used for thermal simulations. (Left) T1, T2, T3 sensors on the central stave. (Right) General UT sensor.