

# *Baby-Mind Front-End Electronics*

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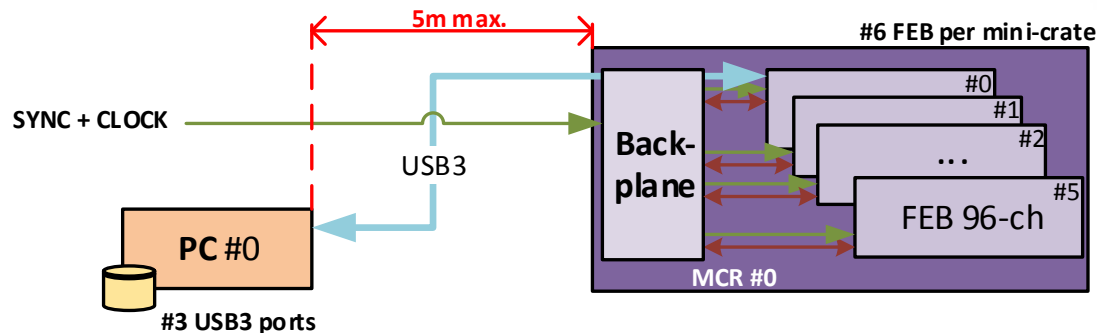
University of Geneva

8-12-2017

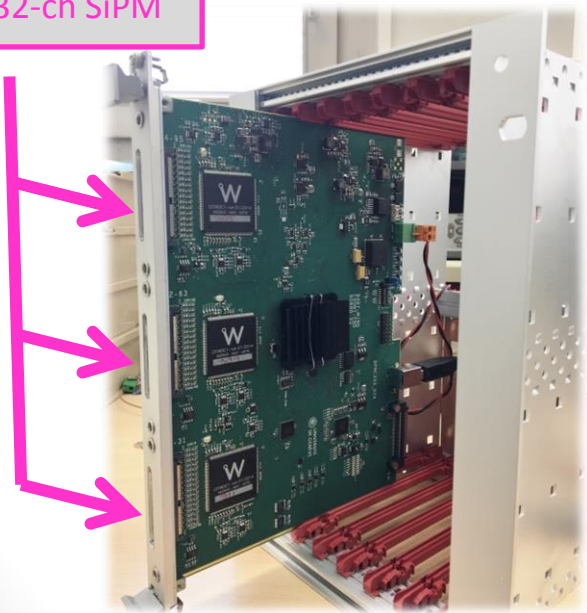
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# DAQ system overview – mini-crate



**FRONT:**  
3x32-ch SiPM



**MCR 6U (6/7 slots)**

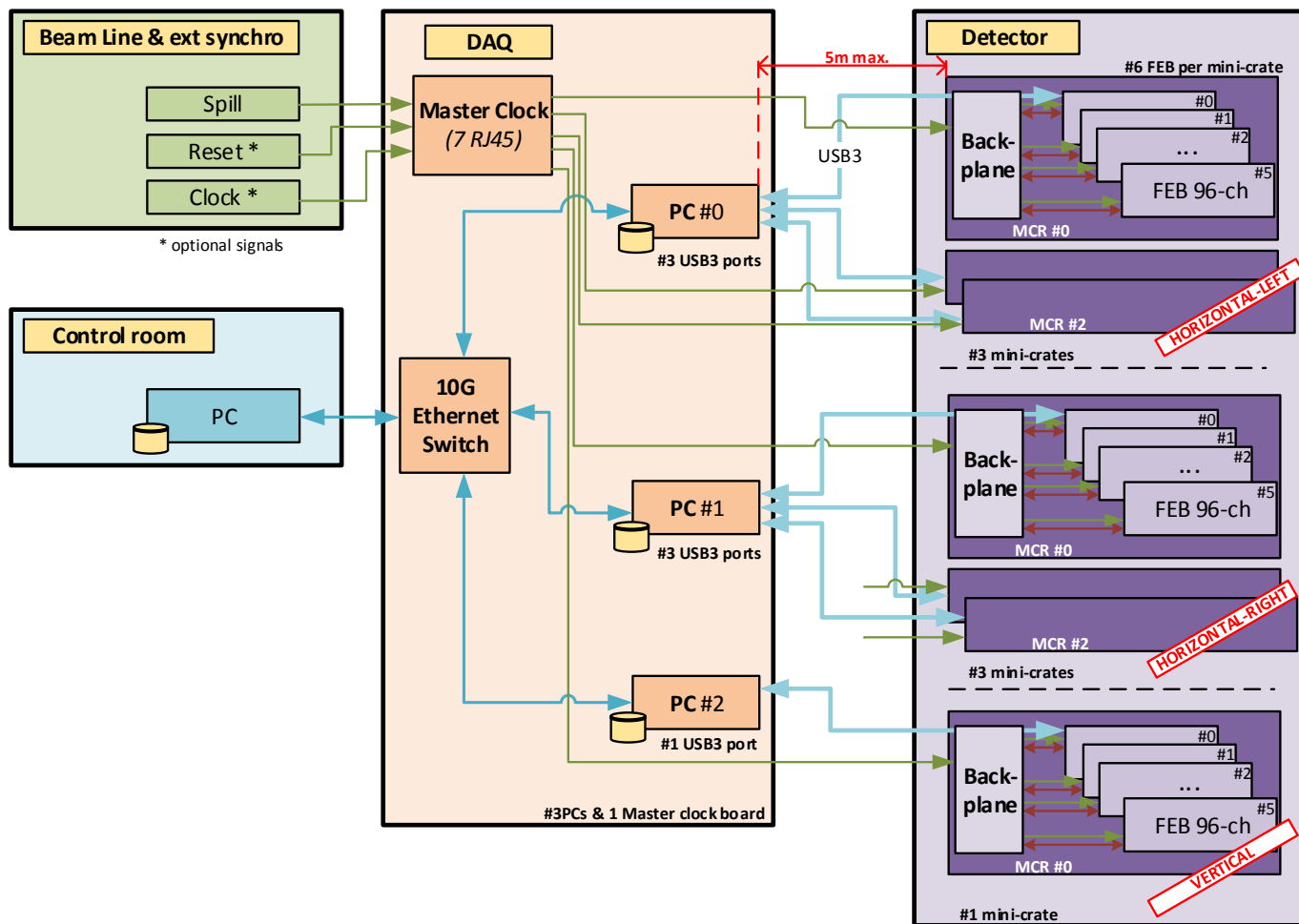


**BACK:**  
 USB  
 SYNC/CLOCK in  
 MCB out (emul.)  
 MCB in (emul.)  
 24V  
 Leds/Address  
 Prog.



# DAQ system overview – overall

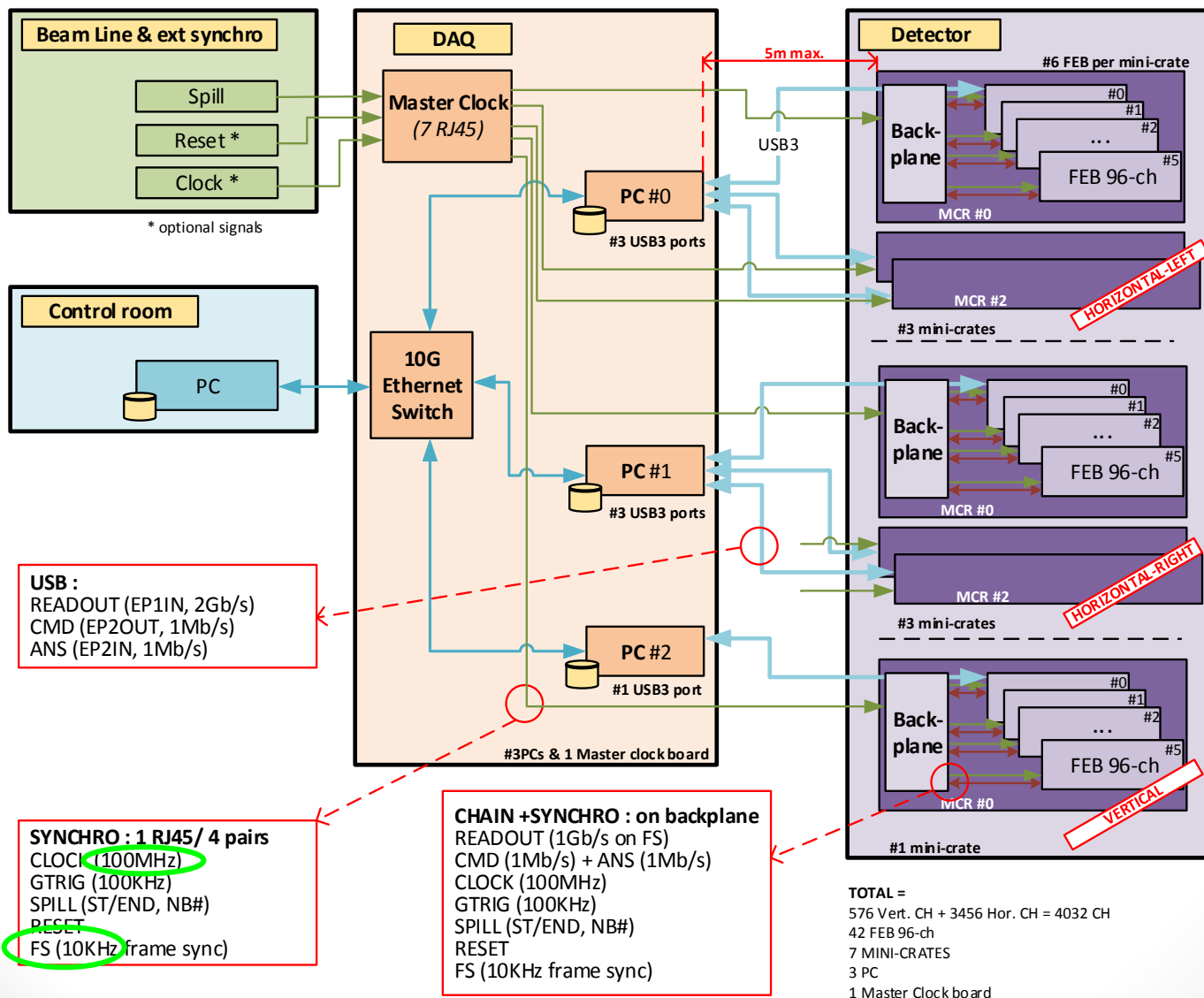
Vertical channels :	576-ch,	6 FEBs,	6 FEBs/MCR,	1 MCR/PC,	1 PC	<b>Total :</b>
Horizontal channels :	3456-ch,	36 FEBs,	6 FEBs/MCR,	3 MCR/PC,	2 PCs	7 MCR/42FEBs/3PCs



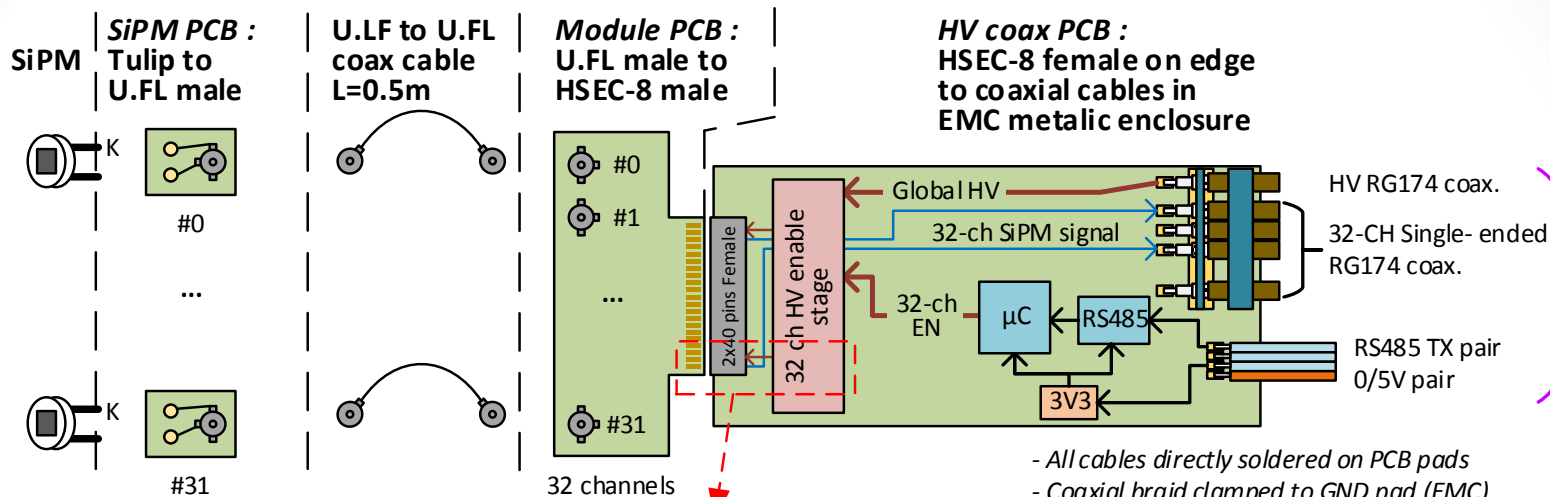
**TOTAL =**  
576 Vert. CH + 3456 Hor. CH = 4032 CH  
42 FEB 96-ch  
7 MINI-CRATES  
3 PC  
1 Master Clock board

# DAQ system overview – main signals

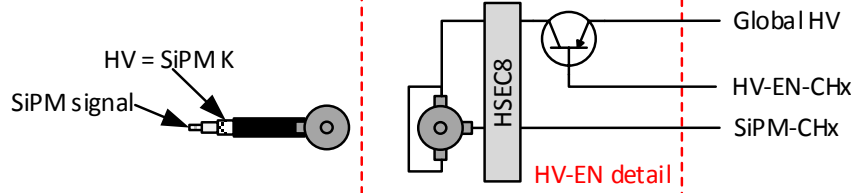
Vertical channels :	576-ch,	6 FEBs,	6 FEBs/MCR,	1 MCR/PC,	1 PC	<b>Total :</b>
Horizontal channels :	3456-ch,	36 FEBs,	6 FEBs/MCR,	3 MCR/PC,	2 PCs	7 MCR/42FEBs/3PCs



# SiPM – FEB Cabling : details – overall



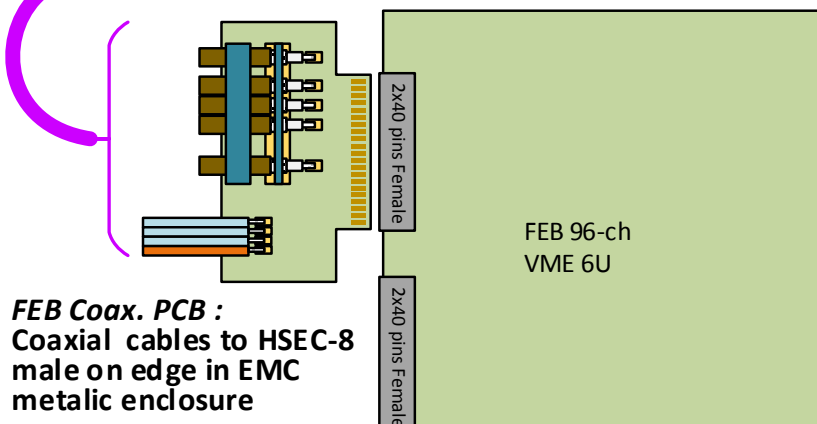
- All cables directly soldered on PCB pads
- Coaxial braid clamped to GND pad (EMC)
- Coaxial cable clamp to GND (mechanical)



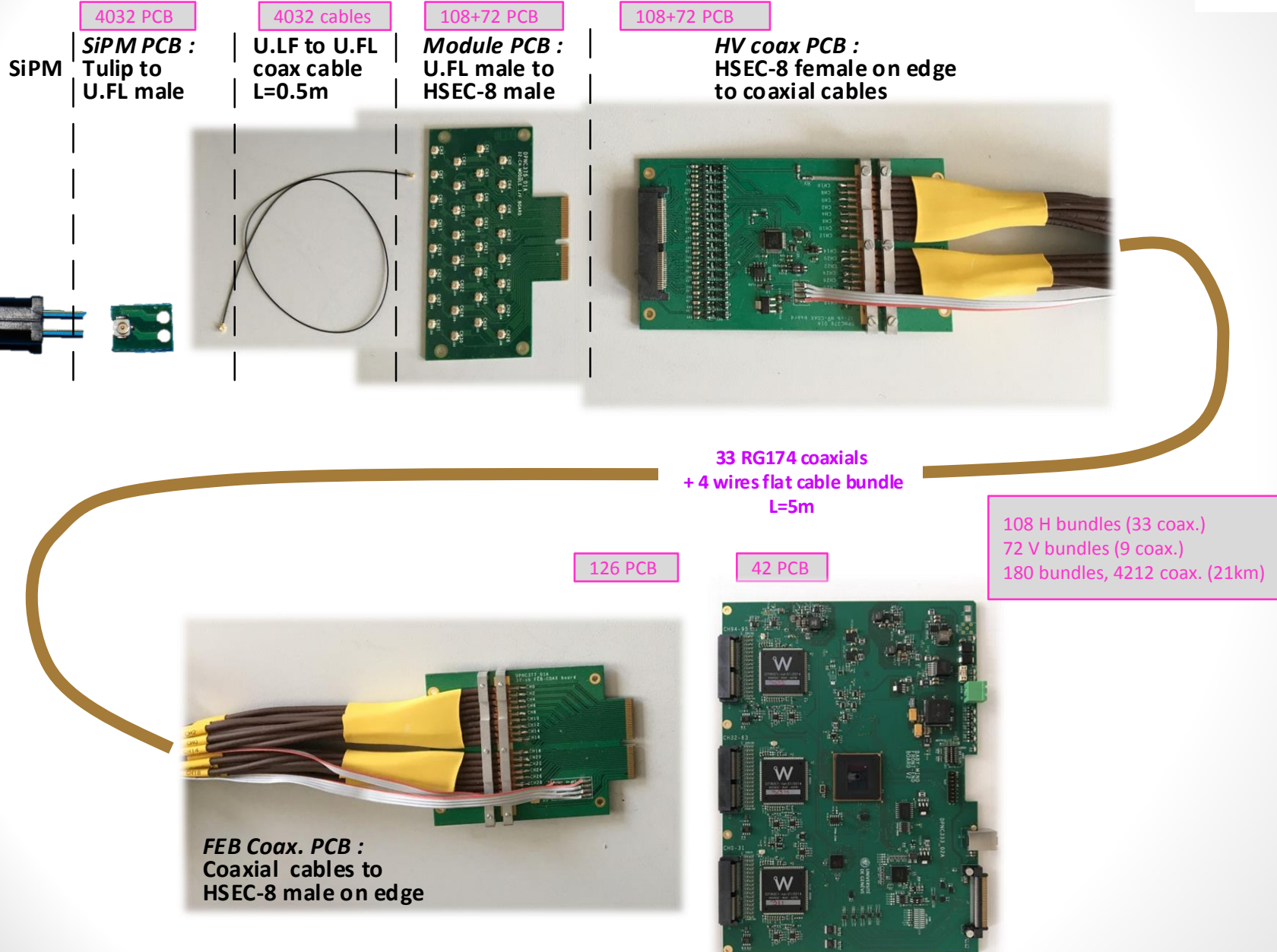
33 RG174 coaxials  
 + 4 wires flat cable bundle  
 L=5m

**SiPM PCB : 2 types**  
 Horizontal + Vertical

**Vertical bars:**  
 8-ch used/HV coax PCB =>  
 4 HV coax PCB +  
 4 bundles to 1 FEB 32-ch  
 coax PCB



# SiPM – FEB Cabling : boards view

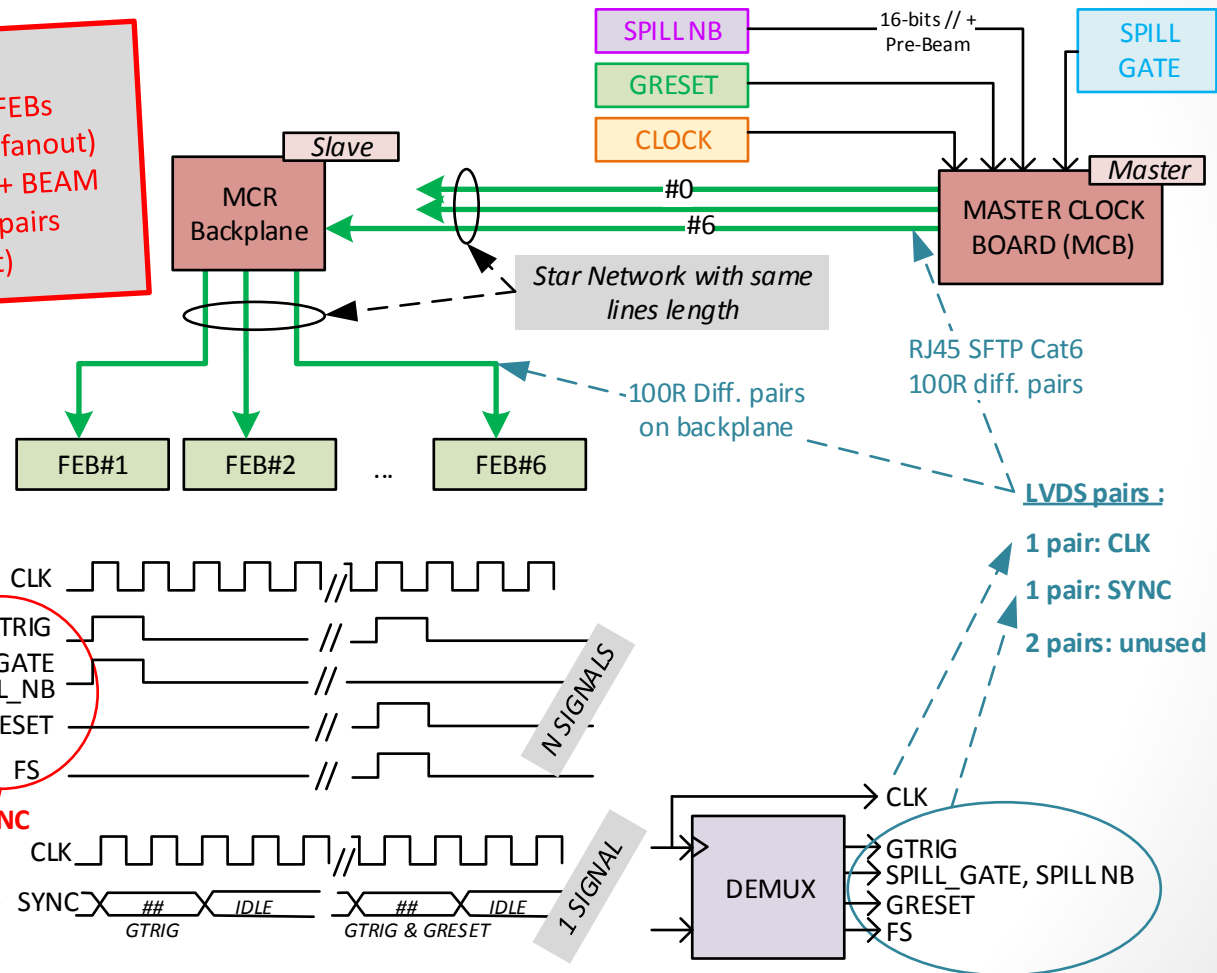


# Master Clock Board Synchronisation

- 100MHz CLK synchronizes exactly all FEBs
- 100KHz GTRIG allows a tagging of all timing event (10.24us counter overflow)
- 10KHz Frame Sync (FS) allows Time Divided Multiplexed (TDM) readout synchronization of the FEBs chain

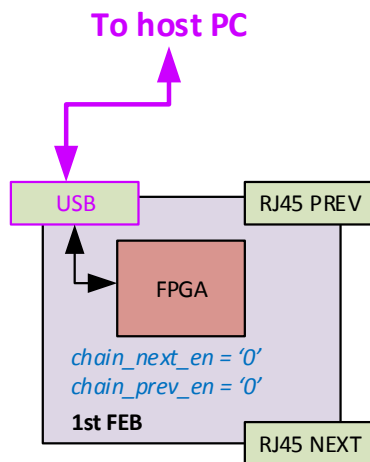
## Baby-mind architecture :

- Backplane propagates over all MCR FEBs CLK+SYNC+SPILL signals (1 to 6 star fanout)
- MCB shapes SPILL + RESET + CLOCK + BEAM TRIG and propagates signals over 4-pairs RJ45 LVDS signals (1 to 6 star fanout)

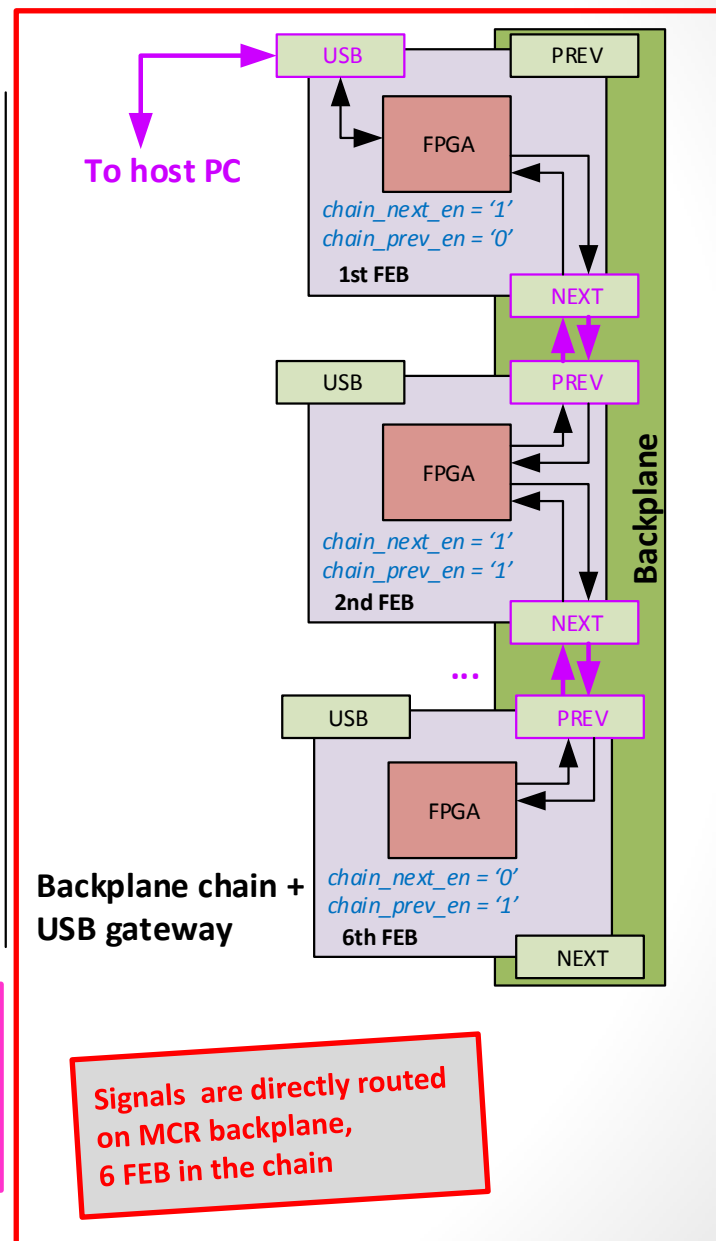


GTRIG is sent synchronously with CLK  
 SPILL\_GATE/NB, GRESET & FS are sent by MCB synchronously with GTRIG

# FEB chain cabling options



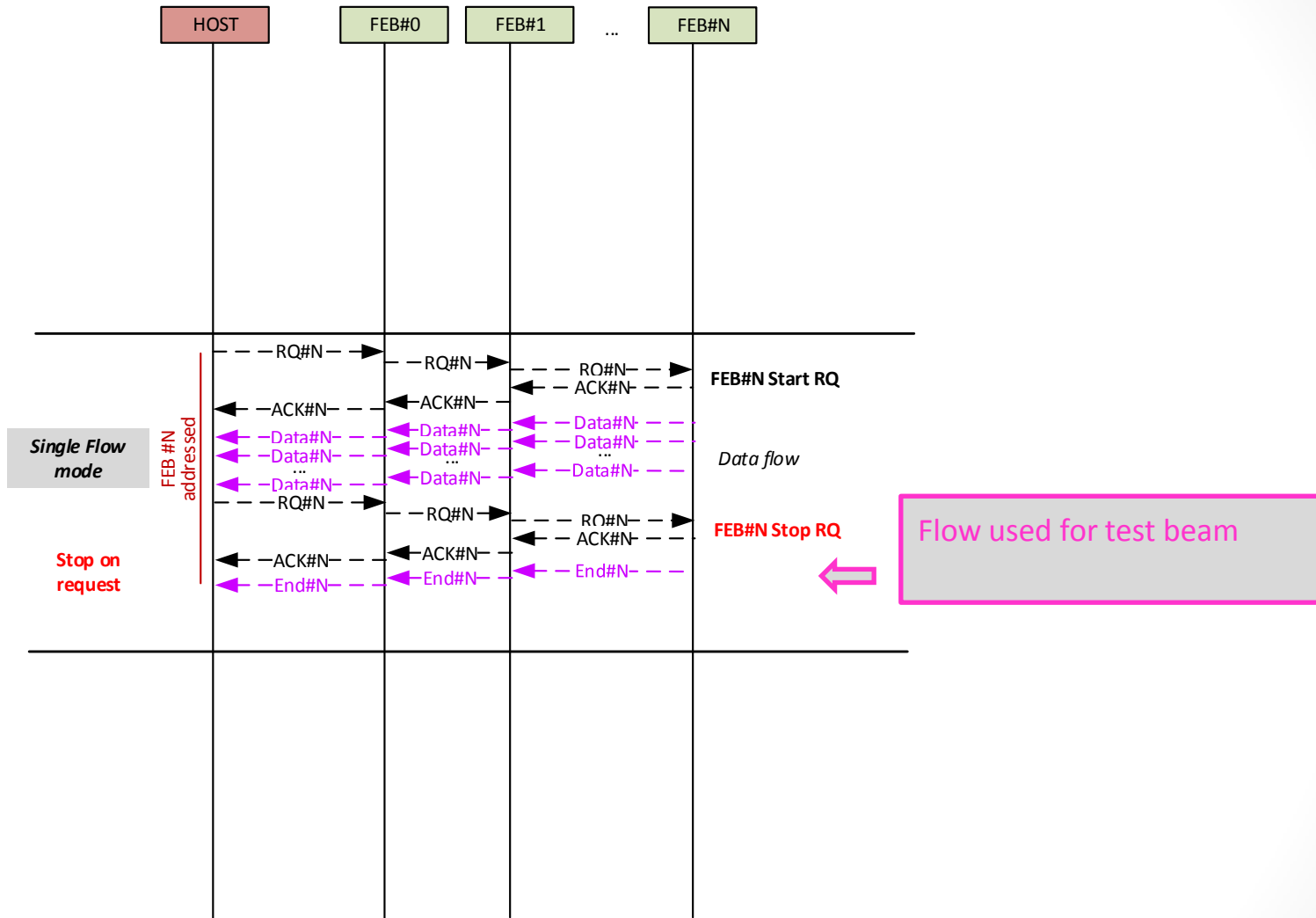
USB standalone (lab, maintenance, calibration)



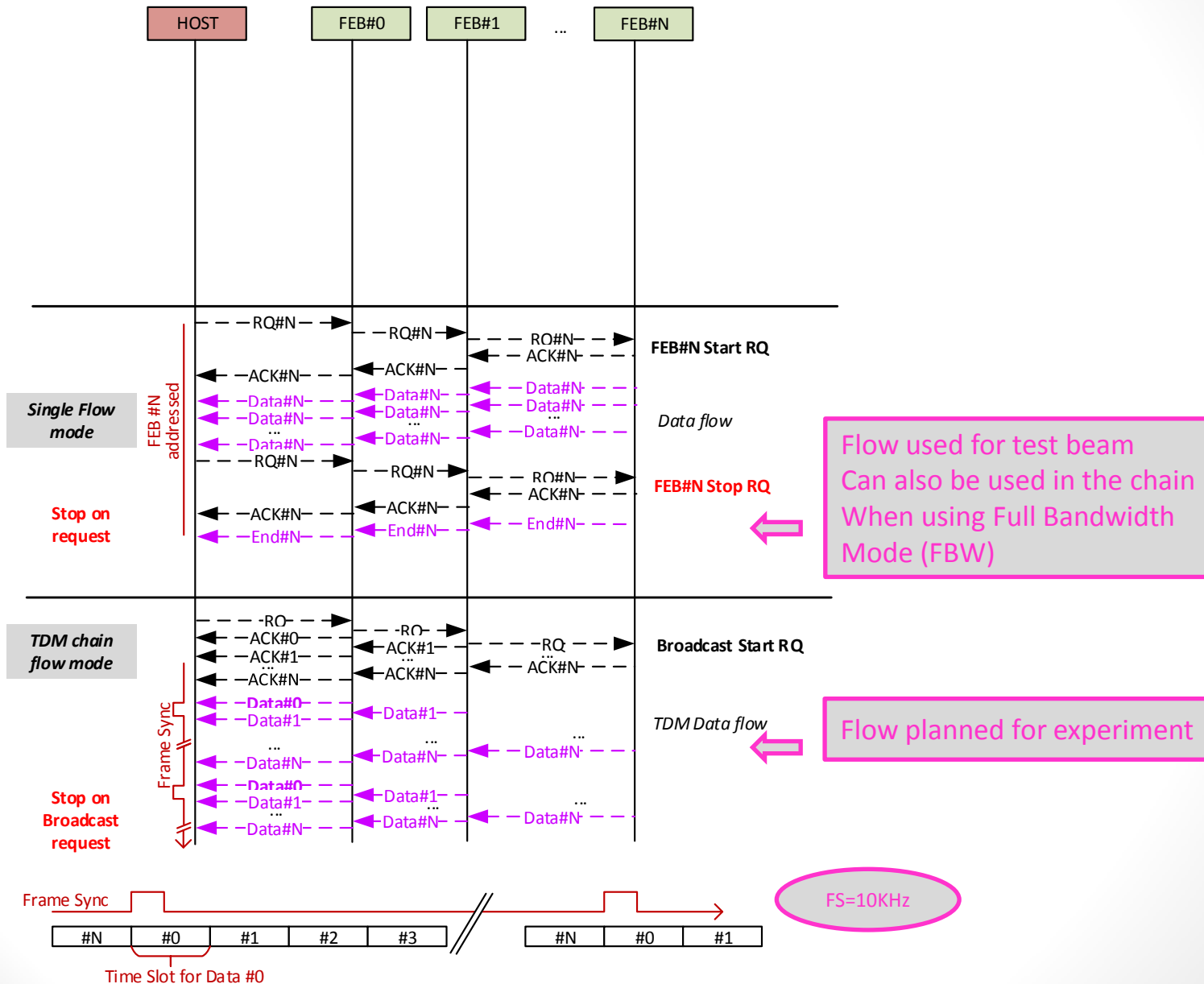
Signals are directly routed on MCR backplane, 6 FEB in the chain

FEB Chain signals :	PREV	flow	NEXT
Protocol command	CMDIN/CTS	=>	CMDOUT/RTS
Protocol answer	ANSOUT/RTS	<=	ANSIN/CTS
Data readout	DOUT	<=	DIN

# Data readout protocol modes – single flow



# Data readout protocol modes – TDM chain flow



# Data readout protocol details with TDM chain flow

## Time Slot Start

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDM ID				ID=0		Slot ID						TDM TAG																			

TDM beacon

## Spill header

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Spill header ID				Board ID								0		SId		Spill tag (from reset request)															
Spill time ID				Spill time on spill start (10ms resolution, max=745.6 h=31 days)																											

## GTRIG header #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTRIG header ID				Global Trigger tag (from reset request)																											

## Event Data : Hit #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit time ID				Channel ID								Hit ID		Tag ID		EDGE		Hit time (2.5ns res.)													

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit Amplitude ID				Channel ID								Hit ID		Tag ID		Amplitude ID		Amplitude measurement													

## Event Data : Hit #n

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit time ID				Channel ID								Hit ID		Tag ID		EDGE		Hit time (2.5ns res.)													

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit amplitude ID				Channel ID								Hit ID		Tag ID		Amplitude ID		Amplitude measurement													

Single board Data

## GTRIG trailer #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTRIG trailer 1 ID				Global Trigger tag (from reset request)																											
GTRIG trailer 2 ID				Hit counts within gtrig*		Global Trigger time (10us res. % current spill start, max=10.5s)																									

## Spill trailer

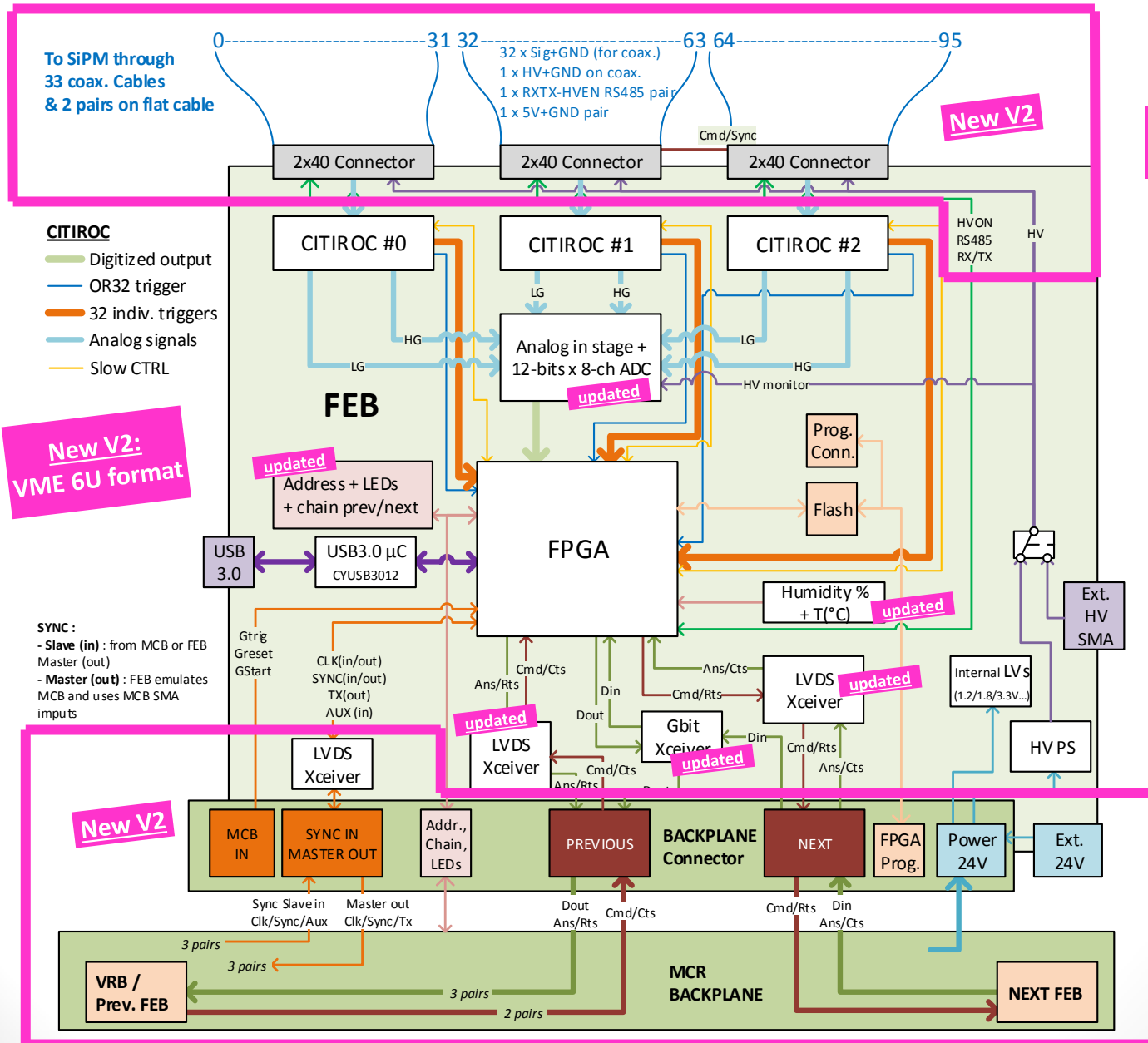
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Spill trailer ID				Board ID								0		SId		Spill tag (from reset request)															
Spill trailer ID				Board ID								1		SId		Temperature								Humidity							
Spill time ID				Spill time on spill end (10ms resolution, max=745.6 h=31 days)																											

## Time Slot End

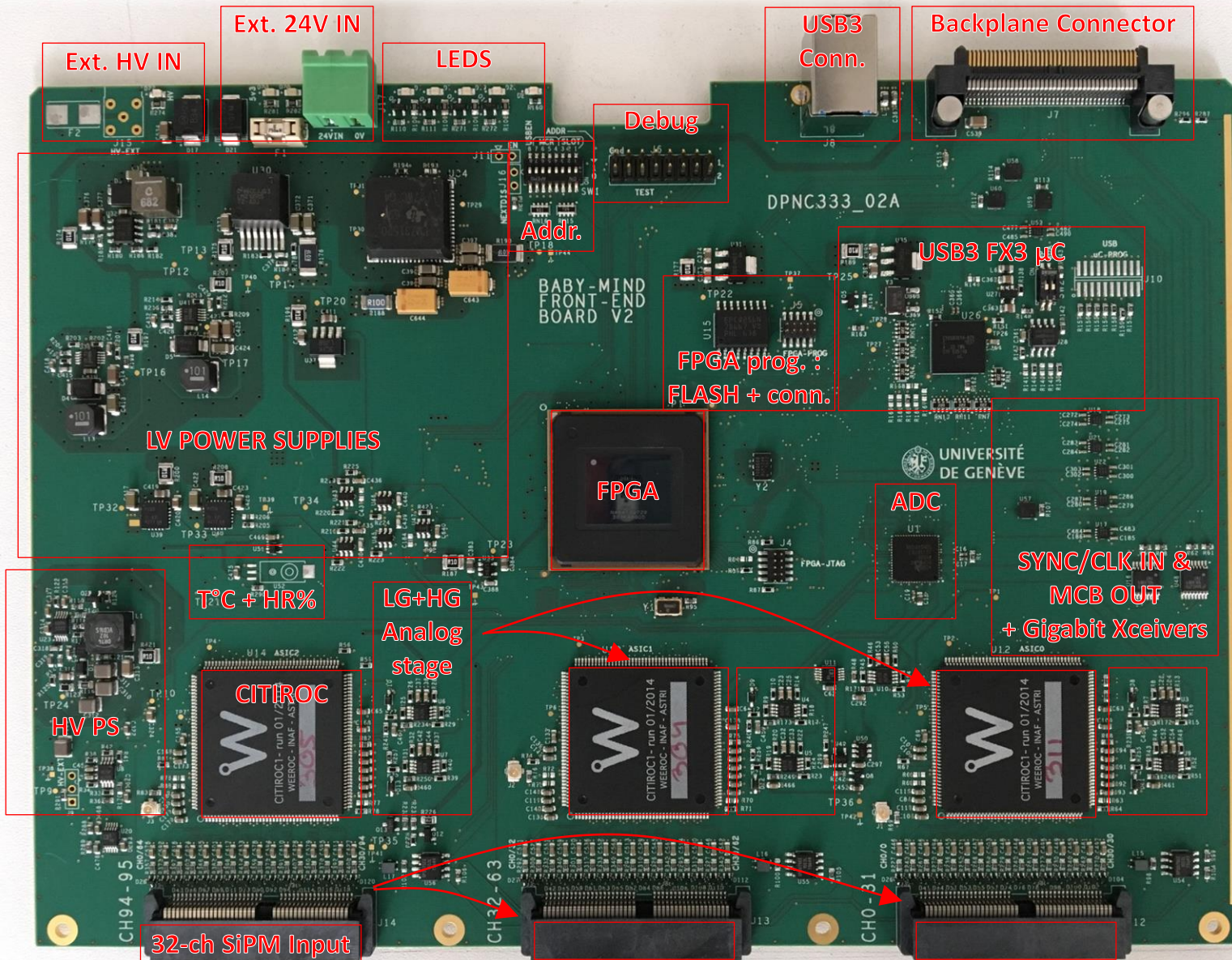
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDM ID				ID=1		Slot ID						21-bits CHECKSUM																			

TDM beacon

# FEB v2 hardware: Bloc diagram

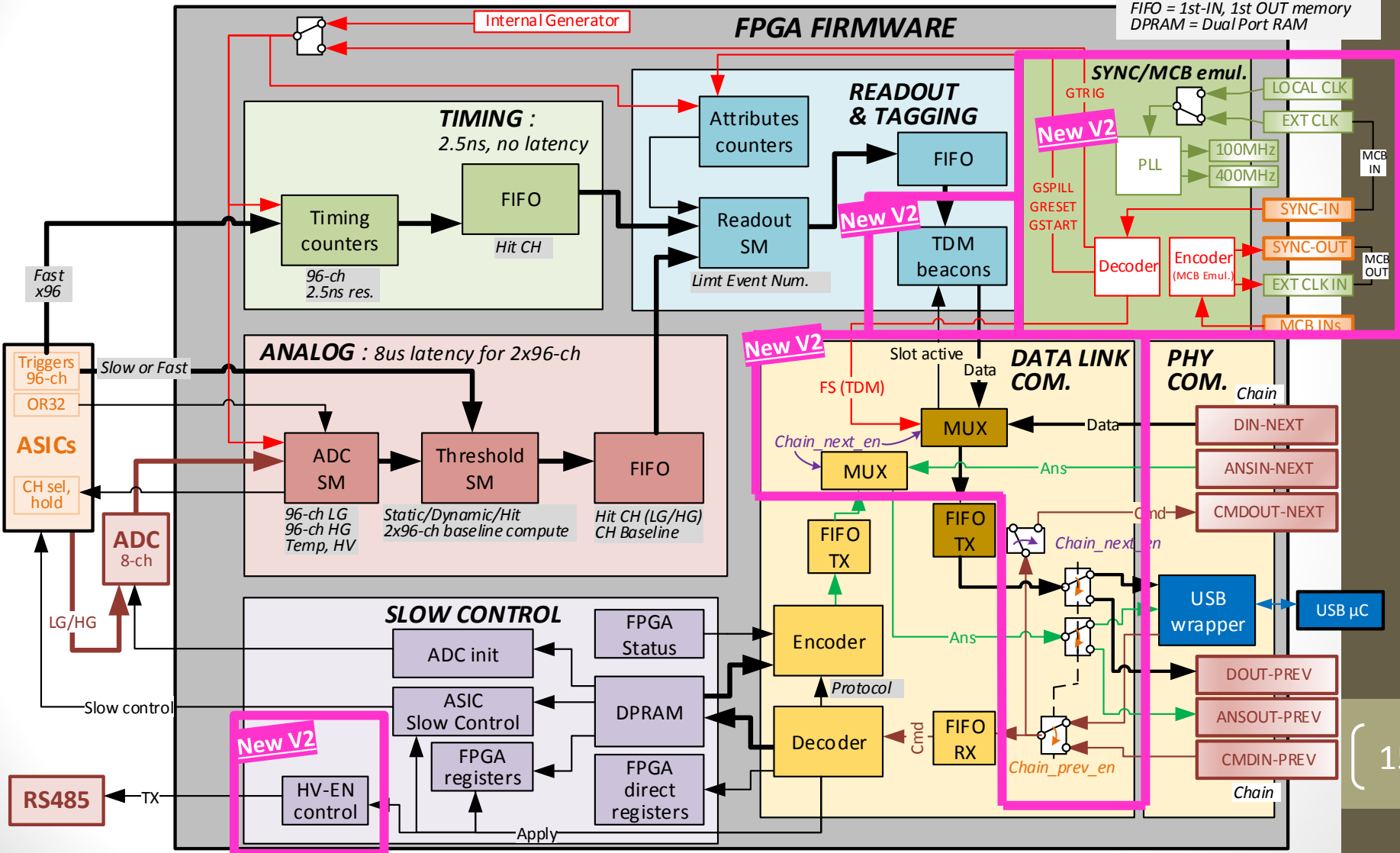


# FEB v2 hardware: board view

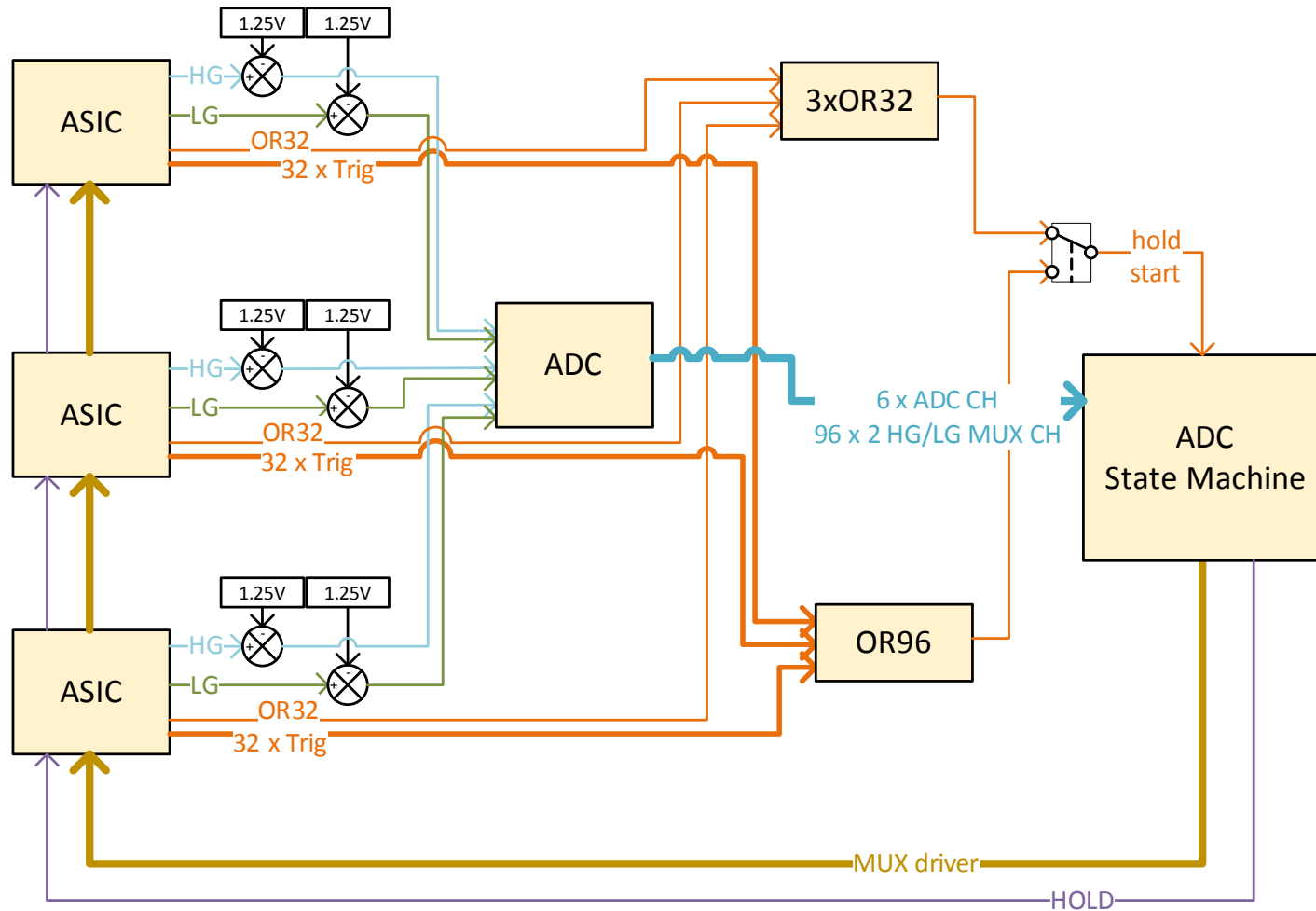


# FEB FPGA firmware overview

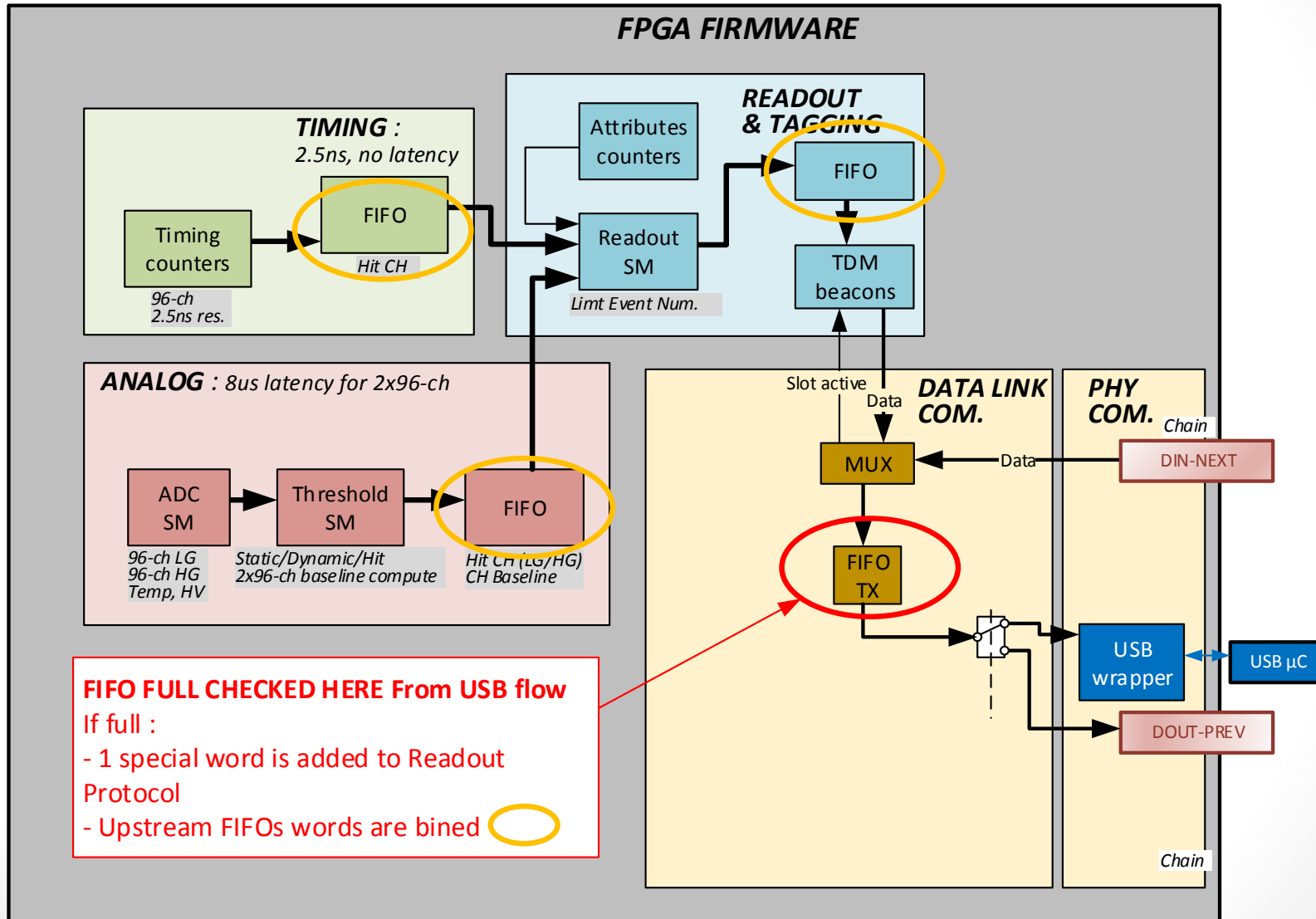
SM = state machine  
FIFO = 1st-IN, 1st OUT memory  
DPRAM = Dual Port RAM



# FEB v2 details: ADC Signal chain



# FEB v2 details: FIFO Full



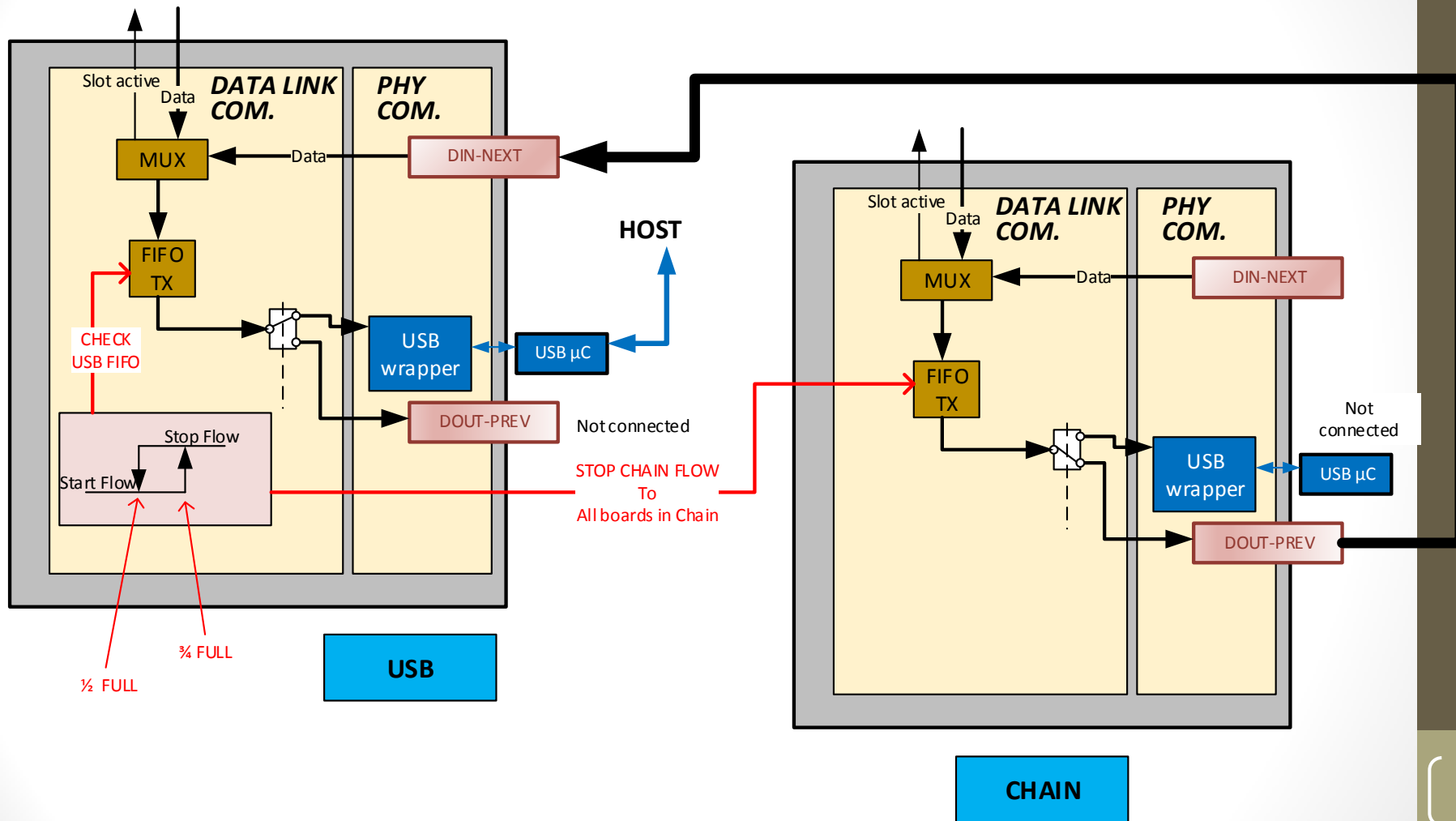
**FIFO FULL CHECKED HERE From USB flow**

If full :

- 1 special word is added to Readout Protocol

- Upstream FIFOs words are binned

# FEB v2 details: TDM flow stop



# Pricing

Description	Qty	Unit Price (€)	Total (€)
Mini PCB SiPM Horizontal / 1-CH	2500	2.78	6953
PCB	2700		891
Components	2500		1892
Assembly	2500		4170
			
Mini PCB SiPM Vertical / 1-CH	800	3.54	2835
PCB	1000		378
Components	800		605
Assembly	800		1852
			
Module PCB Horizontal 32-CH	135	31.86 (0.99€/CH)	2835
PCB	158		948
Components	135		2299
Assembly	135		1055
			
Module PCB Vertical 8-CH	92	14.16 (1.77€/CH)	1303
PCB	92		552
Components	92		391
Assembly	92		360
			
Coaxial cables for bundles (L=5m/ch)	28km	0.082/m (0.41€/CH)	2344
			
Mini-Coaxial cables (U.FL, L=0.5m/ch)	5000	0.90	4519
			






Does not include mechanical parts (e.g. spacers) nor EMC housing

**Warning : pricing for listed quantities, ordering 1/few part(s) will not have the same price !**

# Pricing

19.74€/CH Horizontal

23.43€/CH Vertical

Description	Qty	Unit Price (€)	Total (€)
HVON PCB Horizontal 32-CH	134	33.56 (1.05€/CH)	4497
 PCB Components Assembly	158		842
	134		2681
	134		974
HVON PCB Horizontal 8-CH	92	25.75 (3.2€/CH)	2369
 PCB Components Assembly	92		490
	92		1159
	92		720
FEB Coax PCB (same for 8 & 32-CH)	180	6.27 (0.2€/CH)	1129
 PCB			1129
FEB v2 (without ASIC price)	57	906.7 (9.4€/CH)	51680
 PCB Non supplier components Assembly + supplier comp. Tooling (once) 1 batch starting cost	57		3638
	57		27207
	57		18004
	1		1866
	1		965
CITIROC ASIC	181	128.44 (4.01€/ch)	23248
			

Does not include mechanical parts (e.g. spacers) nor EMC housing

**Warning : pricing for listed quantities, ordering 1/few part(s) will not have the same price !**

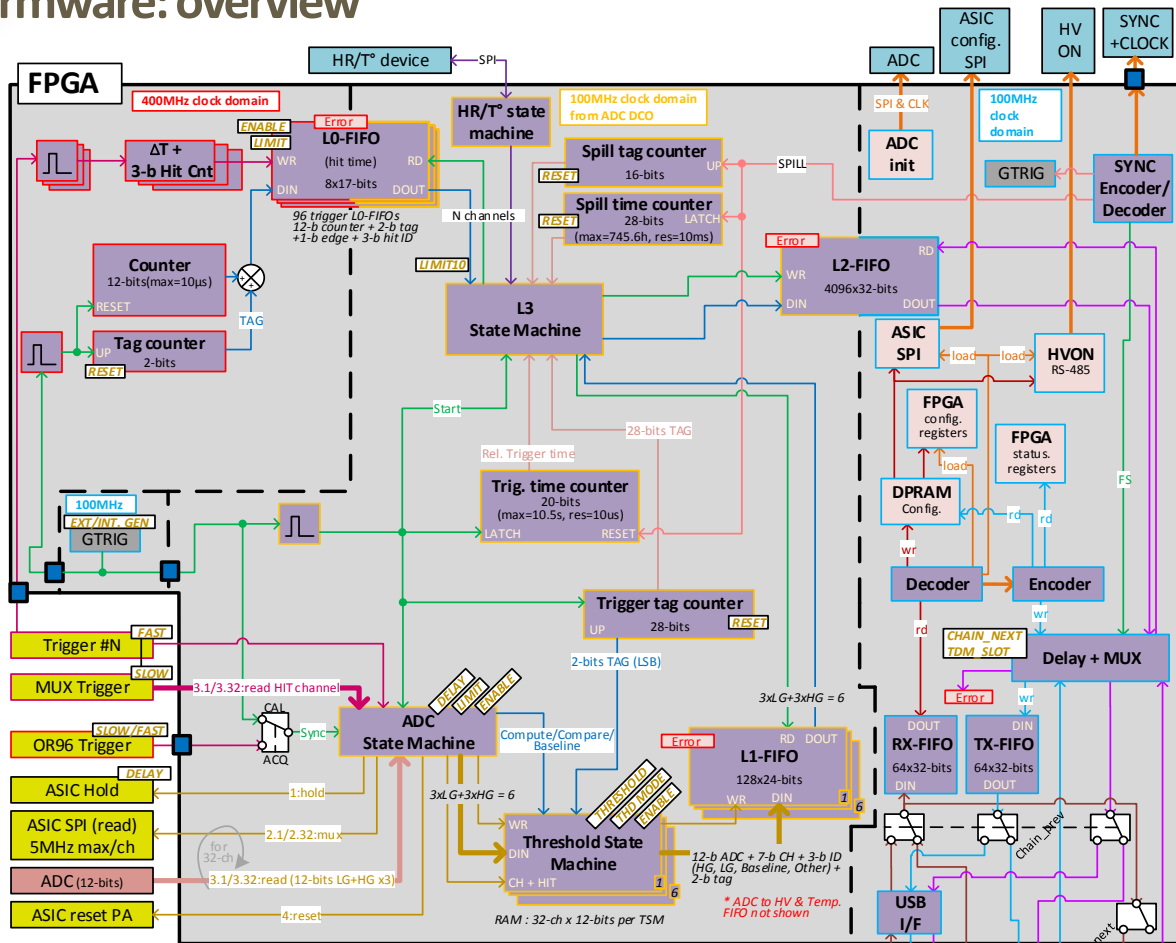


**Thanks for you attention**  
**Questions ...**



# Backup Slides

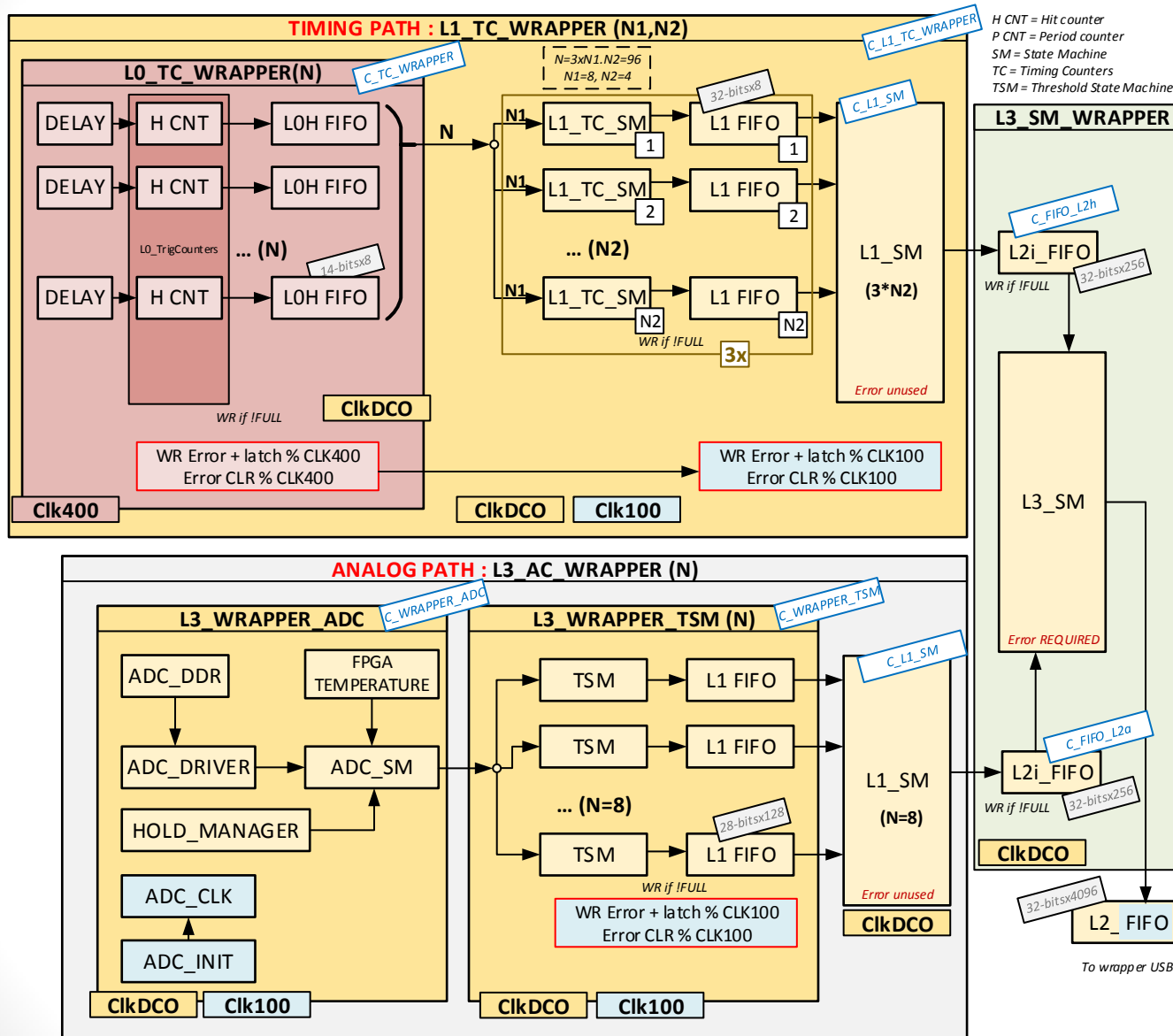
# FPGA firmware: overview



- ENABLE** - channel enable from slow control parameter
  - LIMIT** - Limit the nb of event at 1 per global trigger period from slow control parameter
  - RESET** - Reset register (tag counter, time counter) from slow control command
  - THD MODE** - Threshold computation mode (STATIC, DYNAMIC, HIT)
  - THRESHOLD** - Threshold used to filter ADC values in STATIC THD MODE
  - LIMIT10** - only 10 ADC hits and 10 time hits are pushed into the L2-FIFO
  - SLOW/FAST** - selection between slow or fast ASIC trigger line
  - DELAY** - delay may be applied in order to delay signal assertion after synchronization input signal
- 2-FF synchronizer (metastability removing)

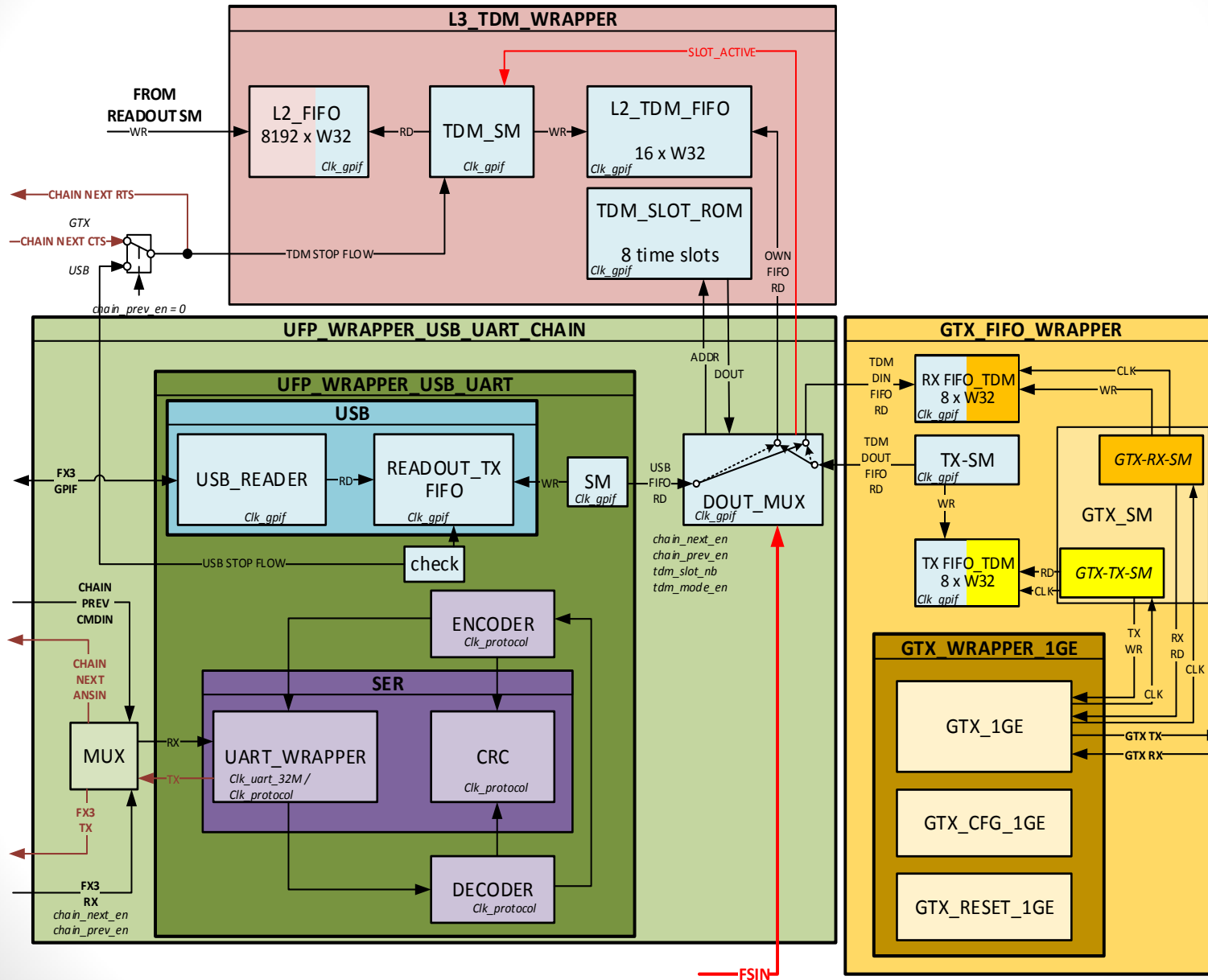
- |   |   |
|---|---|
| <b>ADC State Machine</b> <ul style="list-style-type: none"> <li>- manage ASIC 'Hold' delay % sync</li> <li>- read consecutively multiplexed 32 channels &amp; slow trigger with ASIC MUX output management or fast trigger directly from latch register</li> <li>- manage ASIC 'reset_PA'</li> <li>- push ADC samples Threshold state machine with compute or compare signal</li> </ul>   | <b>L1-FIFO</b> <ul style="list-style-type: none"> <li>- when 3-b ID = 'other' then 7-b CH word is as 2nd ID for:                             <ul style="list-style-type: none"> <li>- DAC value of ASIC#0, #1 or #2</li> <li>- TEMP value of ASIC#0, #1 or #2</li> <li>- HV measure</li> </ul> </li> <li>- when 3-b ID = 'Baseline' then the channel baseline is pushed sequentially to L1-FIFO in order to save bandwidth i.e. a complete baseline cycle is done every 84-ch x trigger period</li> </ul> |
| <b>L3 &amp; L1 State Machine</b> <ul style="list-style-type: none"> <li>- push spill header into L2-FIFO (spill tag, board ID)</li> <li>- push event header into L2-FIFO (trigger tag)</li> <li>- push event data of identical 2-bits LSB trigger TAG into L2-FIFO:                             <ul style="list-style-type: none"> <li>- L0-FIFO trigger (hit time)</li> <li>- L1-FIFO (amplitude)</li> </ul> </li> <li>- push event trailer into L2-FIFO (trigger tag, trigger time, events nb)</li> <li>- push spill trailer into L2-FIFO (spill tag, board ID, HR/T*, spill time)</li> </ul> | <b>OR96 Trigger</b> <ul style="list-style-type: none"> <li>- equals to OR of the 3 OR32 ASICs</li> <li>- may be selected between OR32 (slow trig) or OR32t (fast trig)</li> </ul>   |
| <b>Global TRIG</b> <ul style="list-style-type: none"> <li>- may be generated by external trigger signal (all board synchronized) or internal pulse generator (standalone board)</li> <li>- may be delayed to compensate external cabling delay</li> </ul>   |   |

# FPGA firmware: timing & analog paths wrapping details

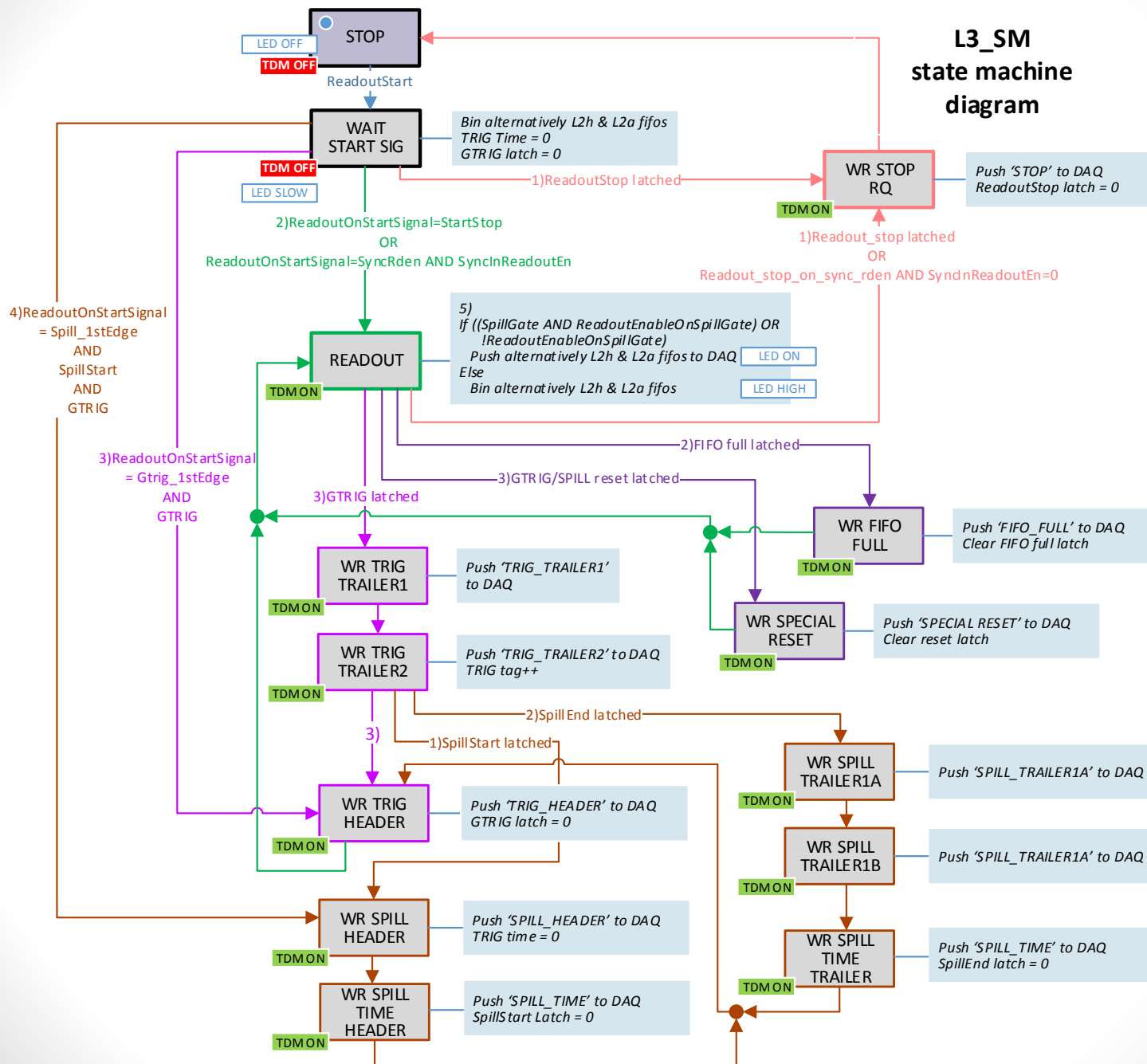


H CNT = Hit counter  
P CNT = Period counter  
SM = State Machine  
TC = Timing Counters  
TSM = Threshold State Machine

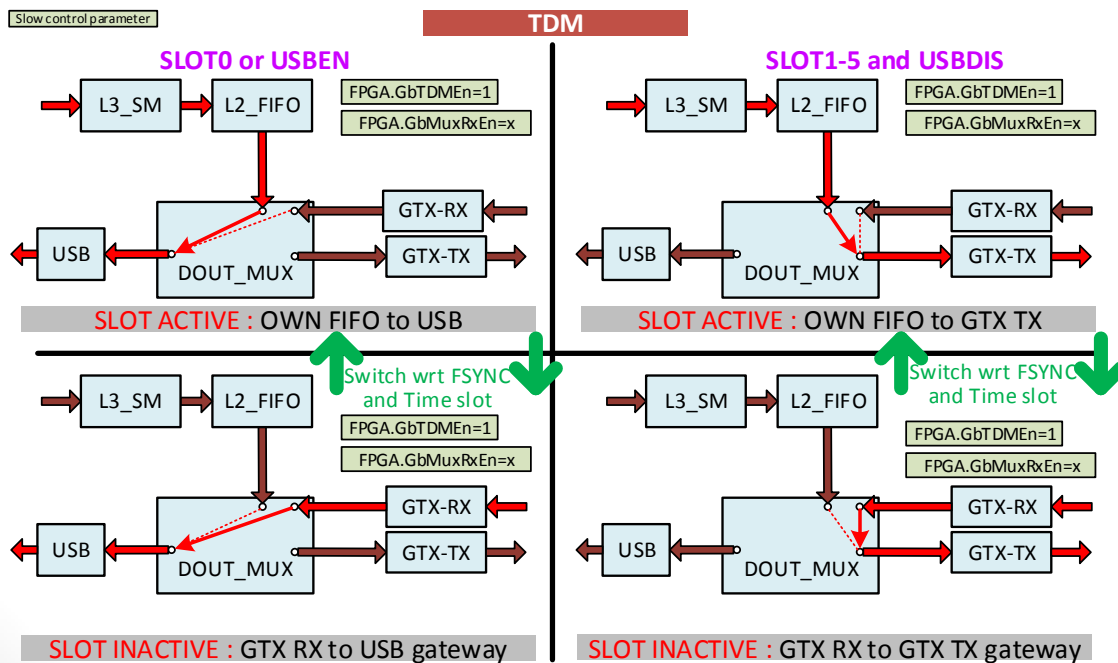
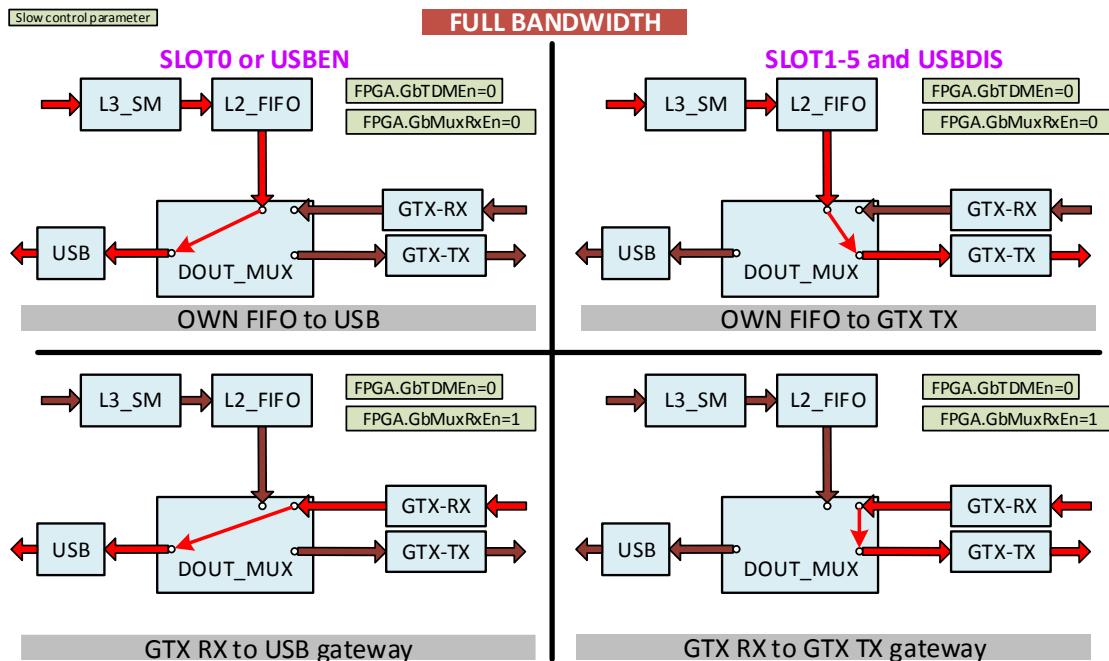
# FPGA firmware: readout wrapping details



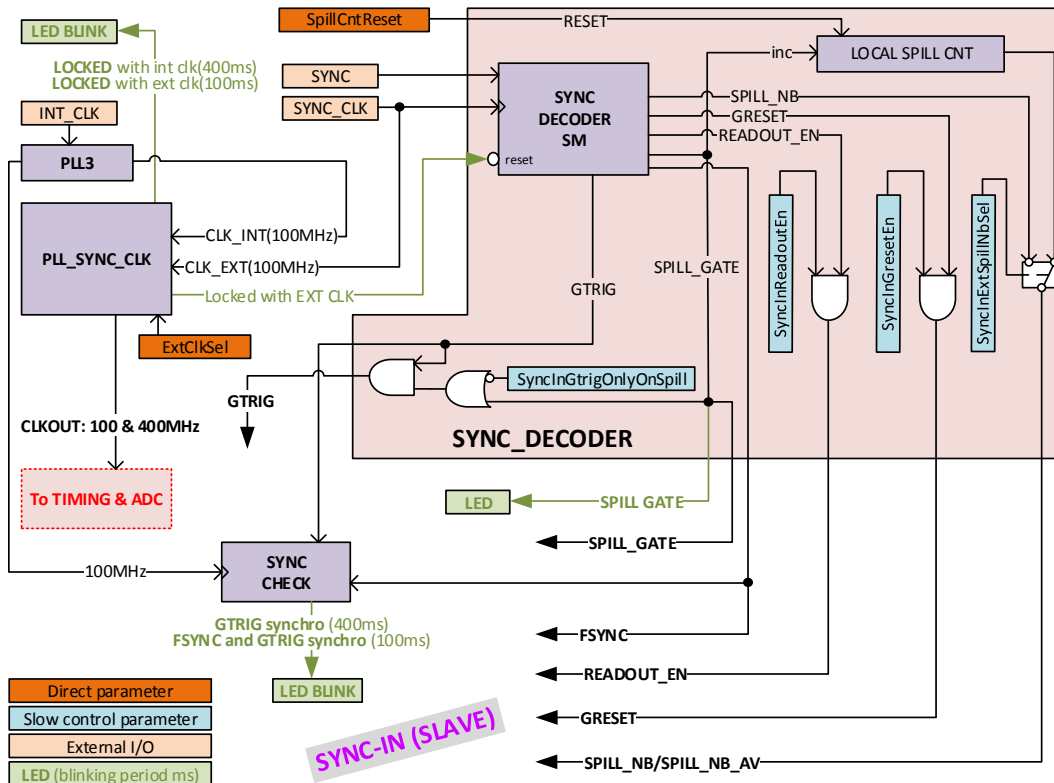
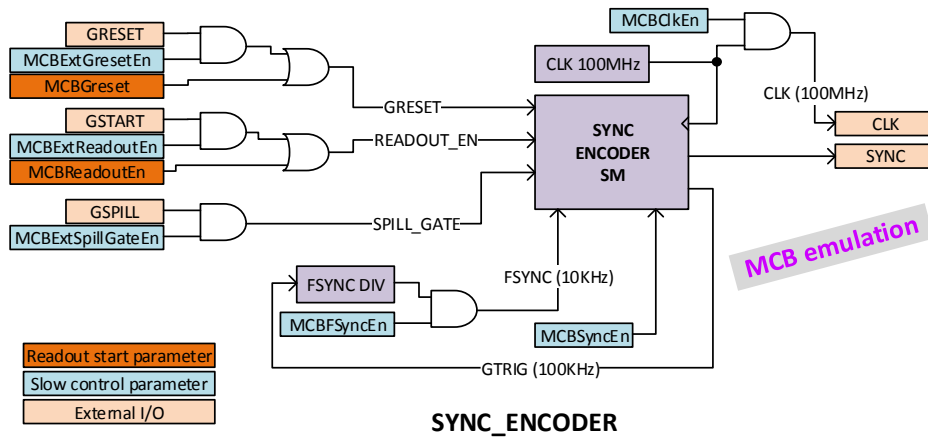
# FPGA firmware: L3 readout state machine



# FPGA firmware: TDM mode multiplexer overview



# FPGA firmware: SYNC encoder & decoder

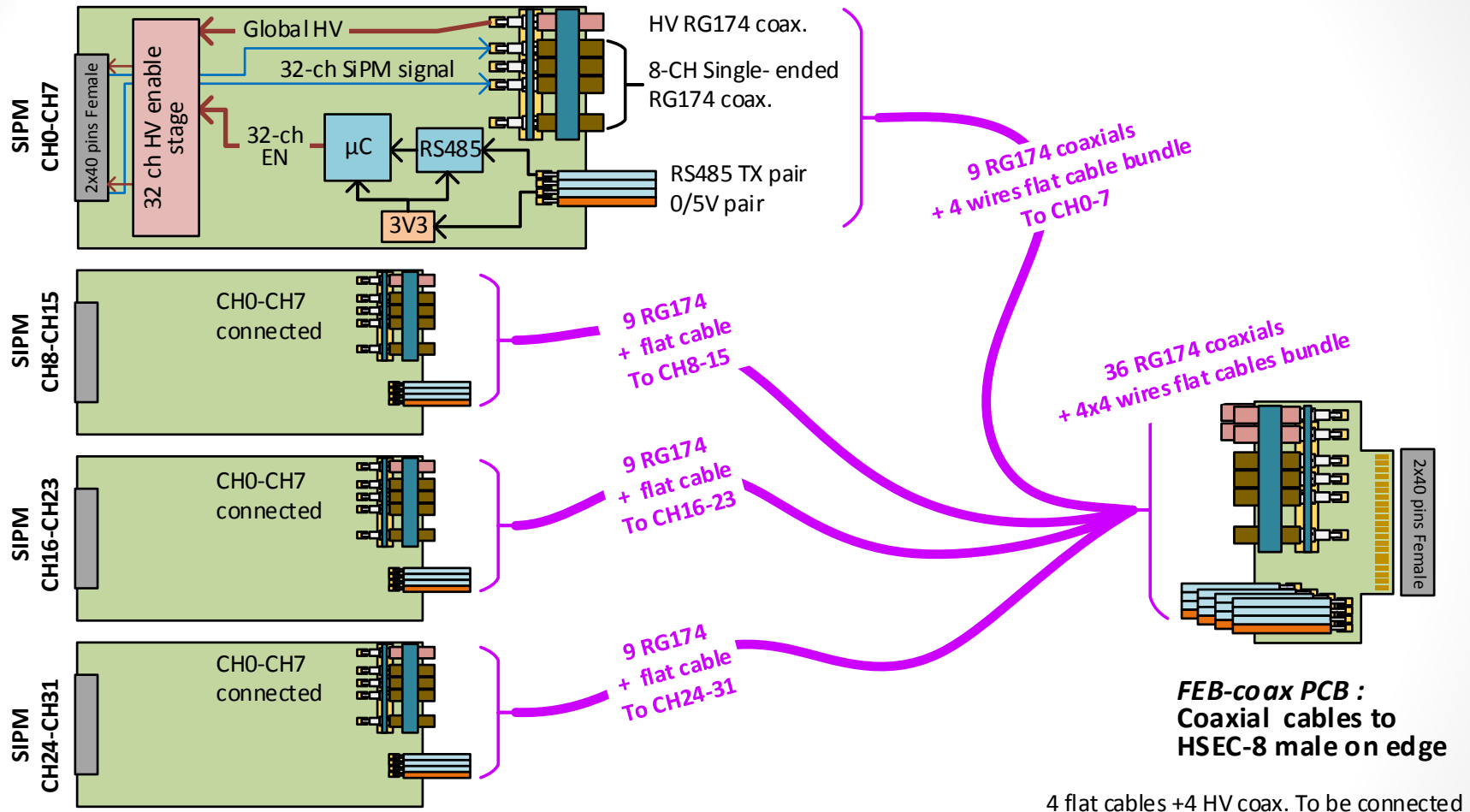


# Readout protocol: Special Word IDs

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>Readout End</b>																																
Special Word ID		Board ID										0	Special Word ID PARAM = 0x10000																			
<b>GTRIG RESET</b>																																
Special Word ID		Board ID										0	Special Word ID PARAM = 0x00001																			
<b>SPILL RESET</b>																																
Special Word ID		Board ID										0	Special Word ID PARAM = 0x00002																			
<b>GTRIG + SPILL RESET</b>																																
Special Word ID		Board ID										0	Special Word ID PARAM = 0x00003																			
<b>FIFO FULL</b>																																
Special Word ID		Board ID										0	Special Word ID PARAM = 0x00010																			
<b>LOST of GTX WORD INTEGRITY</b>																																
Special Word ID		0x00										Special Word ID PARAM = 0xF00FF																				

# Cabling: 8-ch SiPM to FEB cabling details for vertical bars

**4 x HV-coax PCB 8-channels:**  
HSEC-8 female on edge to coaxial cables



All HV-coax PCBs 8-ch are depopulated HV-coax PCBs 32-ch  
i.e. only 8 channels are mounted and used over 32 channels available