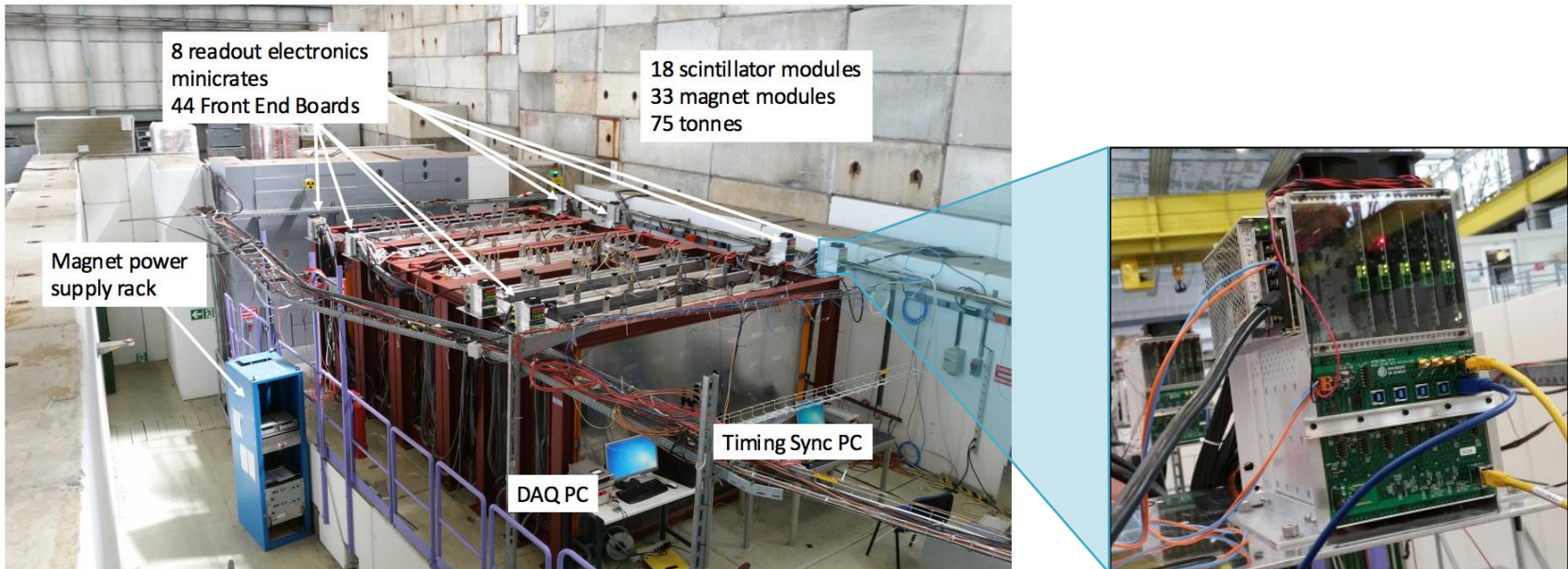


Baby MIND

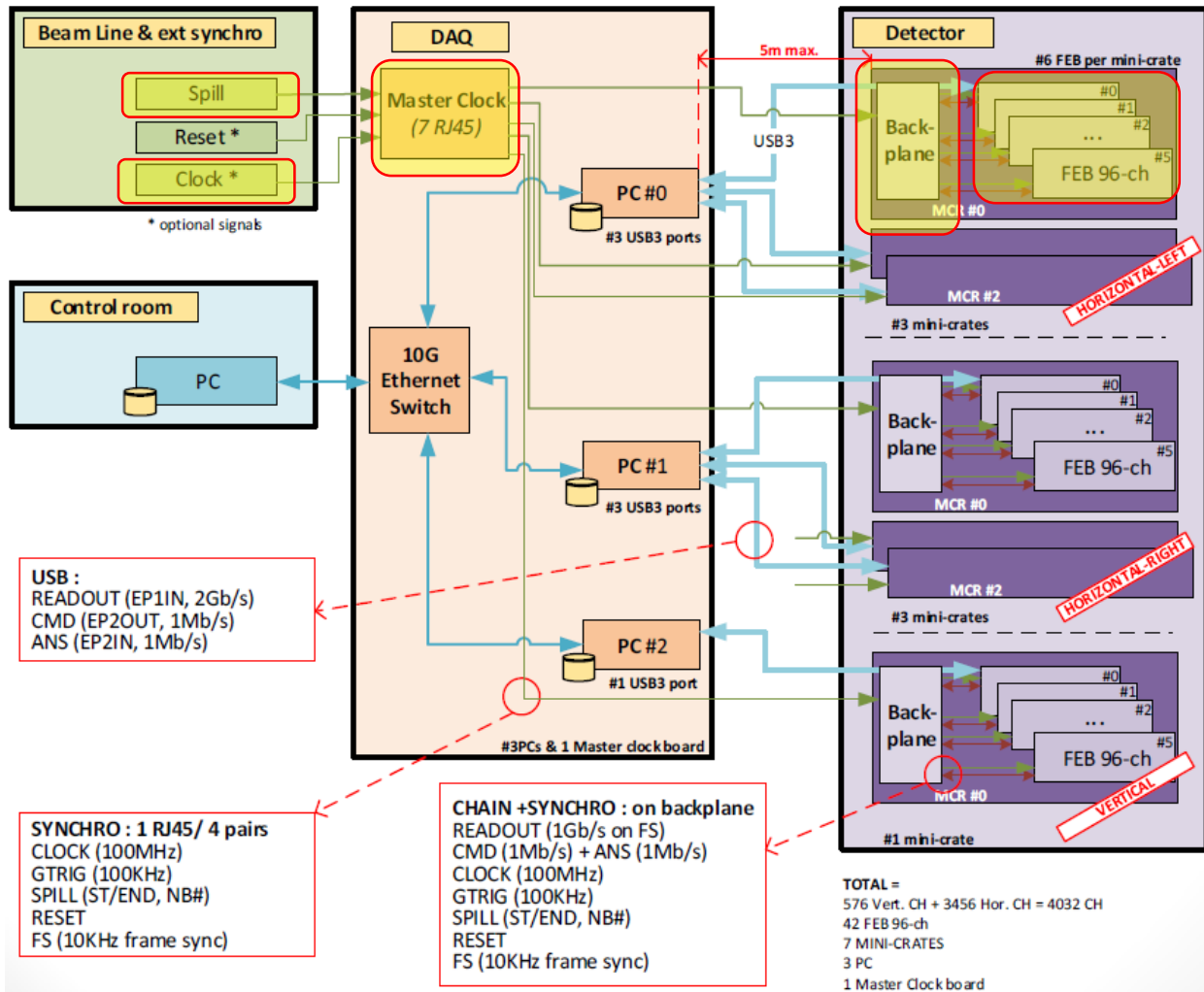
Synchronization at J-PARC

Georgi Mitev

Baby MIND



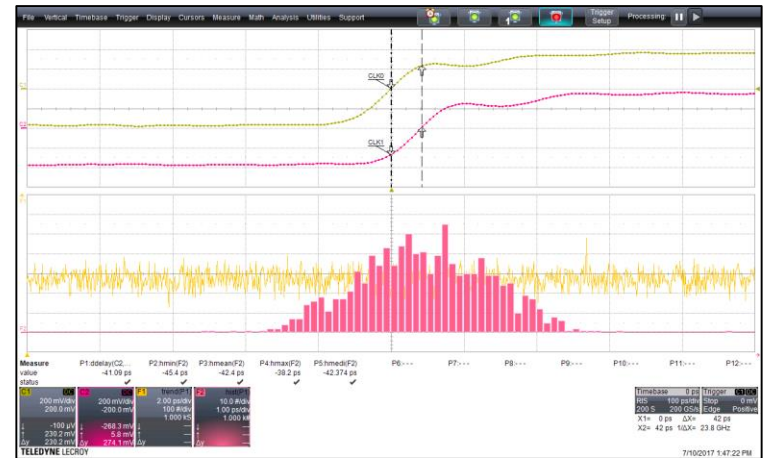
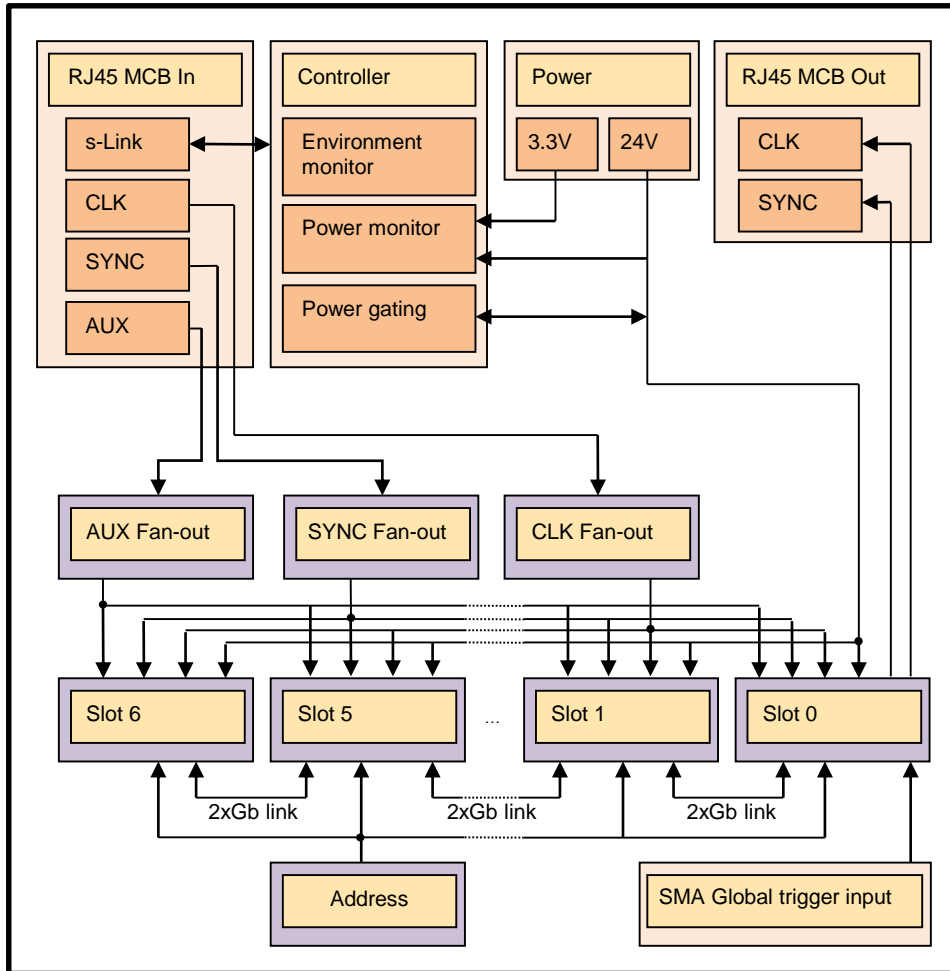
Baby MIND DAQ overview



FEB synchronization setup



Mini-crate Backplane



Clock delay difference

Delay Channel	min (ps)	max (ps)	median (ps)	max - min (ps)	delay (ps)
CLK_0-to-1	-3.4	3.8	-0.374	7.2	-0.374
CLK_0-to-2	4.5	10.4	7.45	5.9	7.45
CLK_0-to-3	10.2	16	12.96	5.8	12.96
CLK_0-to-4	6.4	12.4	9.494	6	9.494
CLK_0-to-5	2.1	7.9	4.647	5.8	4.647
CLK_0-to-6	-5.2	1.8	-1.979	7	-1.979

Mini-crate Backplane 2



IEEE Xplore paper:

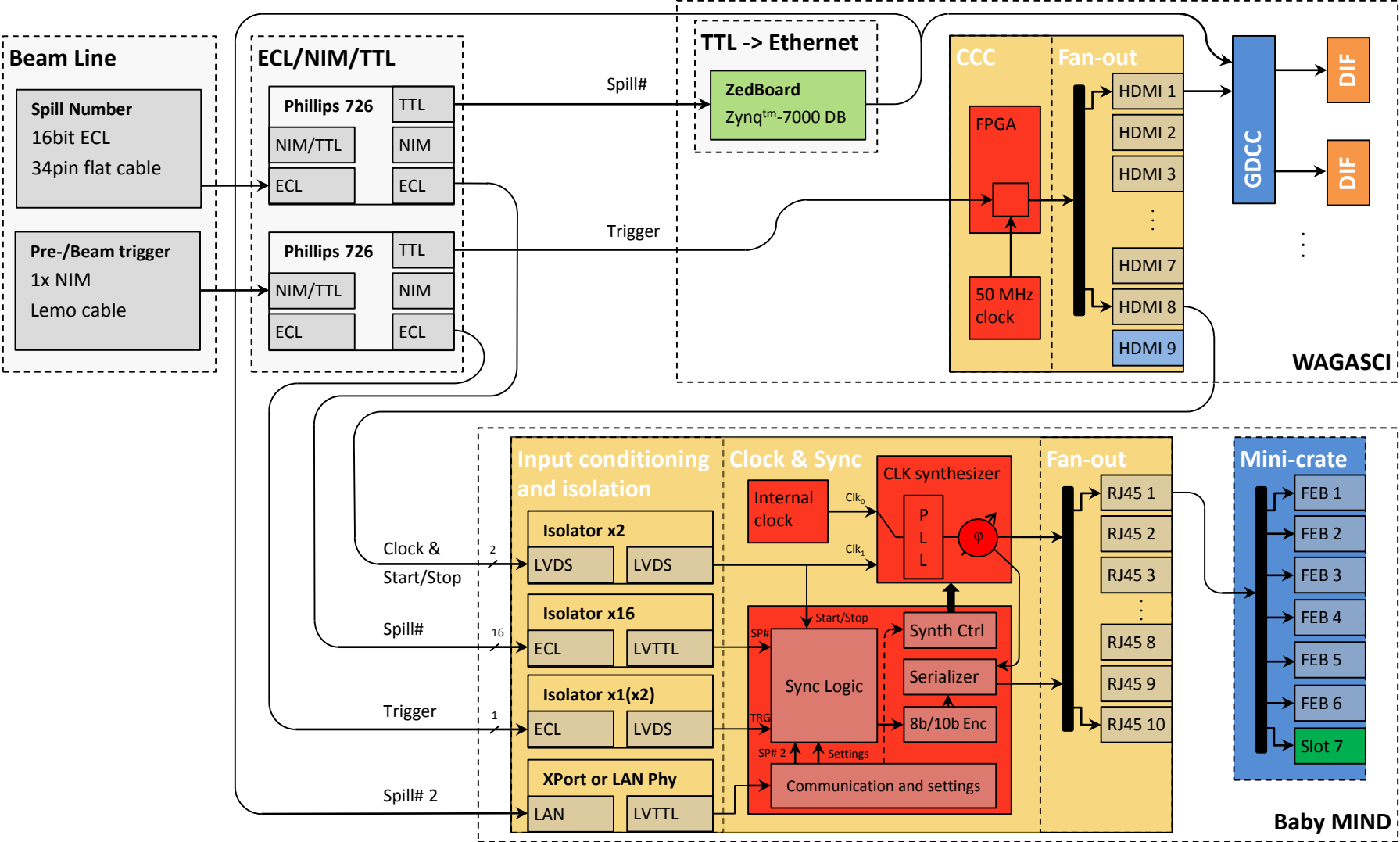
Synchronization of the distributed readout frontend electronics of the Baby MIND detector.

<http://ieeexplore.ieee.org/document/8124369/>

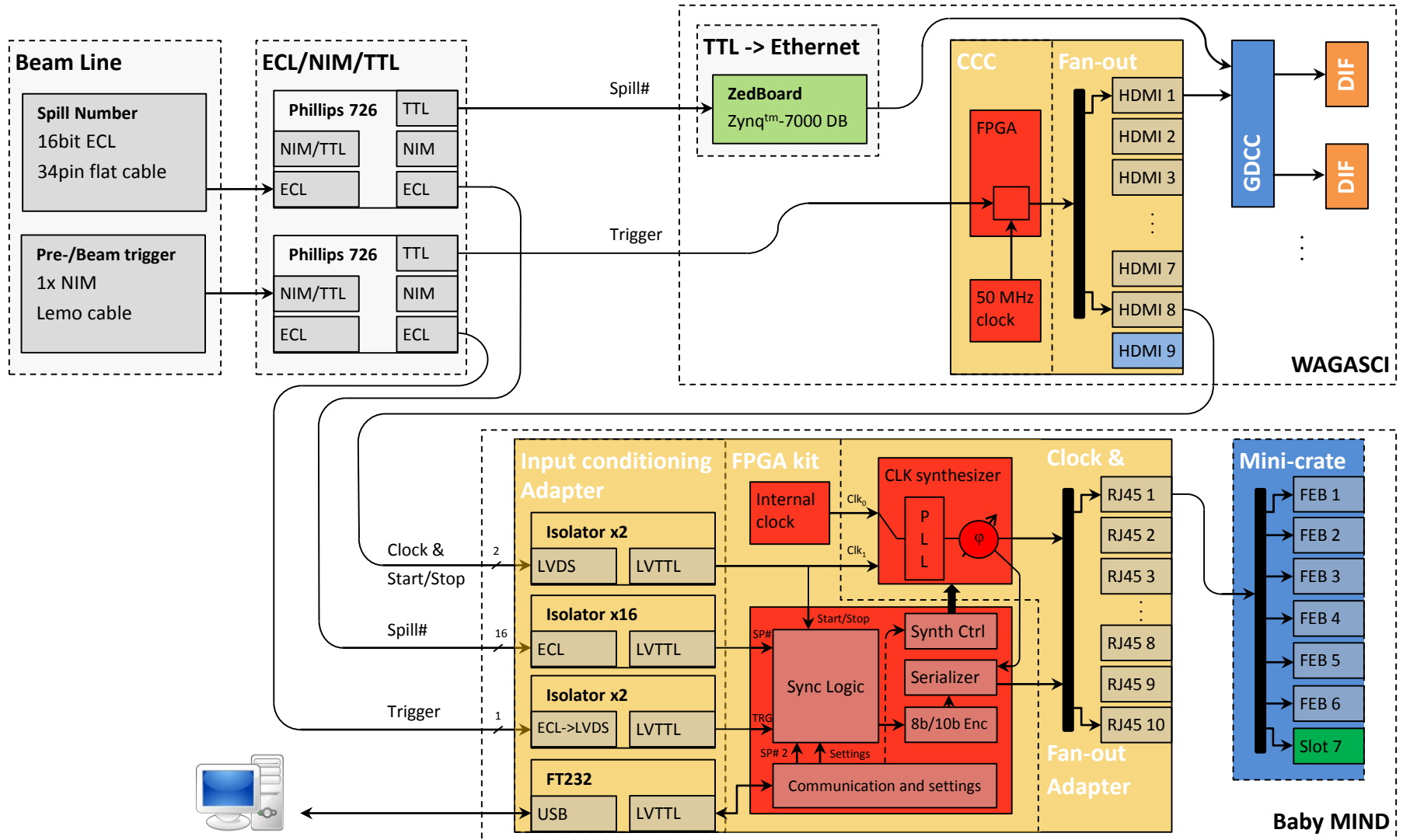
Clock to SYNC delay

Slot delay	min (ps)	max (ps)	median (ps)	max - min (ps)	delay (ps)
CLK-to-SYNC_Input	-1	41	20.66	42	20.66
CLK_0-to-SYNC_0	709.2	738.7	725.5	29.5	746.2
CLK_0-to-SYNC_1	715.2	737.2	725.3	22	745.9
CLK_0-to-SYNC_2	700	722.5	710.6	22.5	731.2
CLK_0-to-SYNC_3	709.4	733.4	720.2	24	740.9
CLK_0-to-SYNC_4	708.4	732.9	720.3	24.5	740.9
CLK_0-to-SYNC_5	699.2	724.2	711.2	25	731.9
CLK_0-to-SYNC_6	717.9	744.4	730.3	26.5	750.9

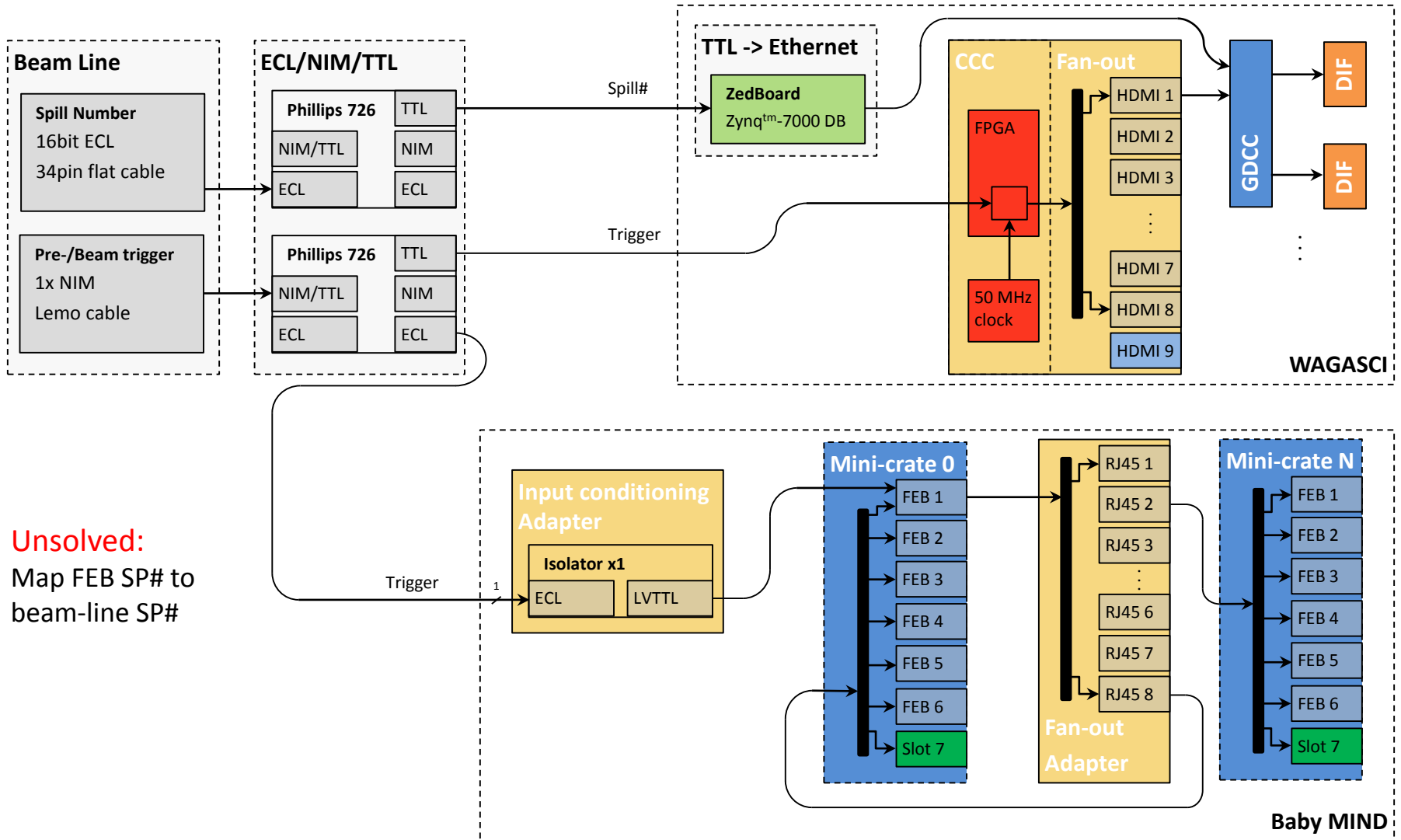
Baby MIND Synchronization chain



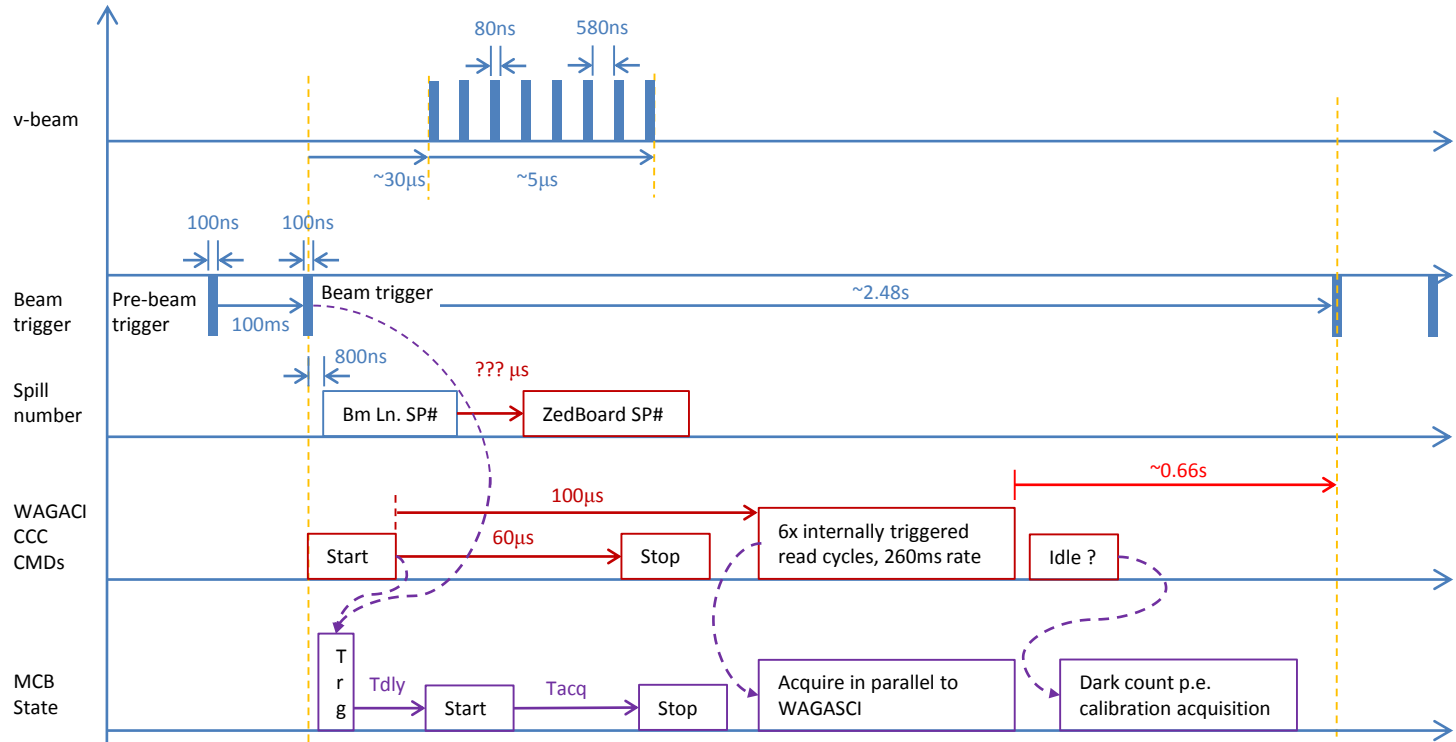
Baby MIND synchronization prototype



Baby MIND synchronization plan B



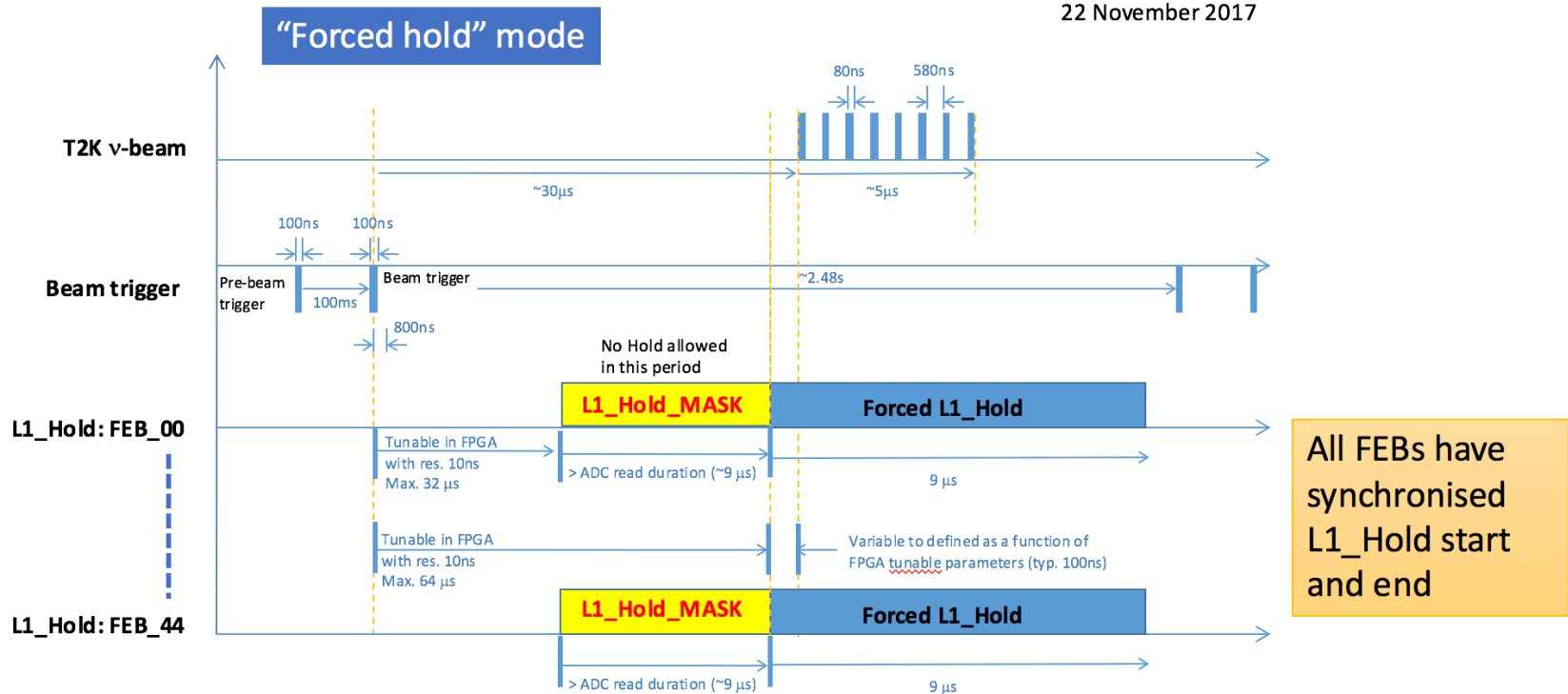
Baby MIND triggering



Baby MIND Hold scheme

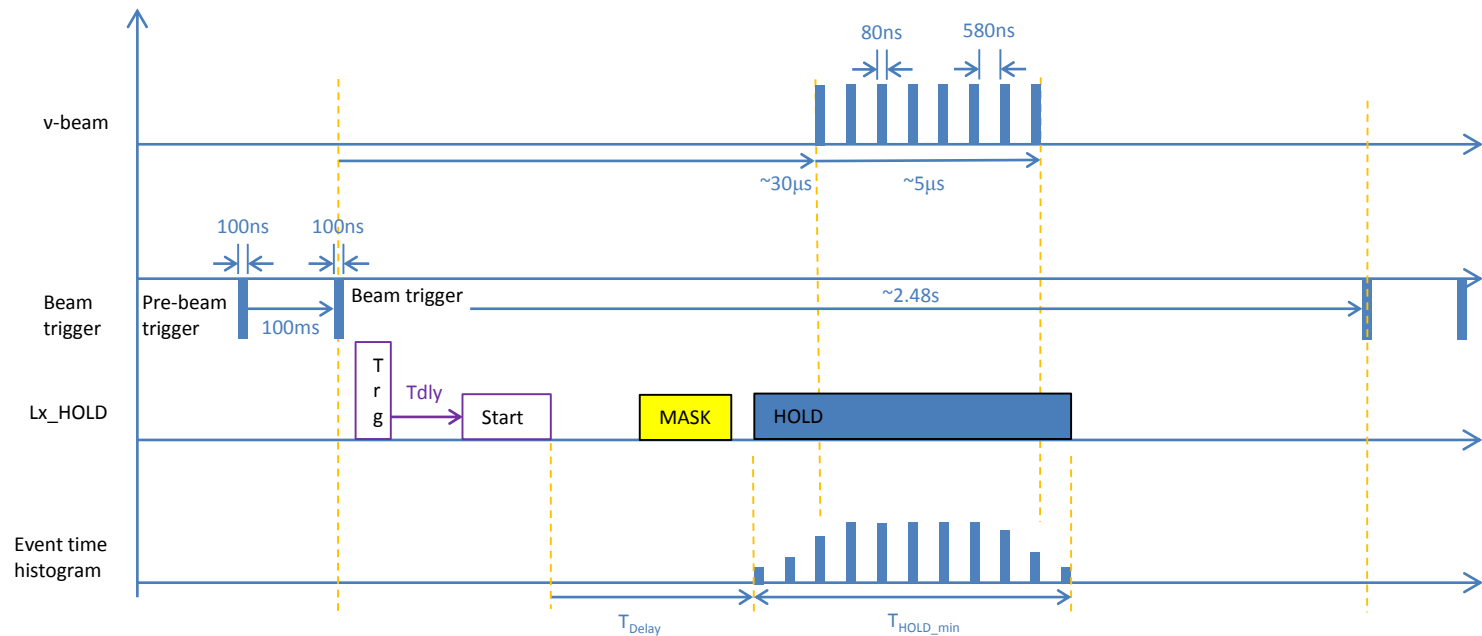
New CITIROC "L1_Hold" Mask and Hold Scheme for WAGASCI T59 - T2K beam operation

22 November 2017



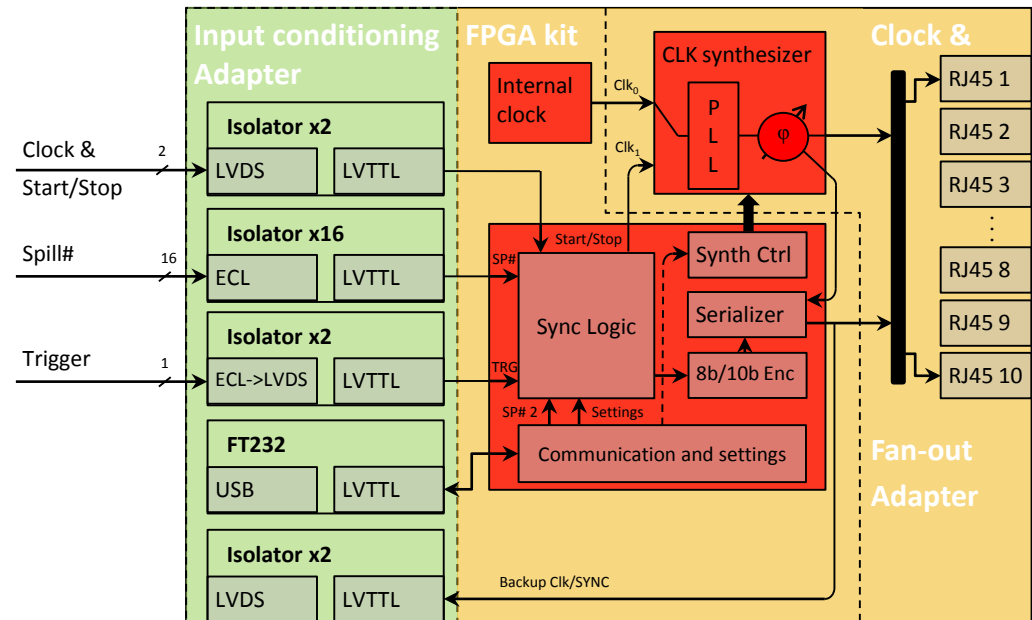
Delay calibration proposition

- Take data with $T_{\text{Delay}}=0$ and large THOLD
- Make a histogram of hit times
- Determine T_{Delay} and T_{HOLDmin} from the histogram



MCB prototype development status

- A pair of FPGA DE10-nano kits have been ordered
- The input adapter schematic is almost complete (also doubles as plan B adapter)
- The exact mapping of spill number signals on the 2x17 ribbon cable isn't known yet
- The exact mapping of spill number signals on the 2x17 ribbon cable isn't known yet
- To be synchronized to UniGe parts database and start PCB design next week
- The fan-out adapter design has barely started
- The FPGA firmware development hasn't started yet



MCB installation and connectivity

- Initial proposition to install the MCB inside the 6U VME crate alongside GDCC/CCC was found hard to achieve. New solution is needed.
- Powered from an outlet adapter
- SYNC outputs - 8 CAT6 cables to the Baby-MIND mini-crates
- Computer control – USB or LAN connection via onboard USB/LAN serial converter
- Clock signal input – LVDS on HDMI from CCC
- Synchronization signals – ECL on ribbon cables from the pair of Philips scientific 726 modules
- Cable lengths and installation paths TBD

WAGASCI trigger rack

Pictures

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WAGASCI Module Rack

Switch Hub
- DAQ Line

Display
- Keyboard
- Mouse
- Display Switch

NIM bin
- ZedBoard
- ECL/TTL conv.
- NIM/TTL conv.

Laptop PC
for WaterSensor

VME crate
- CCC
- GDCC

UPS
Analysis PC

DAQ PC



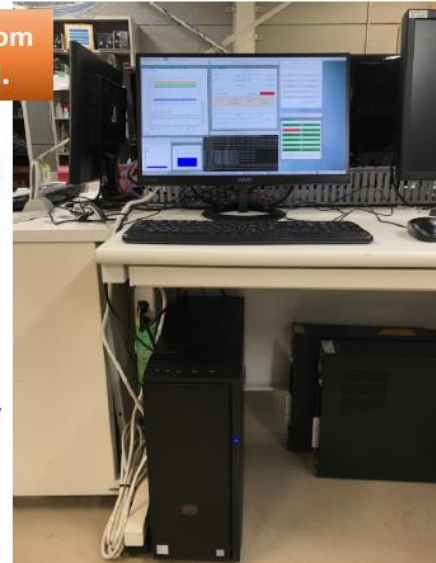
Beam Trigger Modules



Control Room at NA Bld.

**Display &
Keyboard**

Access PC



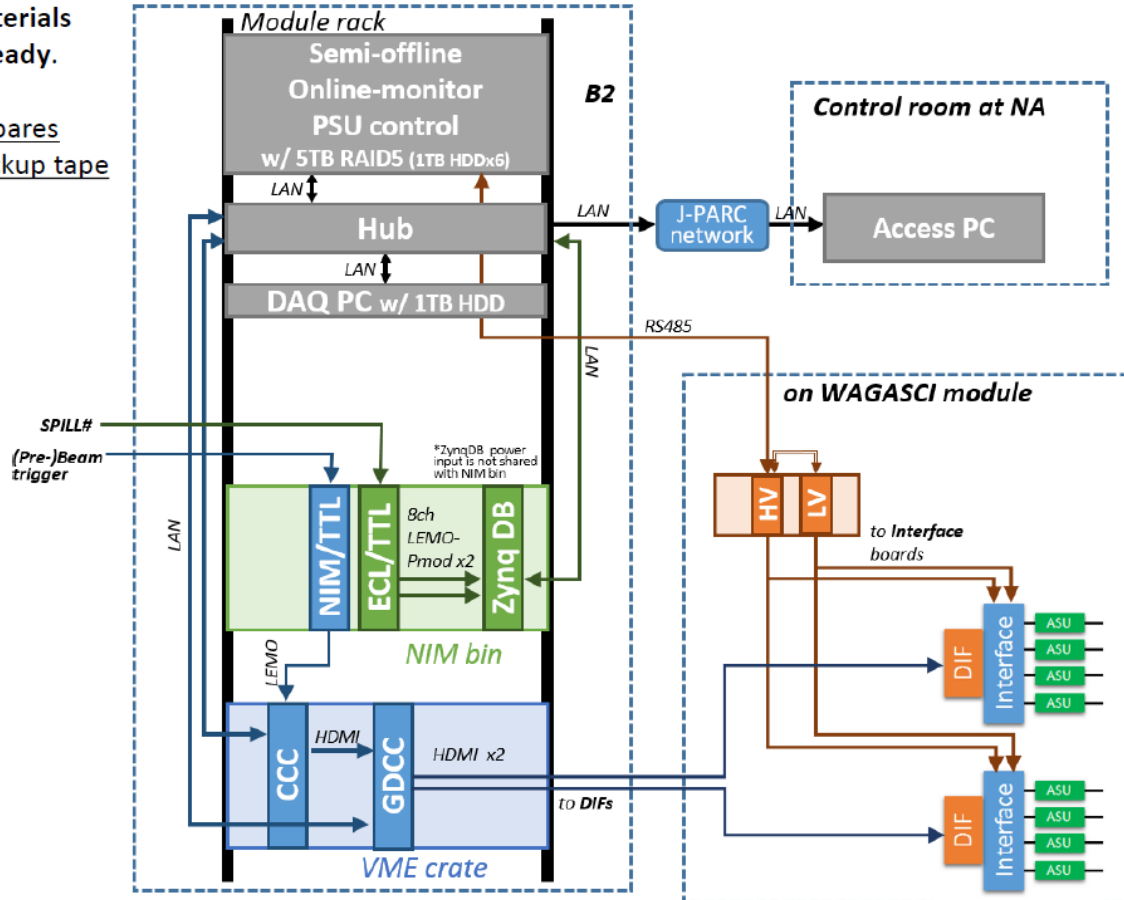
Borrowed
from a slide by
N. Chikuma

WAGASCI trigger rack

The whole system

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- Almost all materials have been ready.
- TODO
 - To prepare spares
 - To set up backup tape in KEKCC



Borrowed from a slide by N. Chikuma

- **Backup Slides**

