

DAQ in practice...  
during summer 2017 beam tests

E. Noah

8 December 2017

T9 control room

T9 beam area



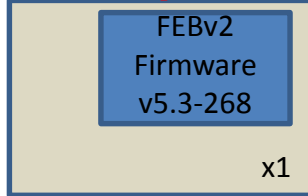
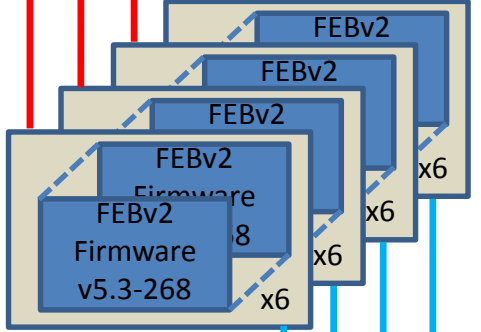
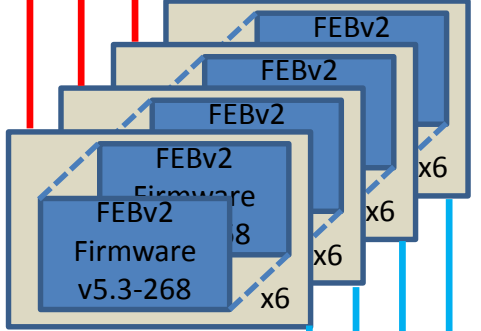
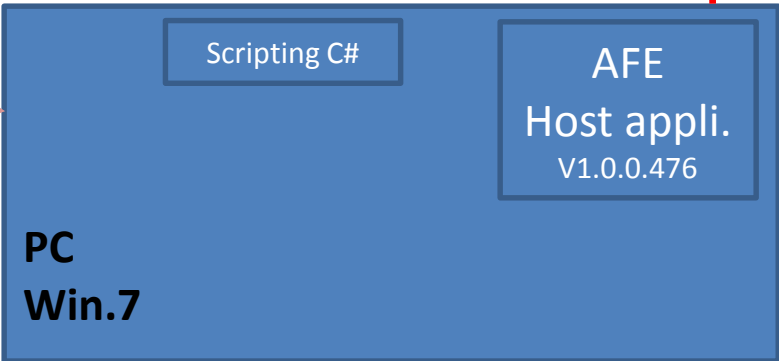
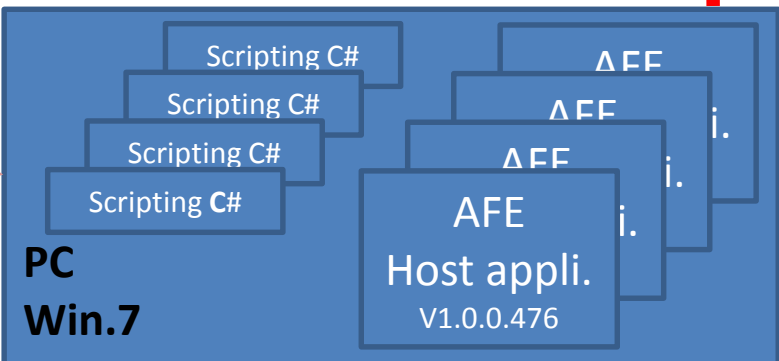
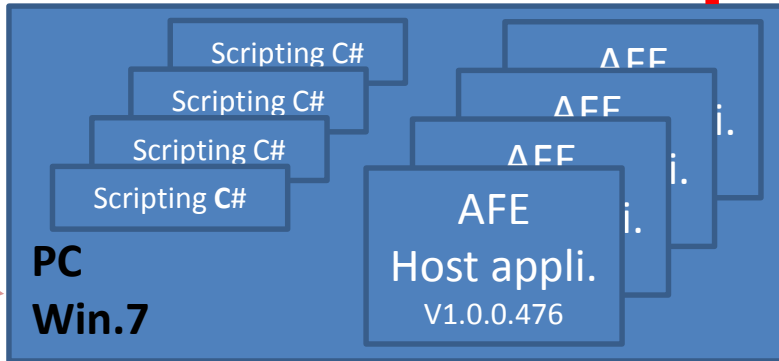
Remote desktop connection



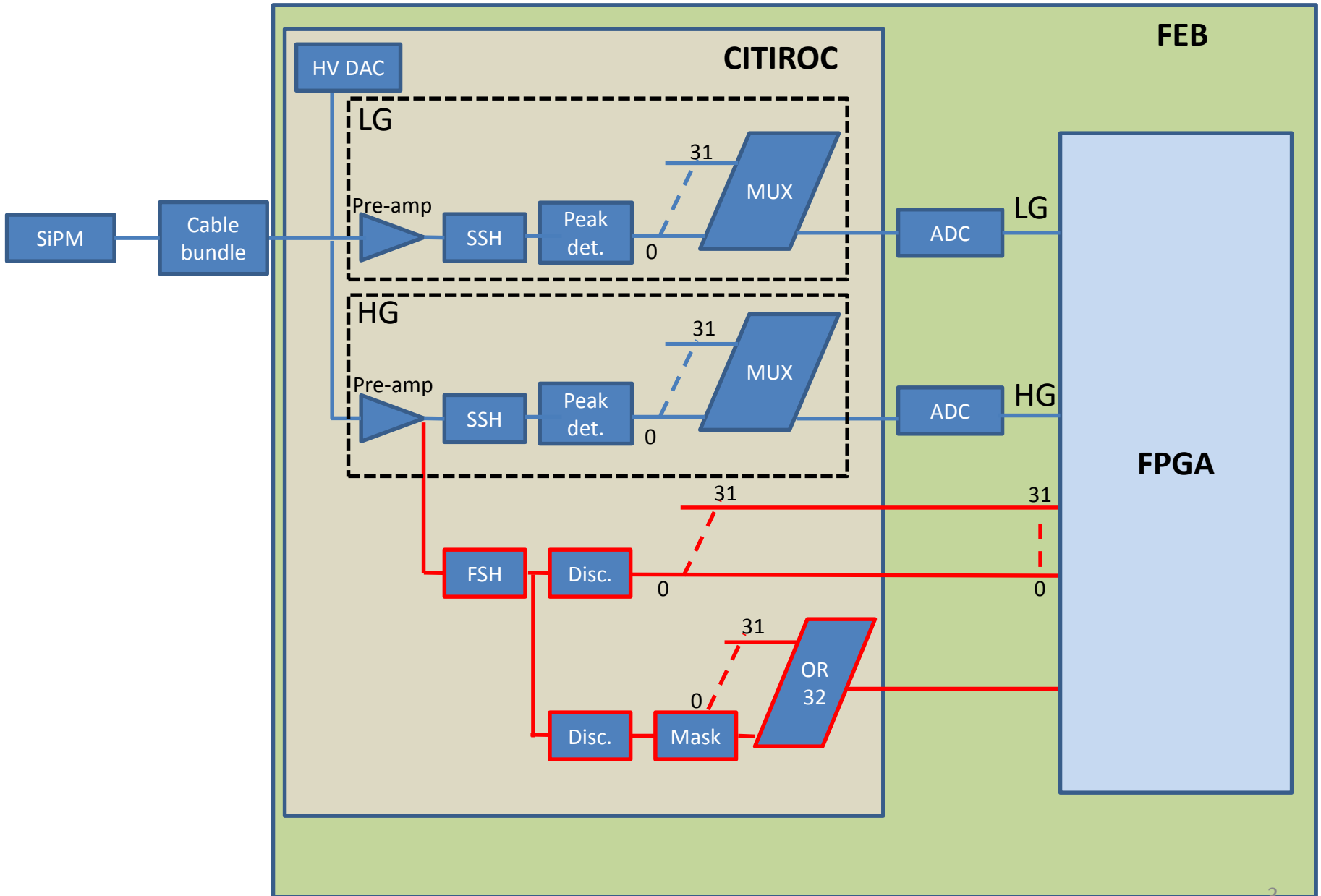
Remote desktop connection



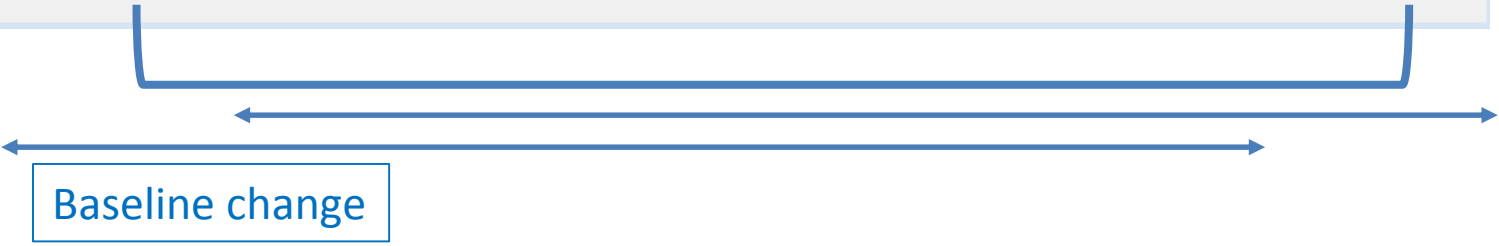
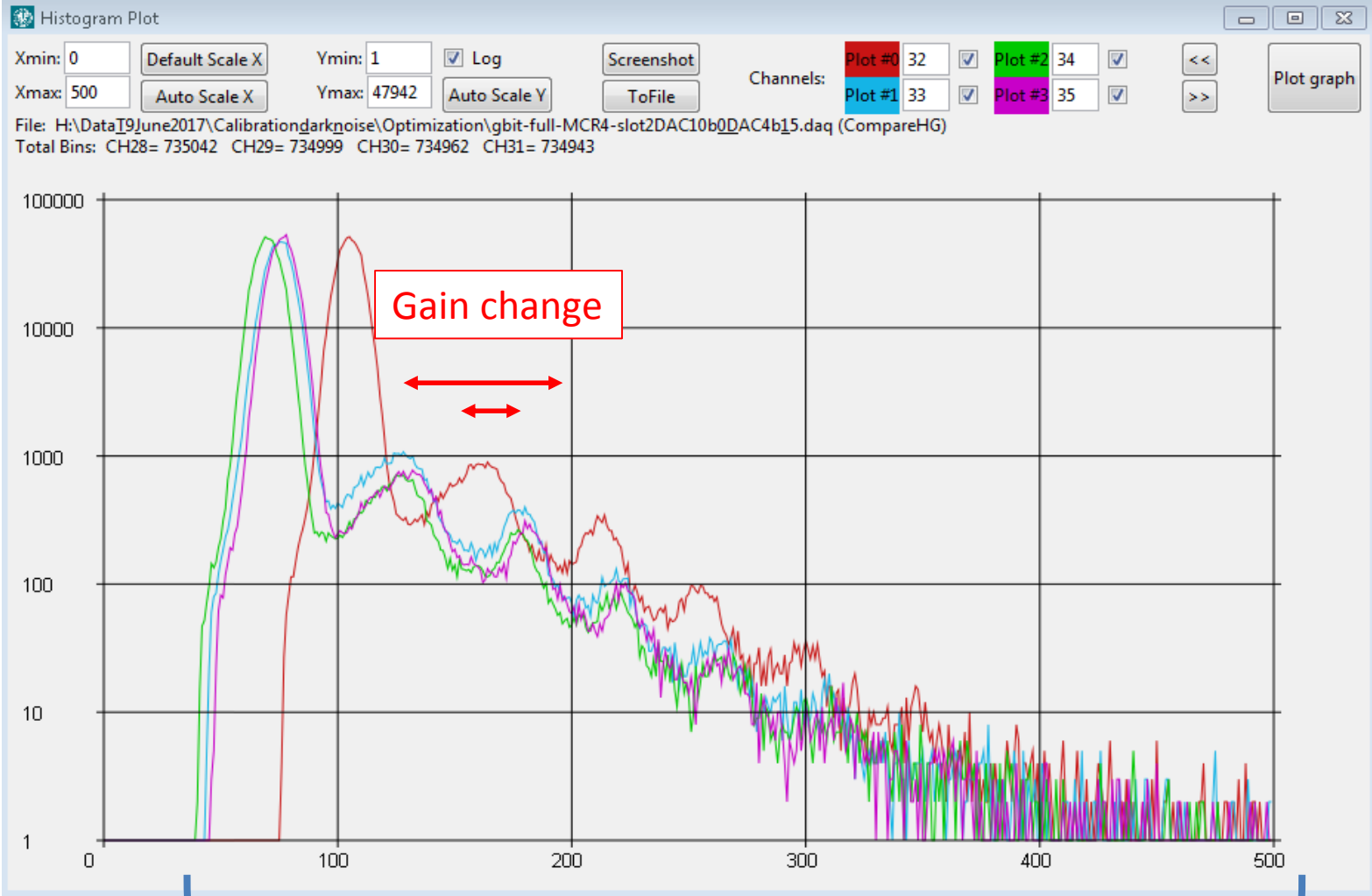
Remote desktop connection



**Signal paths from SiPM affecting signal levels (assume L1Hold does not...)**



# Gain and baseline changes



## Some parameters that are set

component	Parameter	Controllable?	Controllable per ch?	Gain	Baseline shift
SiPM	Device Operating V (f(T))	No	No	-	-
Cable bundle				?	?
CITIROC	HV input DAC	Yes	Yes	Yes	??
CITIROC	Pre-amp HG	Yes	Yes	Yes	??
CITIROC	Shaper time constant	Yes	No	Yes? (TBM)	??
<b><u>Threshold</u></b>					
CITIROC	DiscriDAC10b	Yes	No	??	??
CITIROC	DiscriDAC10b_t	Yes	no	??	??
CITIROC	DiscriDAC4b_Trigger	Yes	Yes	??	??
CITIROC	DiscriDAC4b_Trigger_t	Yes	Yes	??	??
FPGA/ADC	Sampling point	Yes	No	?	?

## Stages possibly affecting I/V levels for signals from SiPM to FPGA

Component	Parameter	Input stage			Output stage		
		Control?	Gain	Baseline shift	Control?	Gain	Baseline shift
SiPM	Operating V (f(T))				No	-	-
Cable bundle	??	No	??	??		??	?
CITIROC	Pre-amp	No	??	??	No	??	??
<b>Analogue data path</b>							
CITIROC	Slow Shaper (HG)	No	??	??	No	??	??
CITIROC	Peak Detector (HG)	No	??	??	No	??	??
CITIROC	Multiplexer (HG)	No	??	??	No	??	??
ADC	ADC	No	??	??	no	??	??
FPGA	-	No	??	??	No	??	??
<b>Trigger/Digital path</b>							
CITIROC	Fast Shaper	No	??	??	No	??	??
CITIROC	Discriminator_t	No	??	??	No	??	??
CITIROC	Discriminator	No	??	??	No	??	??
CITIROC	OR32	No	??	??	No	??	??

# Host application run from Windows 7

File Util App Help

## Baby-Mind Front End Interface

Version: 1.0.0.476(476)

Config File :  
H:\Data\magnet\_reversed\run100\Configurations\MCR4\PDdiscr-allchannels-extclk\_with\_spill\_gtrig\_only\_on\_spill\_slot4.xml

Board: ASIC0 ASIC1 ASIC2 FPGA HvOn

Device Connected: Reconnect Board ID: 32  Bus Association Reload Bus Assoc.

0: (0x206B - 0x0C00) Unige FX3 USB Readout Gateway Get Firmware Version ?

### Status

Get

- HvOn
- GlobalTrigEn
- AsicEventEn
- InternalGenEn
- IntClkSelLocked
- ExtClkSelLocked
- GtrigSynchronized
- GtRxSynchronized
- L0FifoErr
- L1FifoErr
- L2FifoErr
- DoutMuxErr
- L1AdcErr
- ValidWordAsics
- ValidWordFPGA

### Direct Parameters

Set

- HvOn
- GlobalTrigEn
- AsicEventEn
- InternalGenEn
- ExtClkSel
- ReadoutSigStartReset
- SpillCntReset
- TriggerCntReset
- L0FifoReset
- L1FifoReset
- L2FifoReset
- L1AdcReset
- FifoDataClear

### Configuration

Start  Send, Verify & Apply Devices:  
 Send Only  ASIC0  HvOn  
 Valid World Only  ASIC1  
 Apply Only  ASIC2  FPGA

Verify Read

### DAQ

Select File DAQ File:  DAQ File Auto-Increment  
Start  RAM Check Only  
Stop  Timeout Errors Check  Monitoring Queue

Total Transferred (KBytes):   
Transfer Rate (KBytes/s):   
Error Count:

#### Readout Start Parameters

- MCBGreset
- MCBReadoutEn
- GlobalTrigEn
- AsicEventEn
- InternalGenEn

### USB Parameters

Timeout (ms)  StopOnTimeout  AutoResetOnTimeout  
 PacketSize (Bytes)  Packets  FileLimit (KB)  
 Queues  StartRequestOnly

### Application

PlotHG  
Plot LG  
Plot TDiff

- Reset Fifos before Start
- Reset Counters before Start
- Reset 'Readout Signal Start' before Start

HG Monitoring Plot

# Host appli ASIC settings

File Util App Help

## Baby-Mind Front End Interface

Version: 1.0.0.476(476)

Config File :  
H:\Data\magnet\_reversed\run100\Configurations\MCR4\PDdiscr-allchannels-extclk\_with\_spill\_gtrig\_only\_on\_spill\_slot4.xml

Board ASIC0 ASIC1 ASIC2 FPGA HvOn

Copy Paste Copy ASIC0 to others Configure

Channels

Copy Channel0 to others  Absolute Indexes (#)

Channel	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20	#21	#22	#23	#24	#25	#26	#27	#28	#29	#30	#31
DAC4bTrigger_t	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	
DAC4bTrigger	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	
inputDAC	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	135	
inputDAC_En	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
HG_Gain	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55		
HG_CTest	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		
LG_Gain	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62	62		
LG_CTest	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		
PA_DIS	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		
DiscriMask	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		

Global Control

- HG\_SCAorPeakD
- HG\_SH\_TimeConstant
- LG\_SCAorPeakD
- LG\_SH\_TimeConstant
- LG\_PA\_WeakBias
- DAC10b
- TriggerPolarity
- En32Trigger
- EnHitMuxOut
- EnOR32
- EnNOR32
- DAC10b\_t
- EnNOR32\_t
- InputDAC\_4V5ref
- InputDAC\_En
- FastShaperOnLG
- RSorDiscri
- SCAweakBias
- PeakSensingBypass
- SelTrigExtPSC

Per Channel

Per ASIC

# Host appli FPGA settings

Baby-Mind Front End Interface

Version: 1.0.0.476(476)

Config File : H:\Data\magnet\_reversed\run100\Configurations\MCR4\PDdiscr-allchannels-extclk\_with\_spill\_gtrig\_only\_on\_spill\_slot4.xml

Board ASIC0 ASIC1 ASIC2 FPGA HvOn

Configure

ASIC (3)

ASIC #0 [Copy] [Paste] [Copy ASIC0 to others]

Channels

[Copy Channel0 to others]  Absolute Indexes (#)

Channel	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16	#17	#18	#19	#20	#21	#22	#23	#24	#25	#26	#27	#28	#29	#30	#31
HitEn	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
HG_En	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
LG_En	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
OR96tAdcEn	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

GlobalControl

TempEn

L1ThresholdHG 200  L1ThresholdLG 350

**Changed in script: HG=200, LG=20**

GlobalControl

<input type="checkbox"/> L0HitLimit	20	<input type="checkbox"/> IntGenPeriod (5us)	5	<input checked="" type="checkbox"/> IndivTriggerDelay (2.5ns)	<input checked="" type="checkbox"/> MCBClkEn
<input type="checkbox"/> L1HvEn	<input type="checkbox"/> HoldLow	<input type="checkbox"/> HoldDis	<input type="checkbox"/> SyncRdEn	<input checked="" type="checkbox"/> ReadoutEnableOnStartSignal	<input checked="" type="checkbox"/> MCBSyncEn
<input type="checkbox"/> L1HaLimit	<input type="checkbox"/> HoldPaDis	<input checked="" type="checkbox"/> ResetPaDis	<input checked="" type="checkbox"/> ReadoutEnableOnSpillGate	<input checked="" type="checkbox"/> ReadoutStopOnSyncRdEn	<input type="checkbox"/> MCBFSyncEn
<input checked="" type="checkbox"/> 1000 L1HoldHG_Delay (2.5ns)	<input checked="" type="checkbox"/> ResetPscDis	<input type="checkbox"/> RazChnDis	<input type="checkbox"/> ReadoutSID	<input type="checkbox"/> GbTDMEn	<input type="checkbox"/> MCBExtGresetEn
<input checked="" type="checkbox"/> 1000 L1HoldLG_Delay (2.5ns)	<input type="checkbox"/> HoldOnRazChn	<input type="checkbox"/> BaselineReset	<input checked="" type="checkbox"/> GbMuxRxEn	<input checked="" type="checkbox"/> SyncSpillResetEn	<input type="checkbox"/> MCBExtReadoutEn
<input type="checkbox"/> 0 L1AdcDelay (10ns)	<input type="checkbox"/> ComputeOutEn	<input type="checkbox"/> BaselineOutEn	<input checked="" type="checkbox"/> SyncTrigResetEn	<input checked="" type="checkbox"/> SyncInExtSpillNbSel	<input checked="" type="checkbox"/> MCBExtSpillGateEn
Static <input type="checkbox"/> L1ThresholdMode	<input type="checkbox"/> CompareOutEn	<input checked="" type="checkbox"/> AdcComputeEn	<input checked="" type="checkbox"/> SyncInGtrigOnlyOnSpill	<input checked="" type="checkbox"/> SyncInGresetEn	<input type="checkbox"/> MCBExtSpillGateInv
<input checked="" type="checkbox"/> L1lthmFast	<input type="checkbox"/> Or32tADC	<input type="checkbox"/> AdcPhase	<input checked="" type="checkbox"/> SyncInReadoutEn	<input type="checkbox"/> Debug0	<input type="checkbox"/> Debug1
<input checked="" type="checkbox"/> L1OR96_Fast	<input type="checkbox"/> 3			<input type="checkbox"/> 0	<input type="checkbox"/> 0
<input checked="" type="checkbox"/> L1AdcCalSync					
<input checked="" type="checkbox"/> L1AnalogLimit10					
<input checked="" type="checkbox"/> L1TriggerLimit10					
<input checked="" type="checkbox"/> ExtGlobalTrig					
<input type="checkbox"/> 0 ExtTriggerDelay					

**Per ASIC**

**Per Channel**

**All ASICs**

**L1Hold** was 2.5  $\mu$ s  
Should be 9-10  $\mu$ s  
at T2K

**L1Hold** start:  
Mostly from **OR32 x3** during beam test  
A few runs from **OR96**

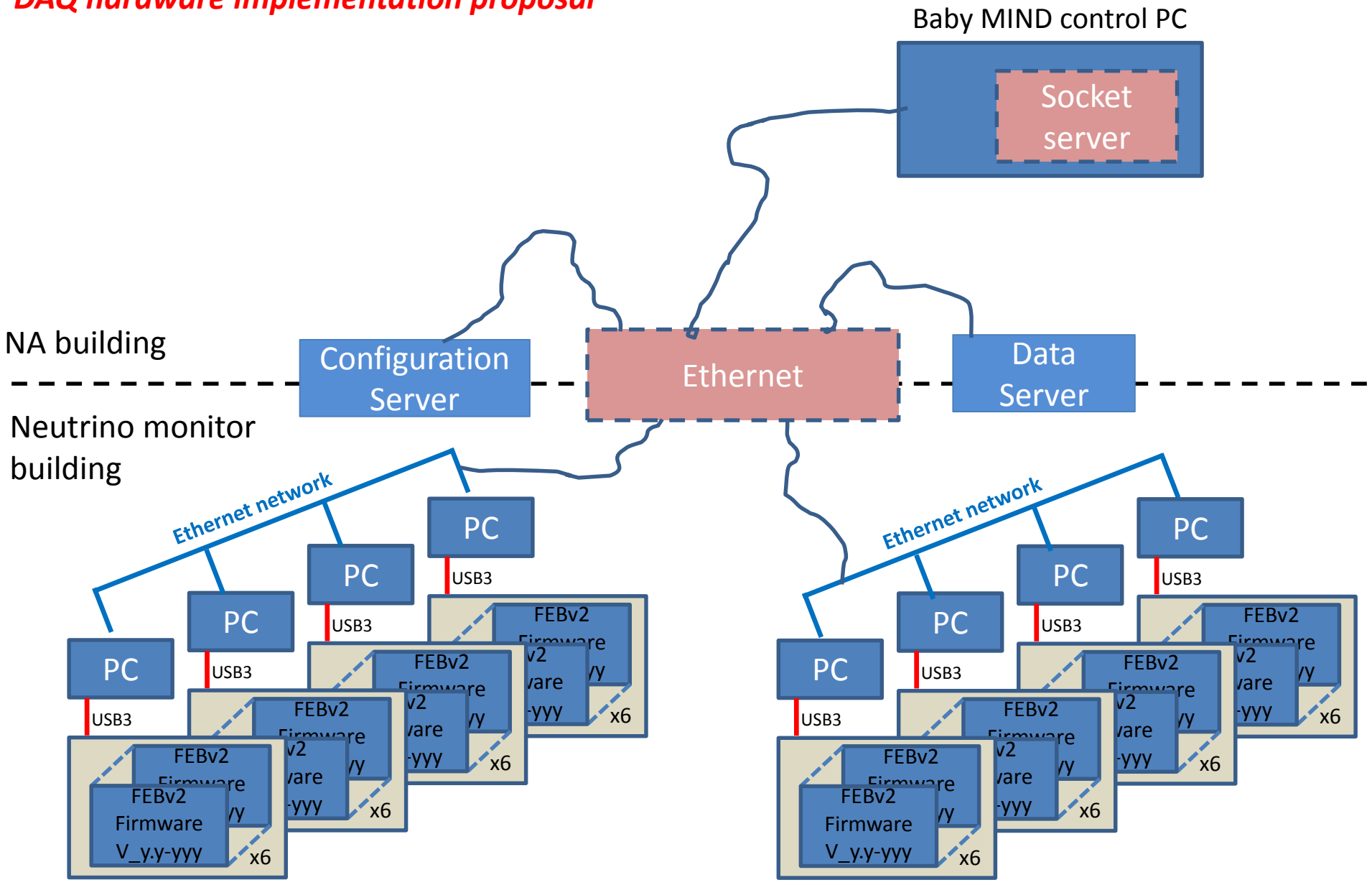
## How the settings were chosen (without the benefit of hindsight!)

- Many issues with unpacking of data during beam tests:  
*with untested unpacking software and without adequate diagnostic tools*
- Settings for discriminator DAQ and FPGA thresholds were chosen based on balancing:
  - *Reduction in readout errors experienced during tests (function of data acquisition rate)*
  - *Efficiency in collecting “beam” data (as opposed to dark counts)*

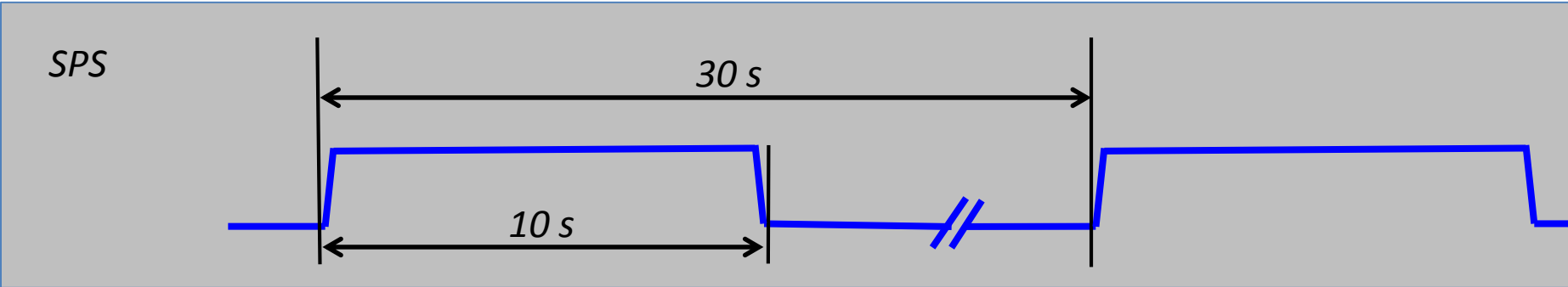
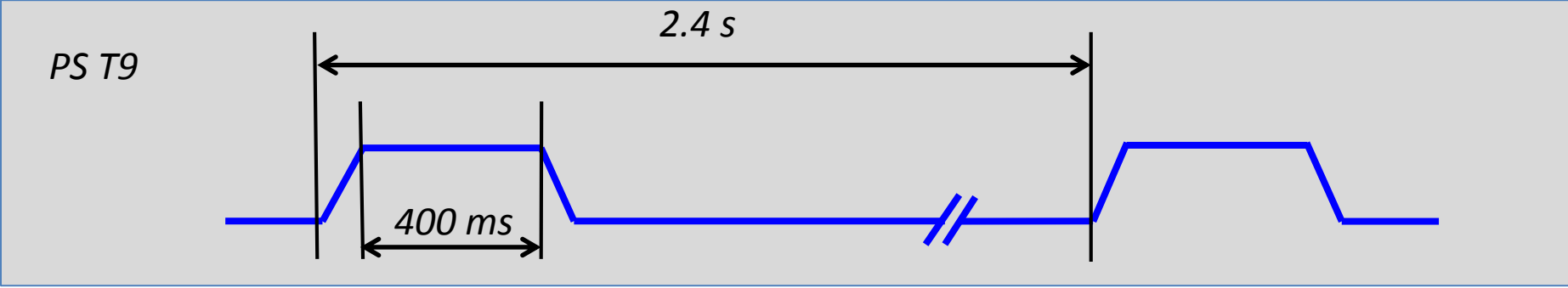
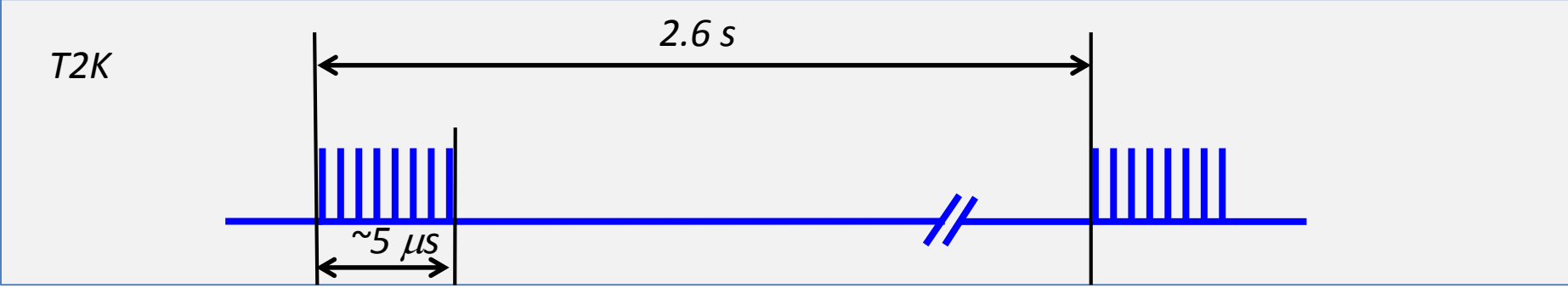
	Run1000 (similar to all runs taken)	Run1100 (special run)	Run1200 (special run)
Or32tADC	False (OR32 x3)	True (OR96)	True (OR96)
HG_SH_TimeConstant (12.5 ns steps)	1	4	1
LG_SH_TimeConstant (12.5 ns steps)	1	4	1
L1_HoldHG_Delay (2.5 ns)	1000	3000	1000
L1_HoldLG_Delay (2.5 ns)	1000	3000	1000

# *Few notes for DAQ at J-PARC*

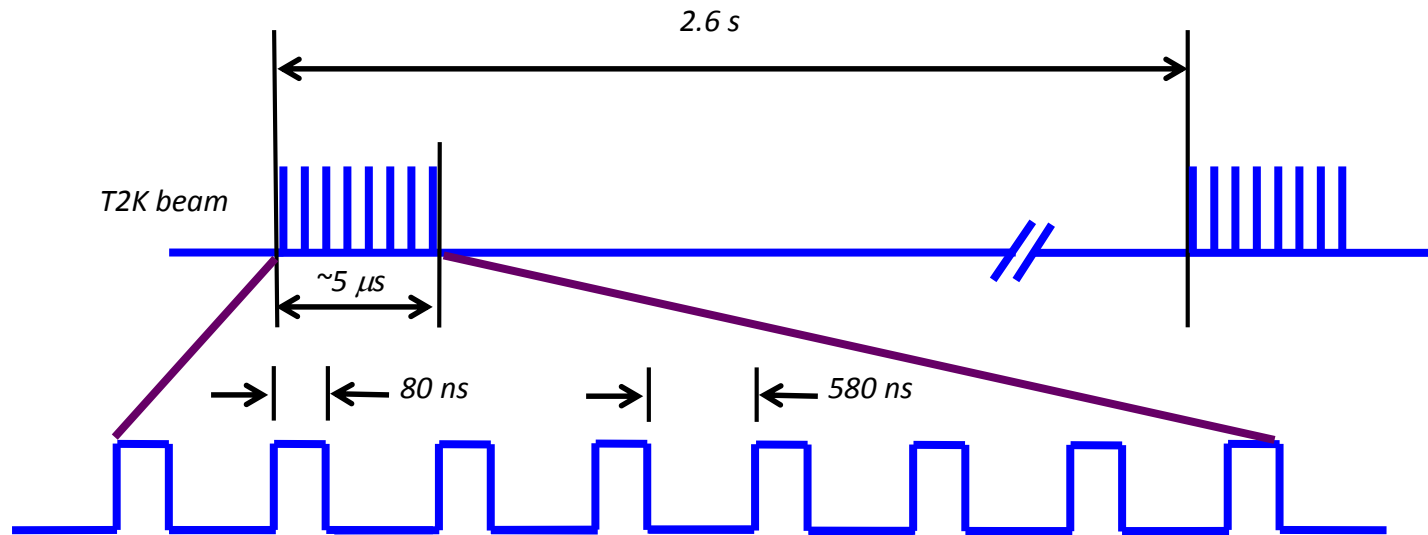
# DAQ hardware implementation proposal



**Beam time structures**



## T2K Beam bunch structure



### Event rates per spill @ Baby MIND

( $\sim 7 \text{ m}^2$ , 61 t Fe) for 750 kW:

- WAGASCI events:  $< 0.01$
  - $\nu$  interactions in Baby MIND:  $< 3$
  - beam induced events (non-WAGASCI):  $< 4$
- on average **1 muon track per bunch**

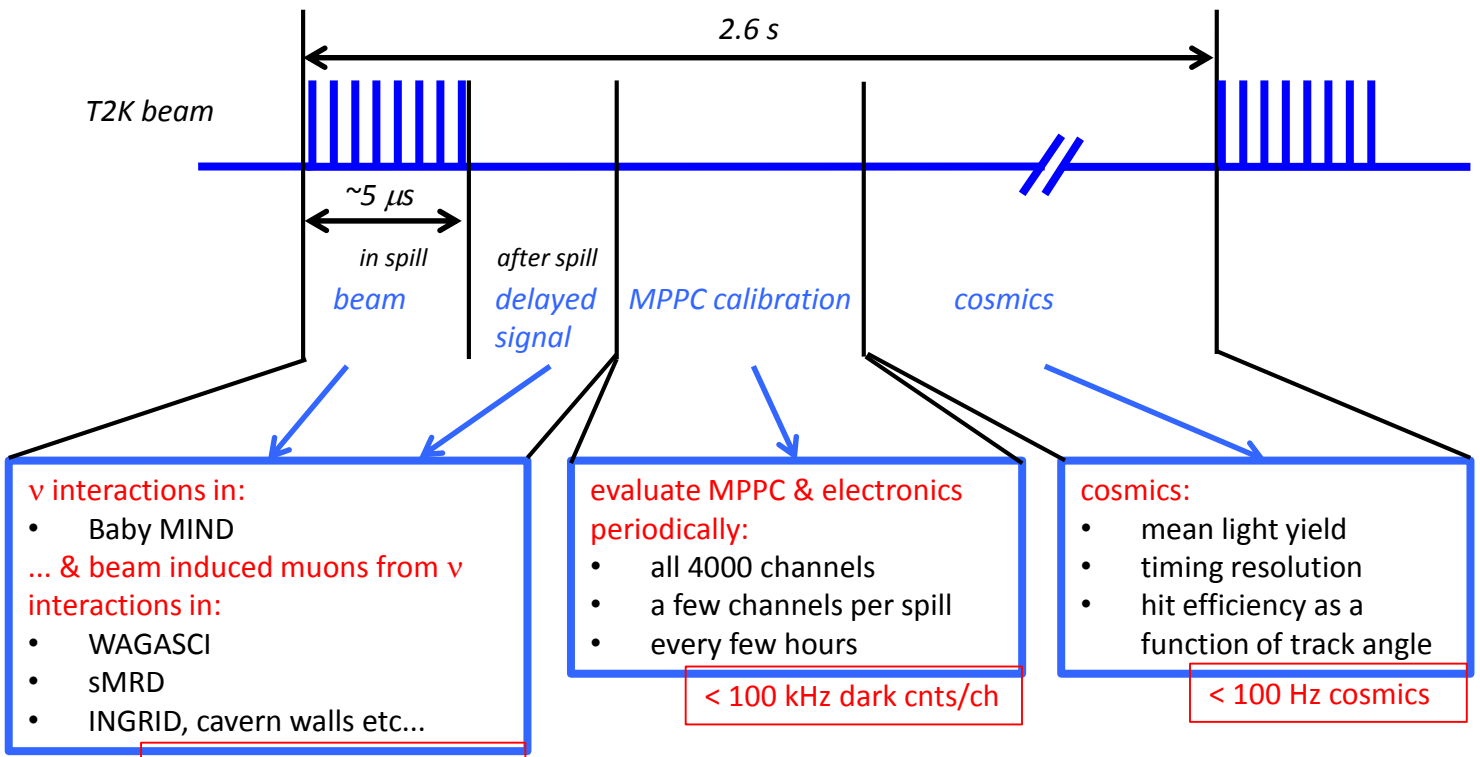
NIM A 694 (2012) 211-223:

PhysRev D90, 052010 (2014) ( a little more... x1.36 TBC )

e.g. event rates @ INGRID ( $\sim 22 \text{ m}^2$ , 99.4 t Fe):

- $\nu$  events:  $1.5 / 10^{14}$  POT
  - beam induced events cavern walls:  $4 / 10^{14}$  POT
- for runs I and II: max. 145 kW ( $3 \times 10^{14}$  POT  $\rightarrow$  750 kW) <sup>14</sup>

# Baby MIND data taking at WAGASCI T59



**ν interactions in:**

- Baby MIND

**... & beam induced muons from ν interactions in:**

- WAGASCI
- sMRD
- INGRID, cavern walls etc...

< 10 muon tracks per spill  
< 100 hits per FEB per spill

... but depending on DAC threshold level, will also get dark counts

**evaluate MPPC & electronics periodically:**

- all 4000 channels
- a few channels per spill
- every few hours

< 100 kHz dark cnts/ch

**cosmics:**

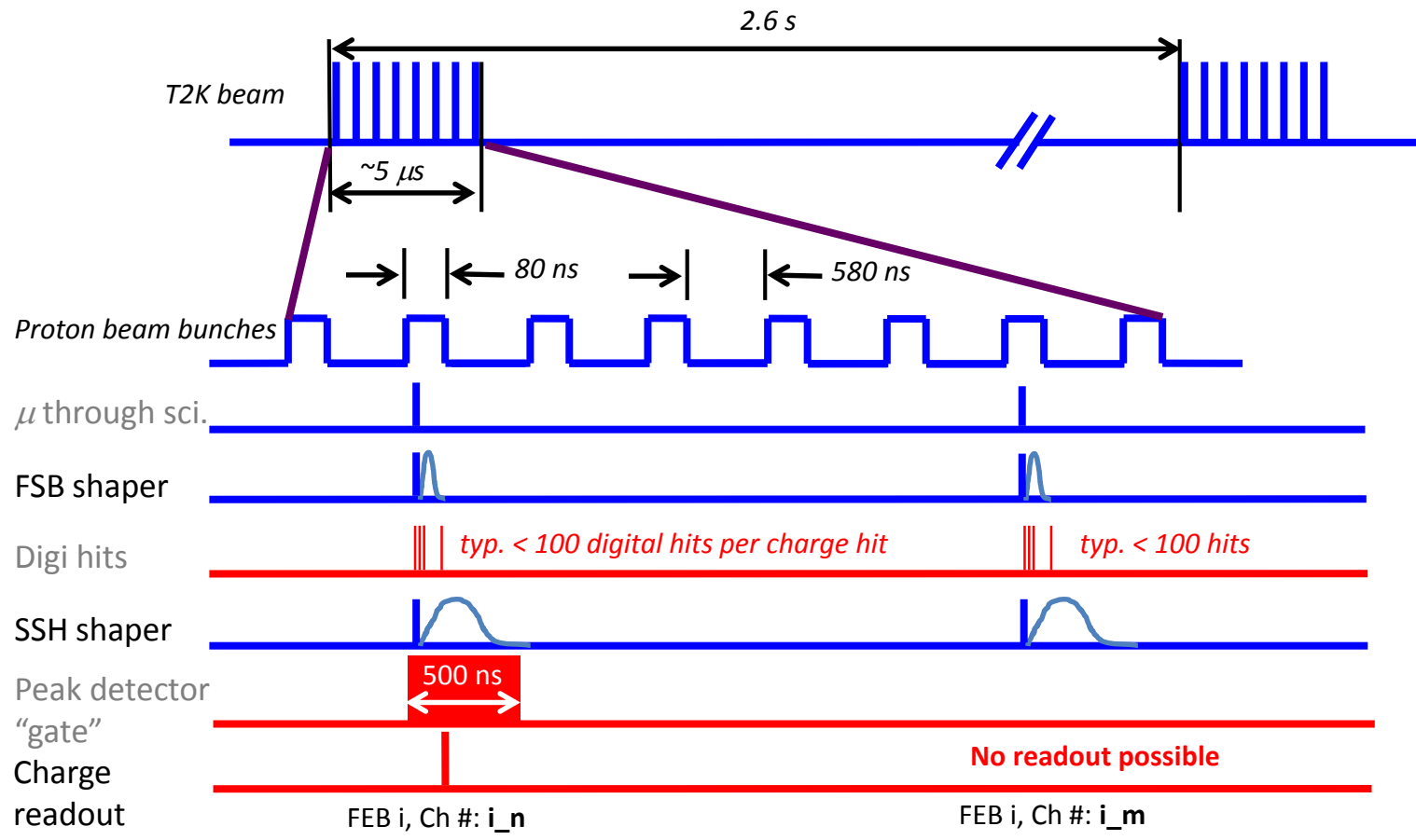
- mean light yield
- timing resolution
- hit efficiency as a function of track angle

< 100 Hz cosmics

Need functionality to change ASIC configuration!

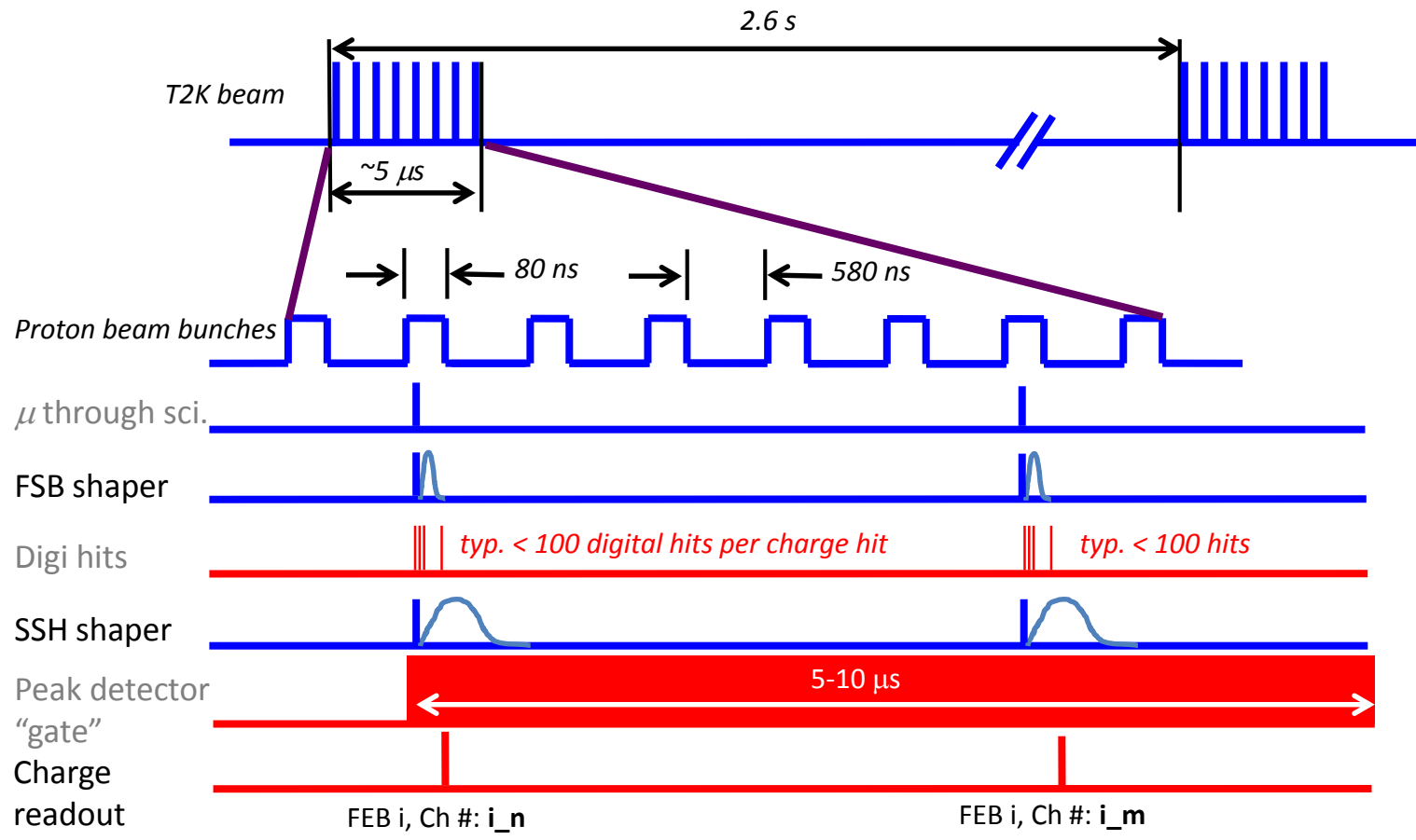
*Optimising the readout of analogue  
signals from CITIROC*

**Readout with peak detector window set to 500 ns**



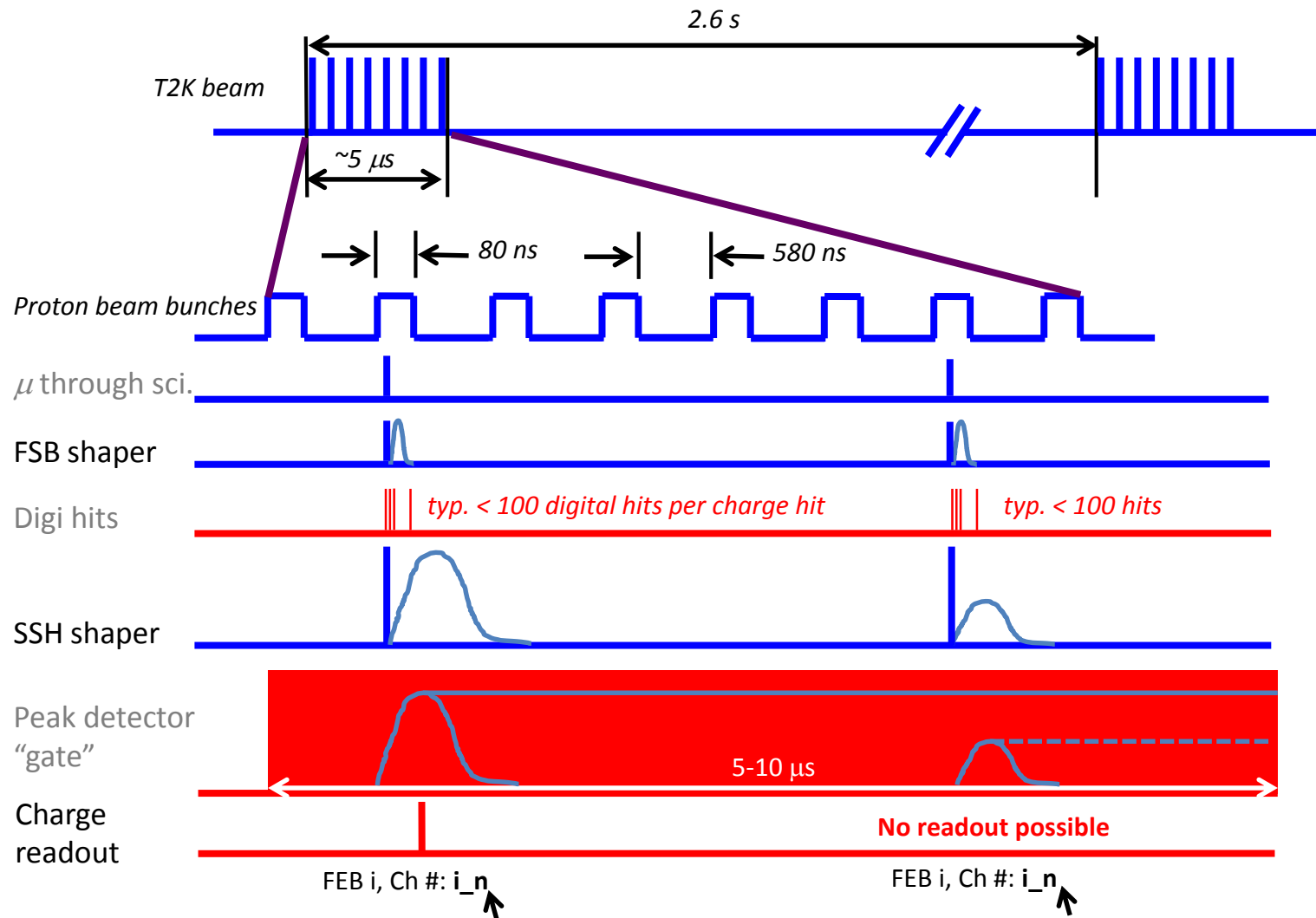
# Readout with peak detector window set to 5-10 $\mu$ s

Charge readout from two separate channels is possible  
Use digital trigger hits to reconstruct event time



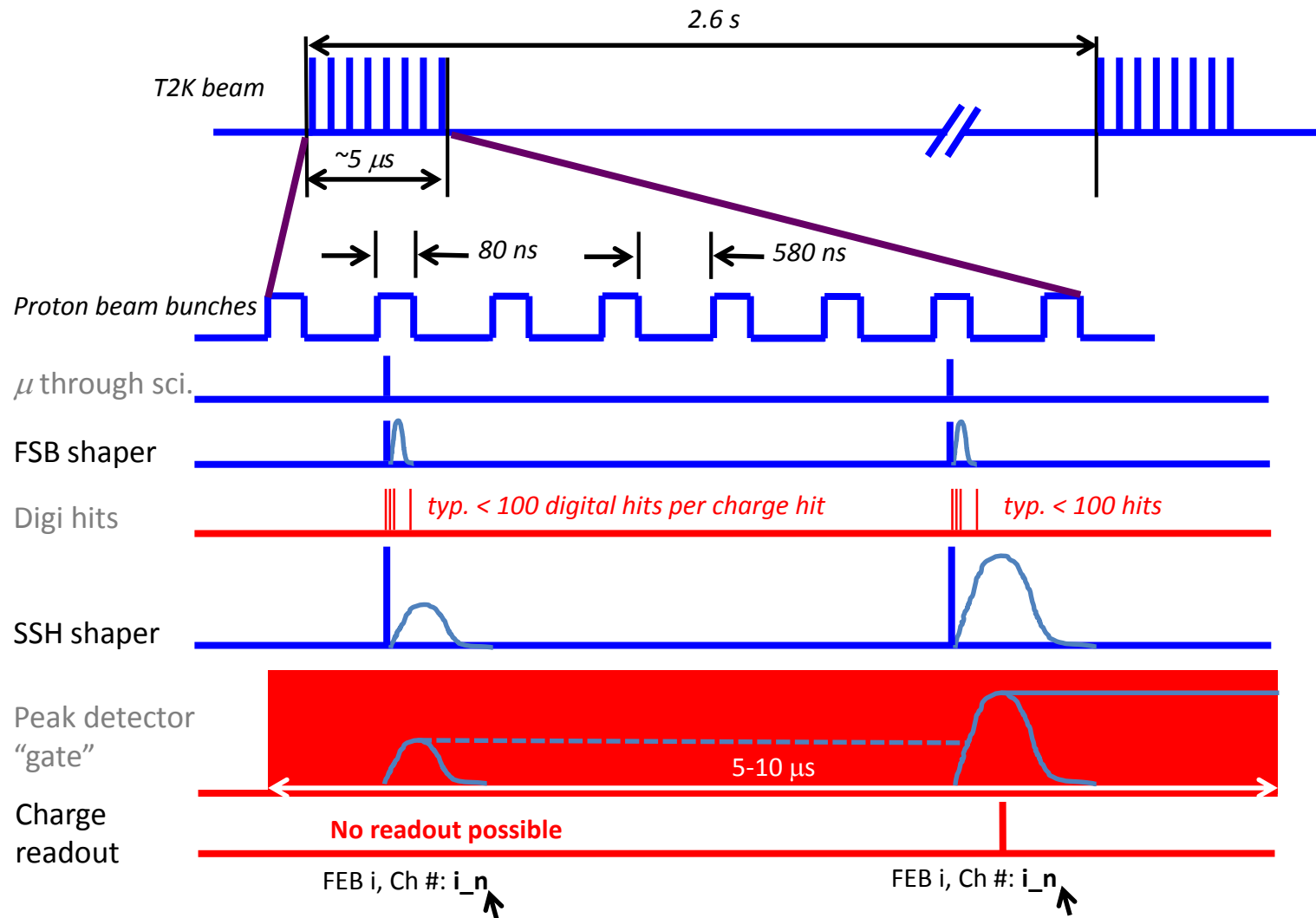
**Readout with peak detector window set to 5-10  $\mu\text{s}$ : Channel occupancy >1 within spill**

For a given channel "Peak detector" will only retain highest amplitude hit occurring in its 10  $\mu\text{s}$  window

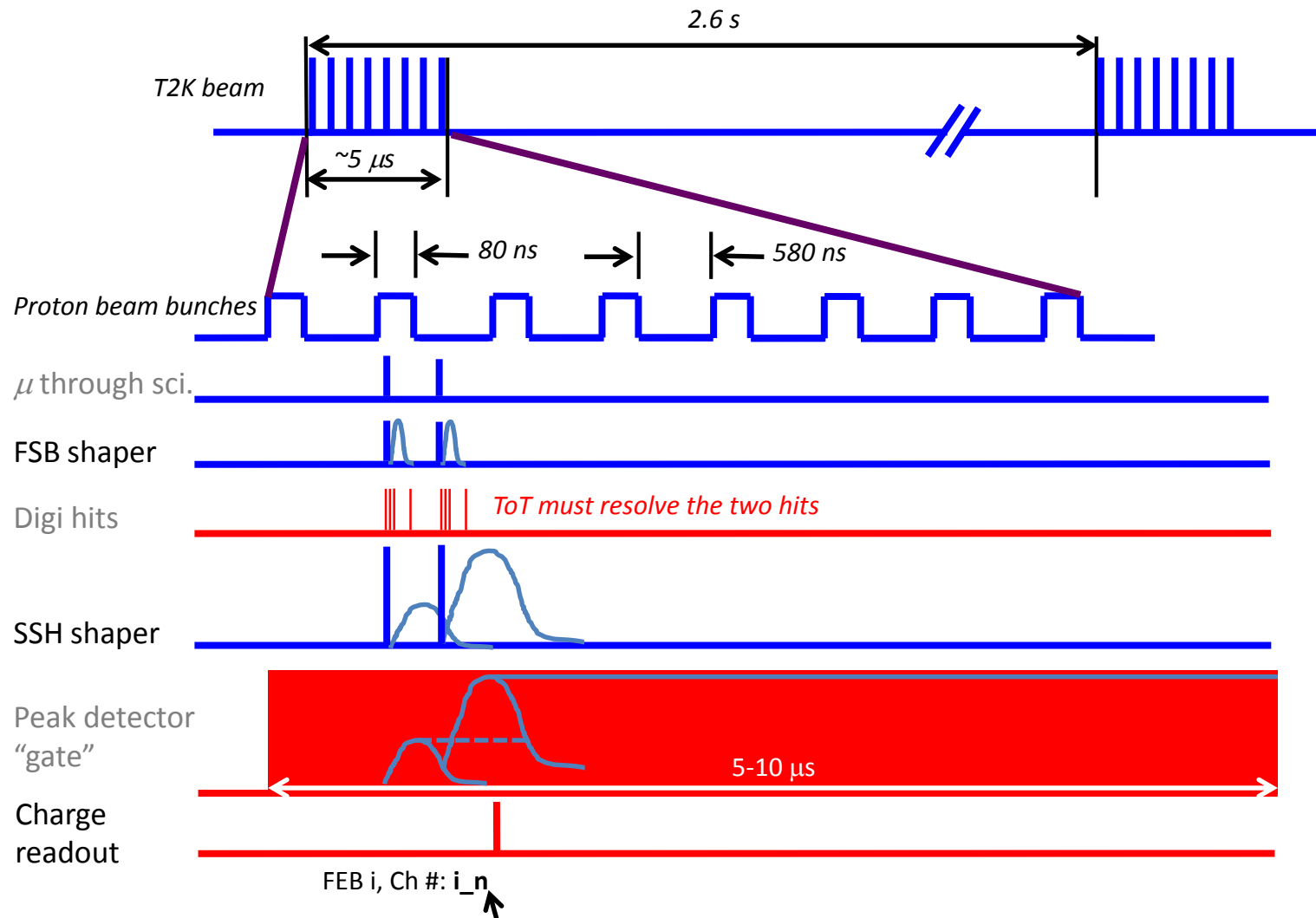


**Readout with peak detector window set to 5-10  $\mu\text{s}$ : Channel occupancy >1 within spill**

For a given channel "Peak detector" will only retain highest amplitude hit occurring in its 10  $\mu\text{s}$  window

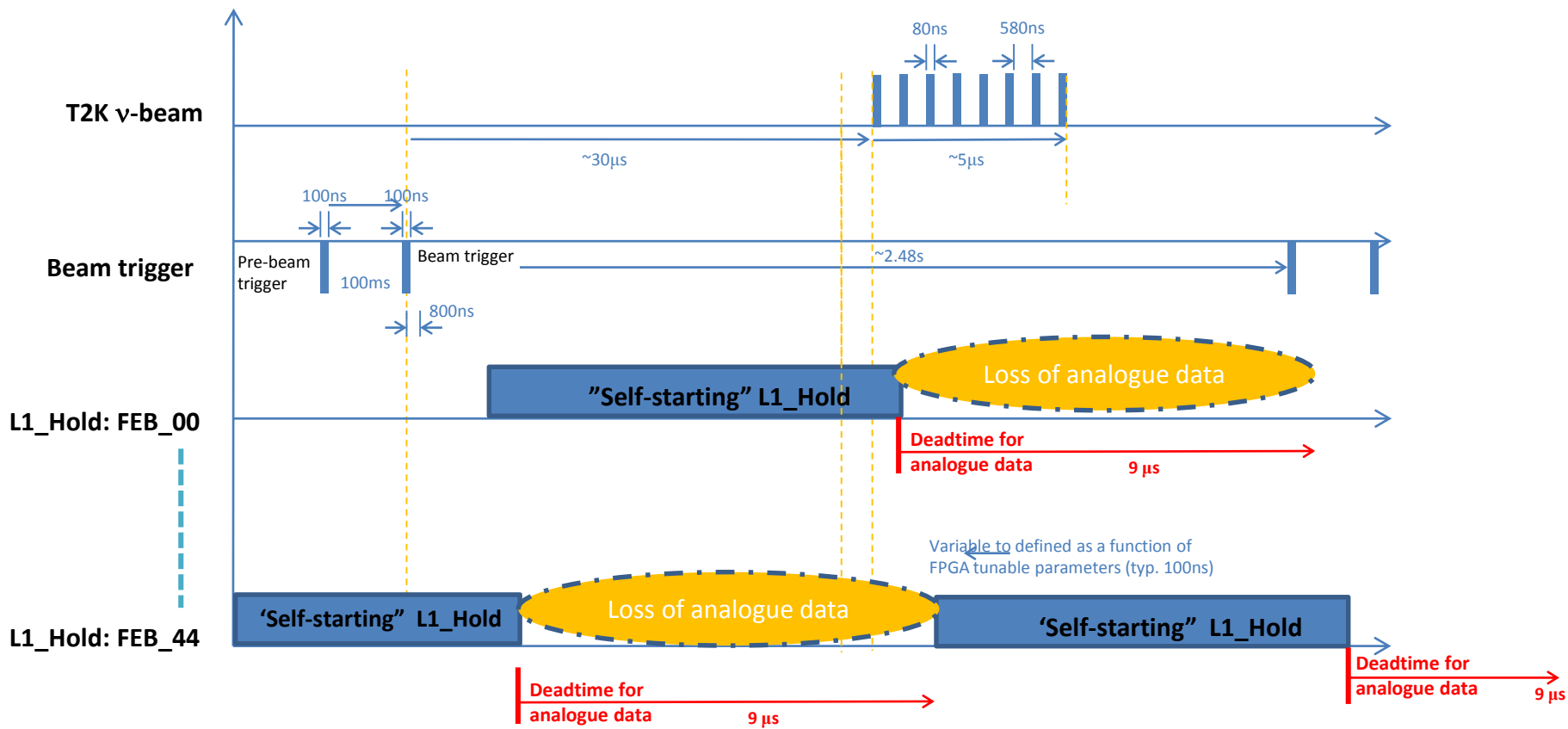


**Readout with peak detector window set to 5-10  $\mu\text{s}$ : Channel occupancy >1 within spill**



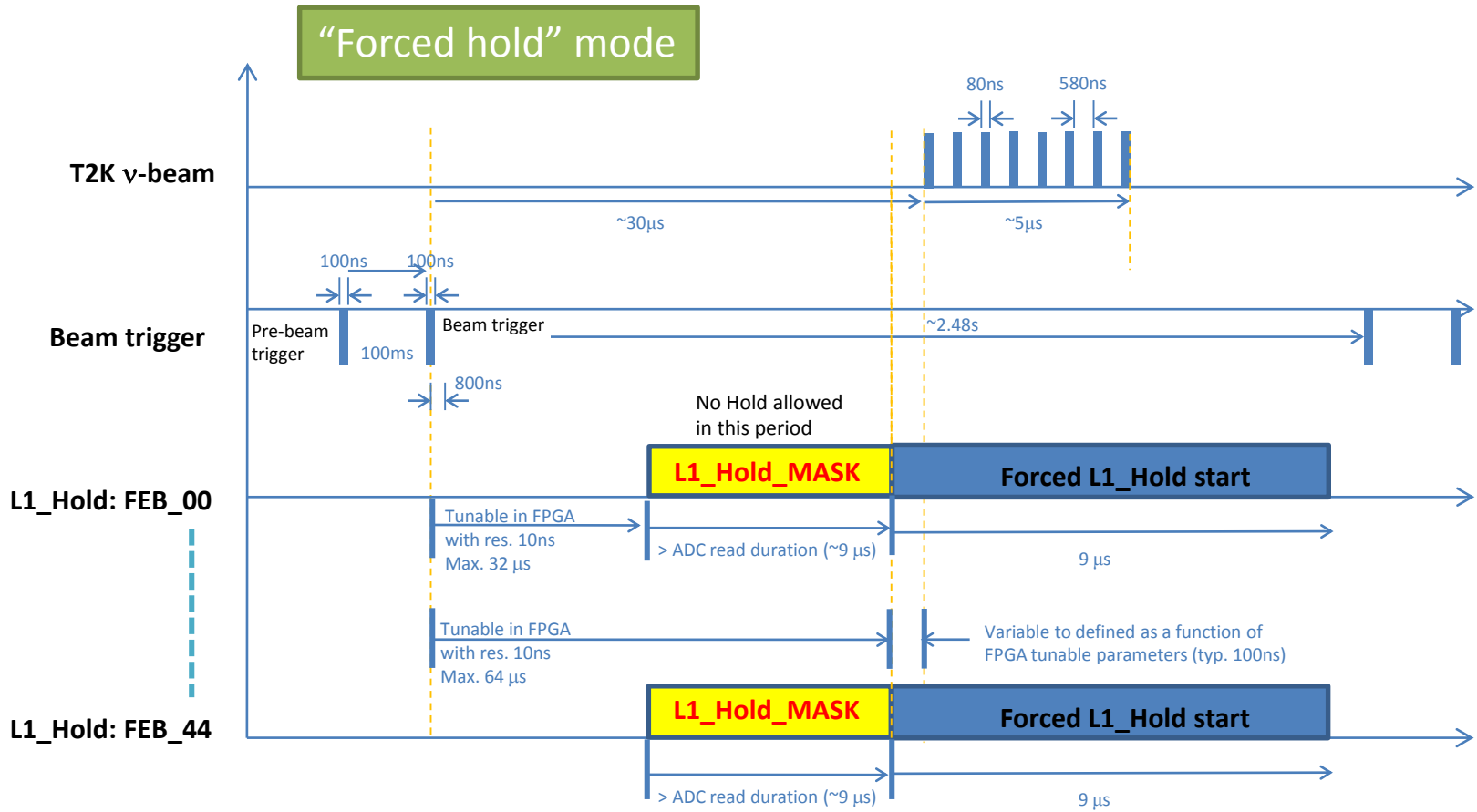
**For summer 2017 beam test: L1Hold starts independently for all 44 FEBs**  
**... Consequence of this for operation with T2K beam**

“Free hold” mode, all CITIROCs are “self-starting”



# New CITIROC "L1\_Hold" Mask and Hold Scheme for WAGASCI T59 - T2K beam operation

22 November 2017



All FEBs have synchronised L1\_Hold start and end