



BE Beams Department | Beam Instrumentation

LIU BWS electronics

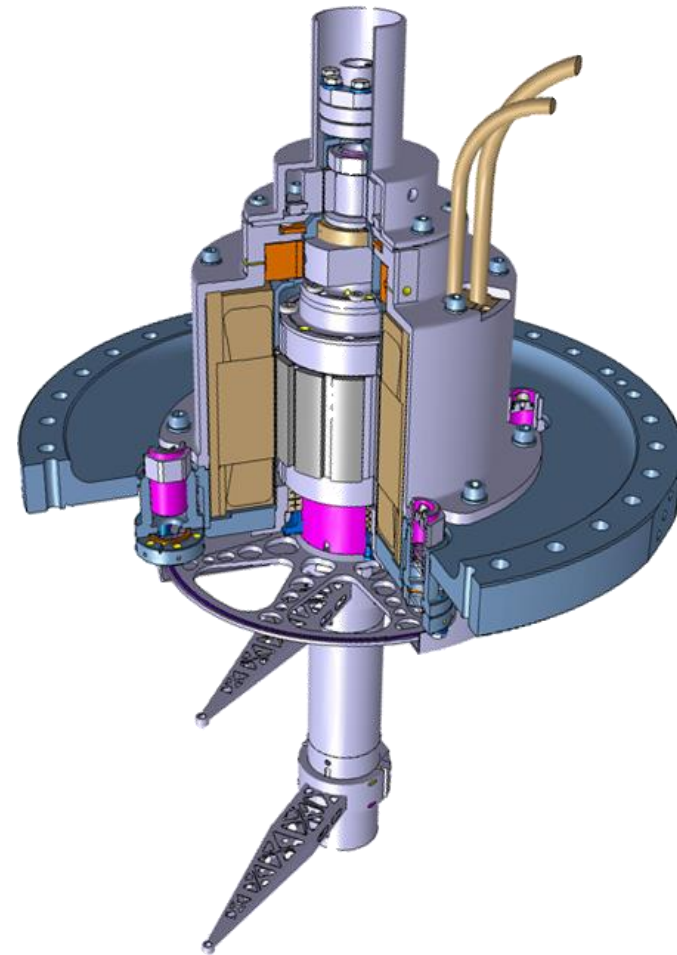
J. Emery for the Beam Wire-scanner team

BI-TB 26.01.2018



Content

- Wire-Scanner system architecture
- Electronics hardware
- Firmware / Software
- Lab tests
- LIU electronics for the linear scanners
- 2018 milestones





Laboratory tests (January 2018)



Motor Bench

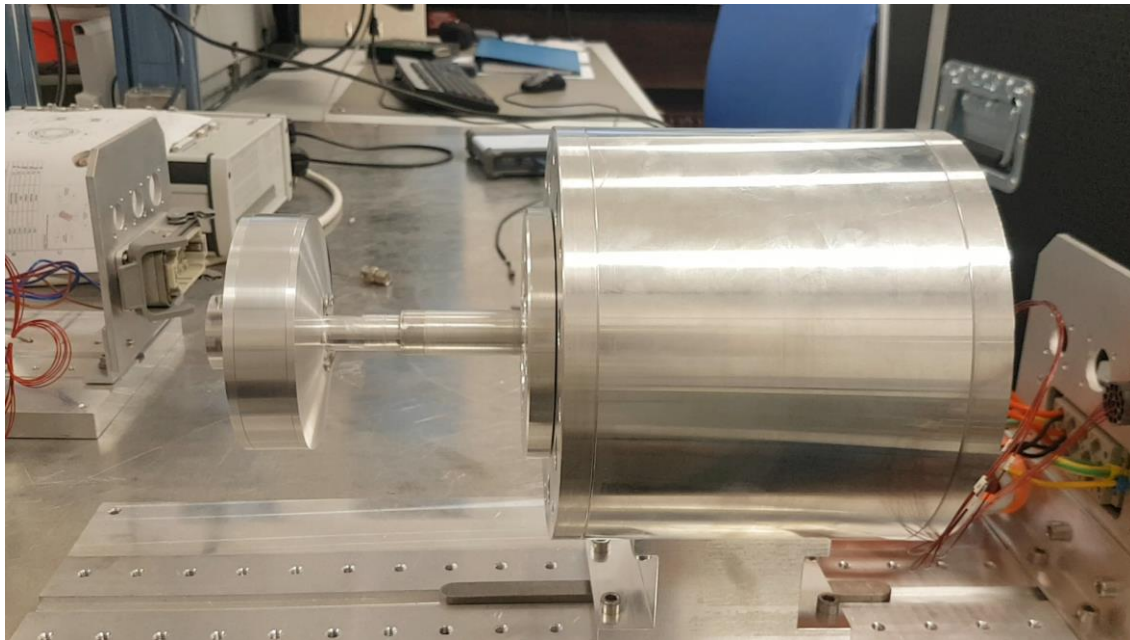
Dspace control system

VFC based control system

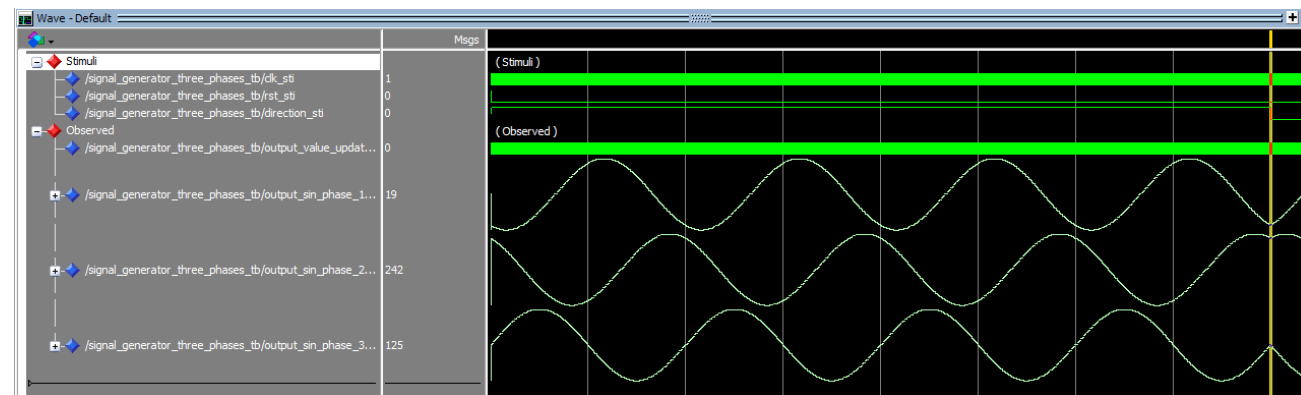
Intelligent Drive Crate (IDC)



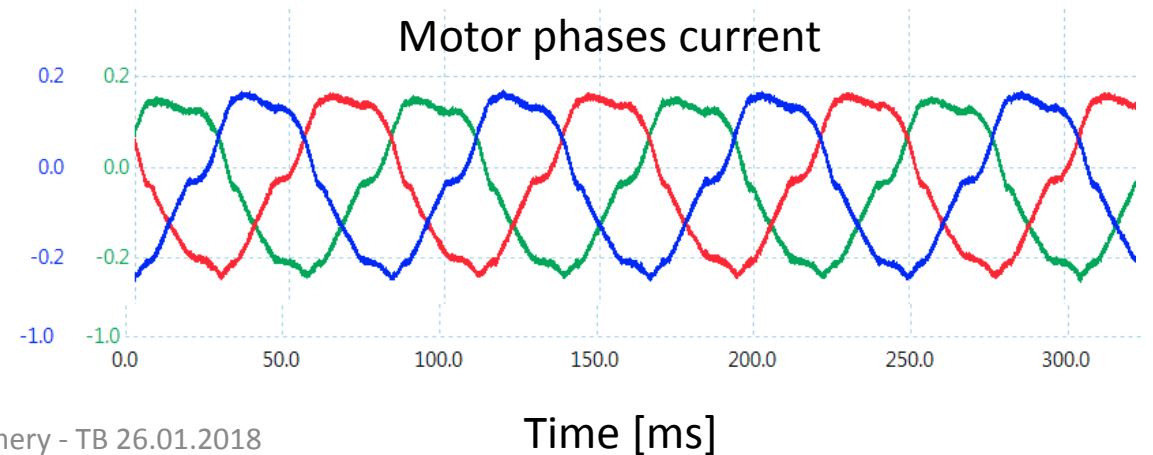
Laboratory tests: Custom power driver + VFC based control



3 phases control signals simulation in VHDL (Modelsim)

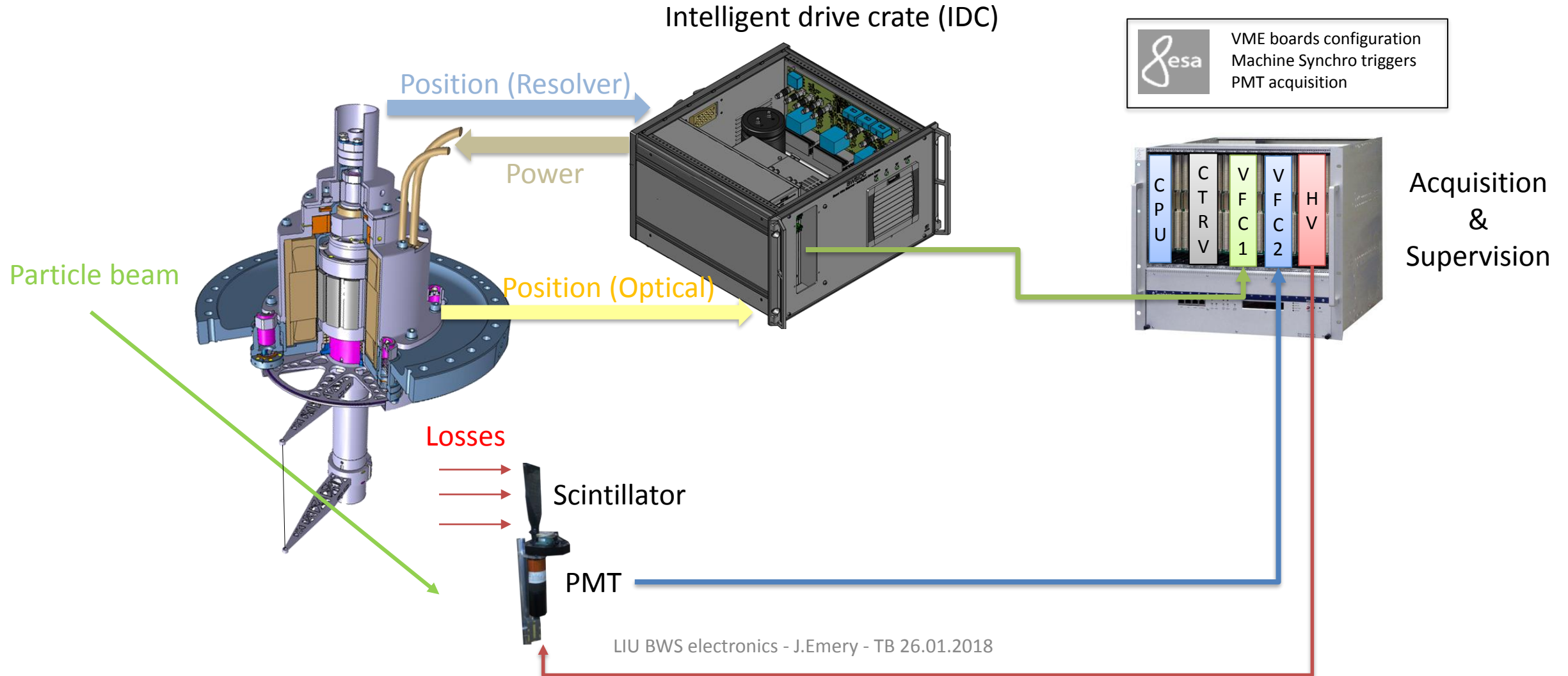


Motor phases current



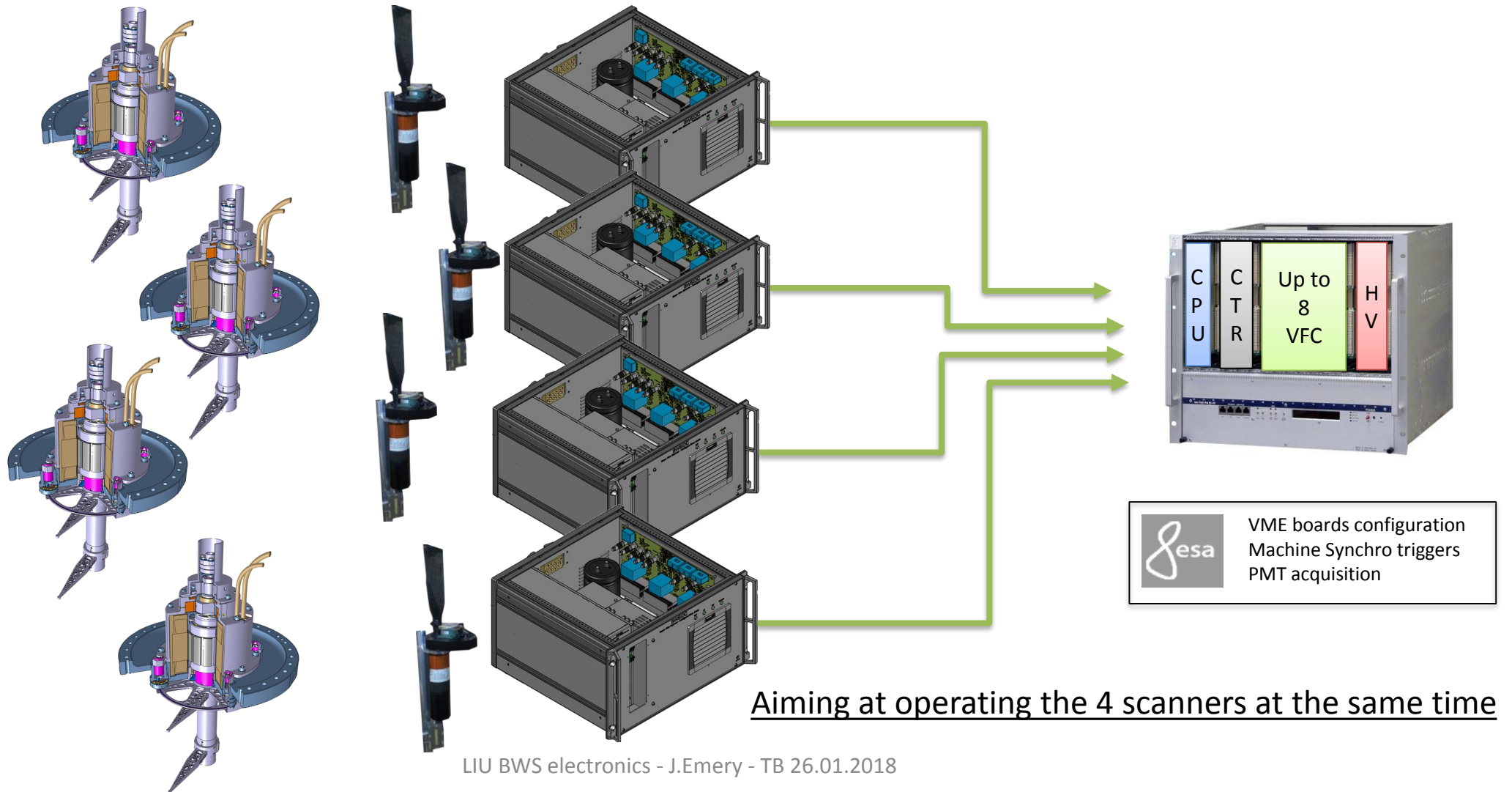


LIU Wire scanner system architecture





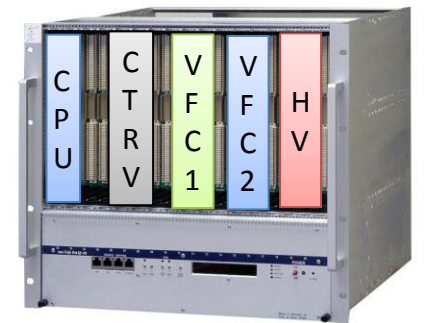
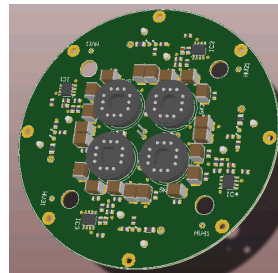
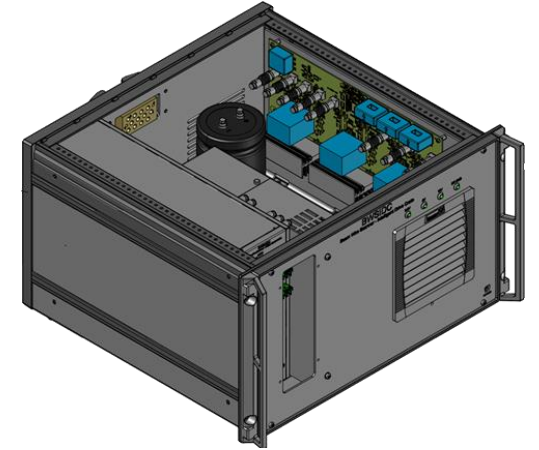
LIU Wire scanner system architecture





Hardware item list

- Scanner controller (IDC):
 - Stand-alone operation of the scanner mechanism
 - Custom design
 - Based on VFC board + 3 custom boards
- Acquisition and Supervision:
 - VME based system
 - 1 VFC to connect to the IDC
 - 1VFC + commercial mezzanine for PMT signals digitalization
 - 1 commercial HV module (ISEG)
- Sensor assembly:
 - Multi-PMT baseboard





Control and power electronics First implementation (for SPS and PSB)

Control Electronic

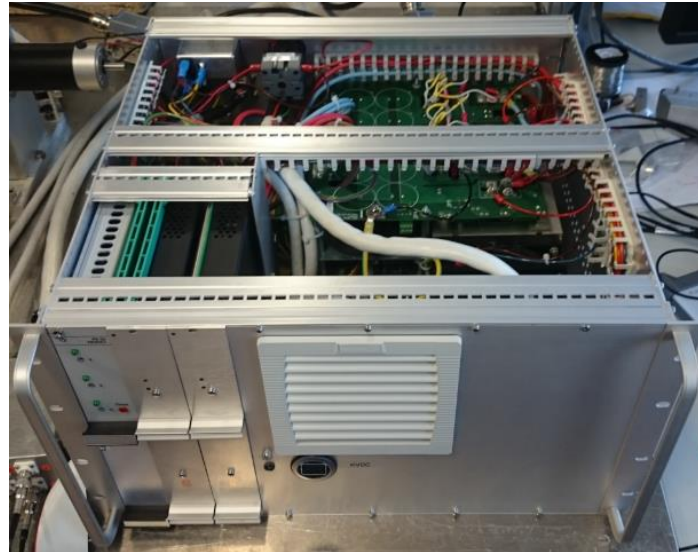
- 1 pcs. Altera development kit ARRIA V SoC
- 1 pcs. Mezzanie FMC board, CERN J.Emery



3U

Power Unit

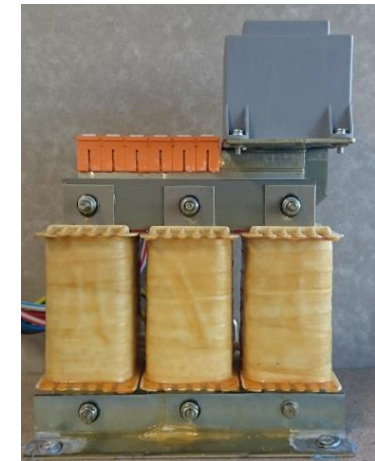
- 1pcs. Motor Inverter. Arcel
- 1Pcs. Measurement board,CERN L.Timeo
- 2pcs. DC bus Power Supply.DeltaElektronika



**6U
= 34.5Kg**

Filter

Filter,Schaffner



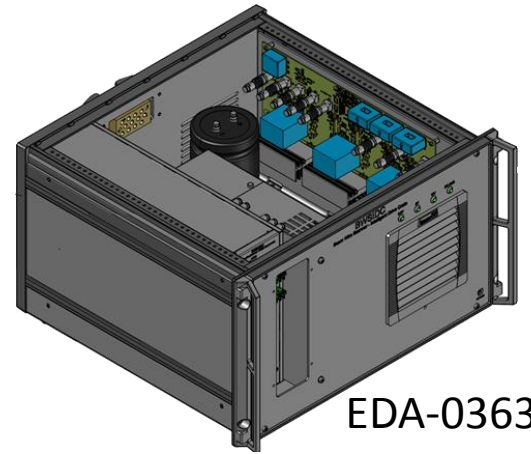
External
Filter

330*100*165mm

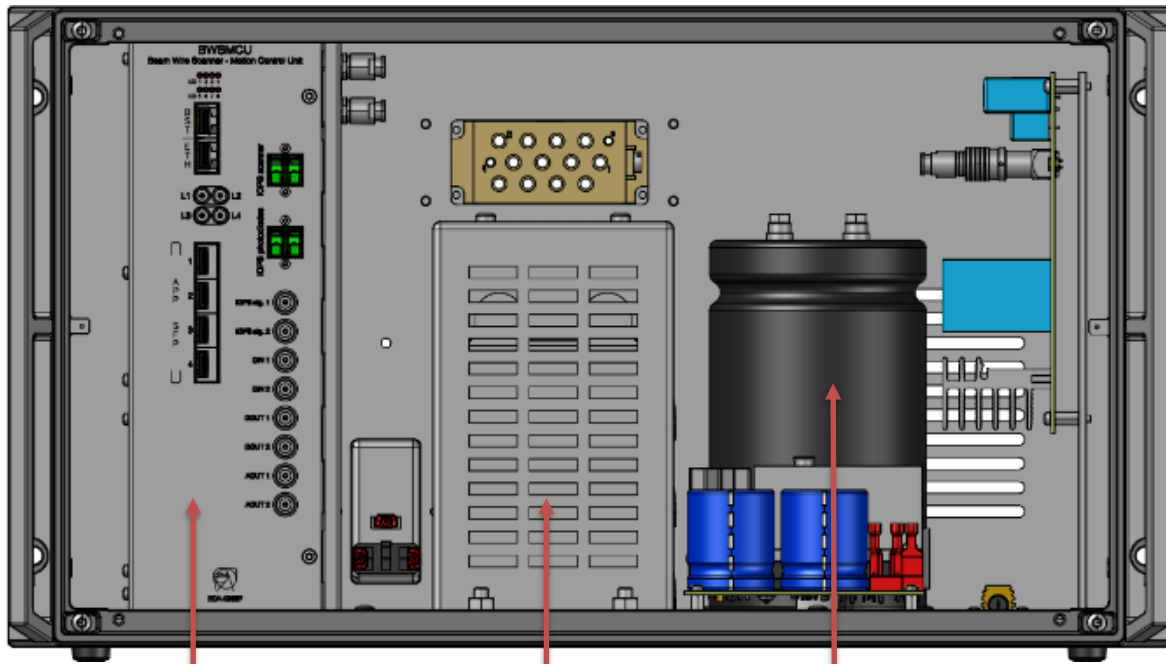


Intelligent Drive Crate (IDC)

6U, \approx 22Kg



EDA-03634



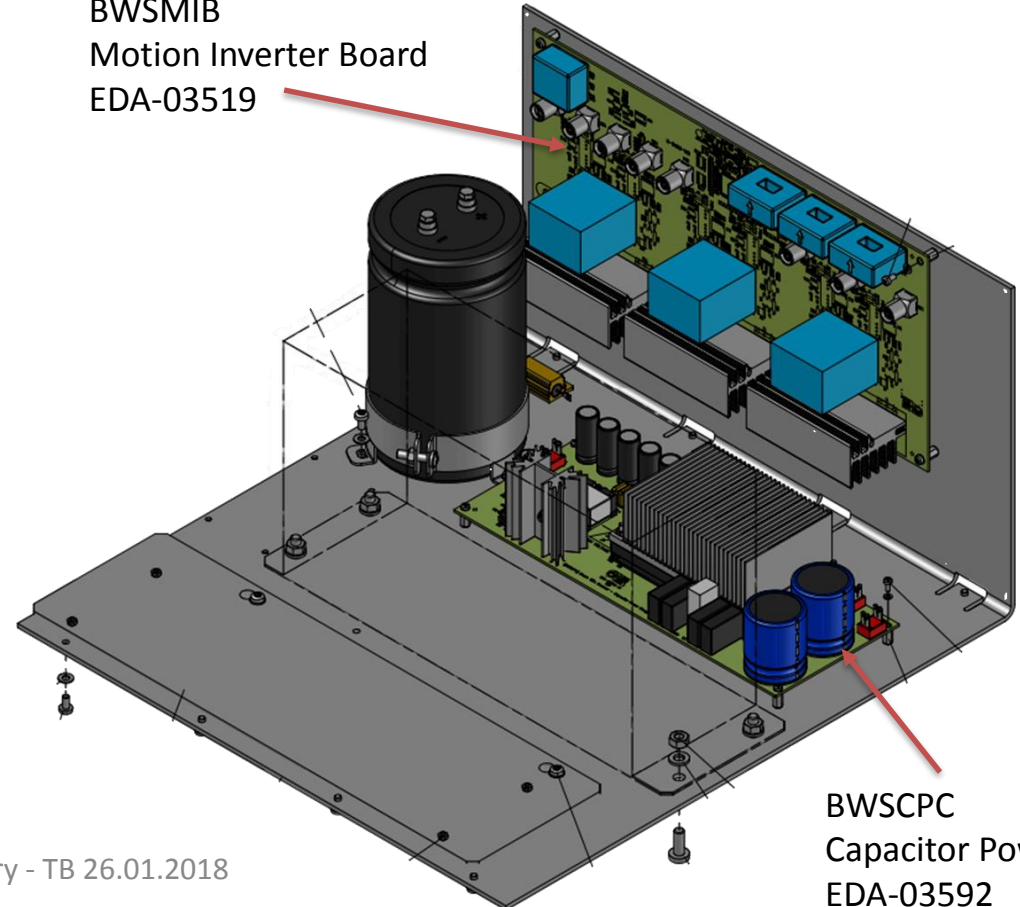
DC-BUS Capacitor

BWSMCU

Motion Control Unit
EDA-03697

Output filter "sinus"

BWSMIB
Motion Inverter Board
EDA-03519



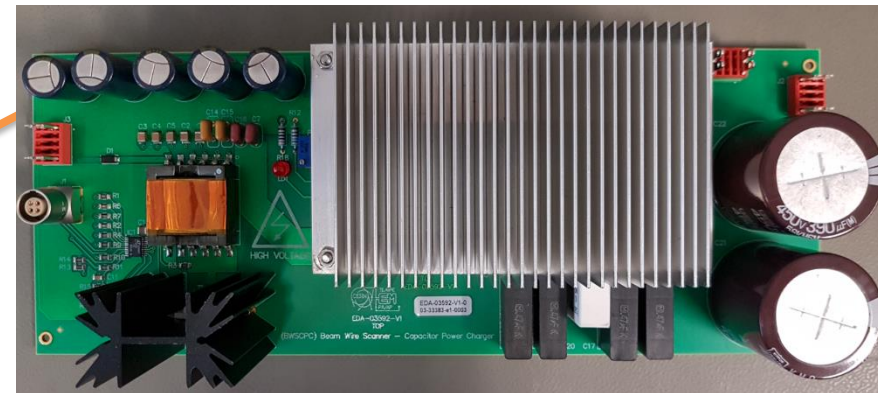
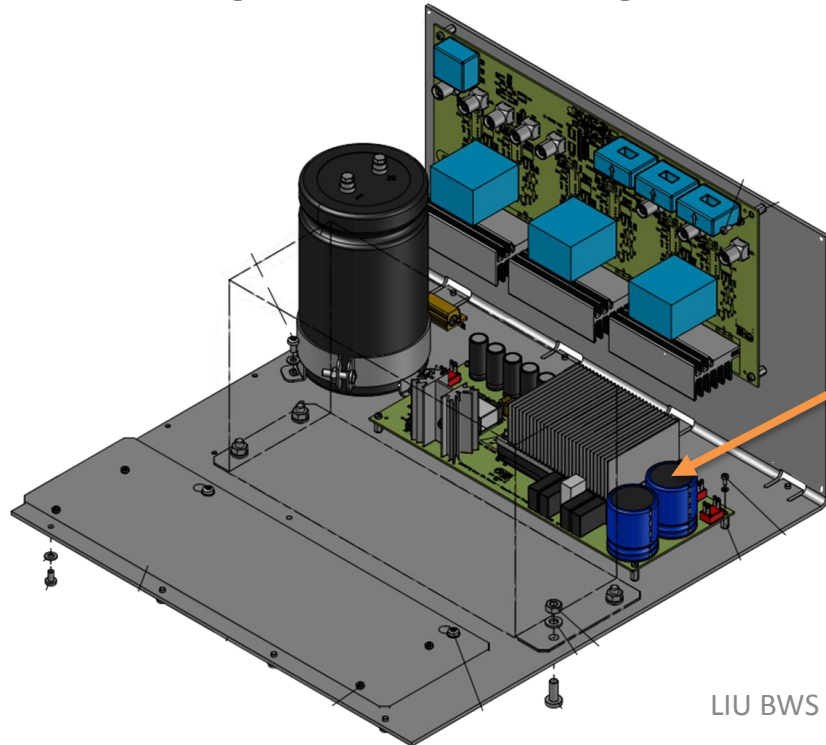
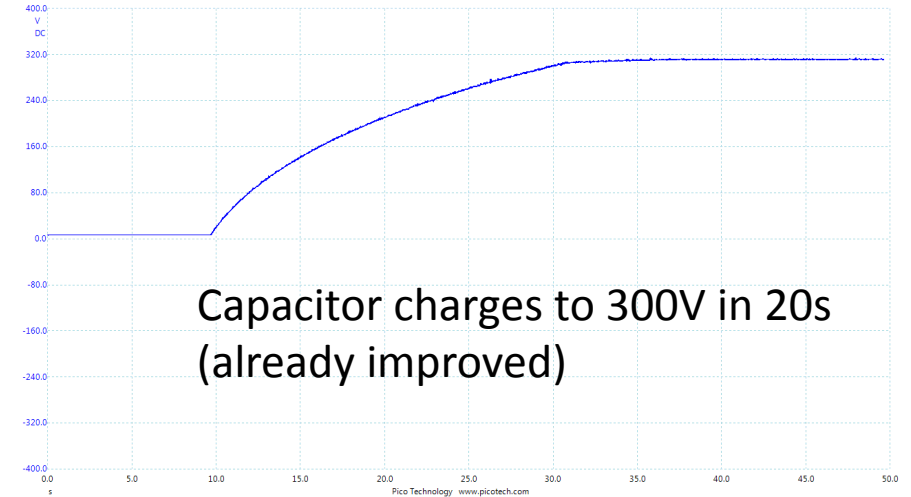
BWSCPC

Capacitor Power Charger
EDA-03592



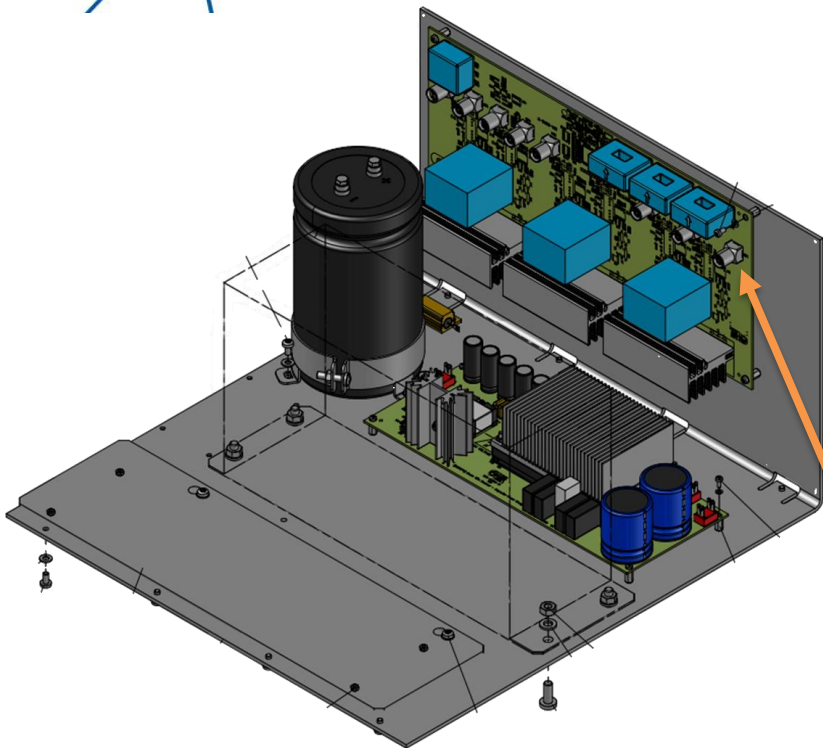
BWSCPC - Capacitor Power Charger - EDA-03592

- Charge DC-BUS capacitor up to 500V (was 400V)
- Replace the Delta Electronics 300V supplies (obsolete)
- Increase the charge current from 0.3A to 0.45A RMS
- In the future, increase current to 0.55A for shorter charging time (higher scan cycle rate)
- Version 2 being done at the design office

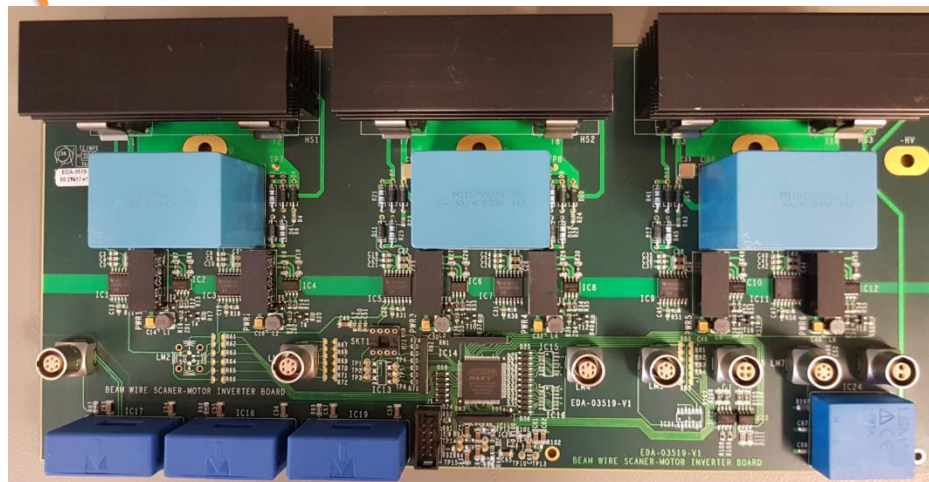




BWSMIB - Motion Inverter Board - EDA-03519



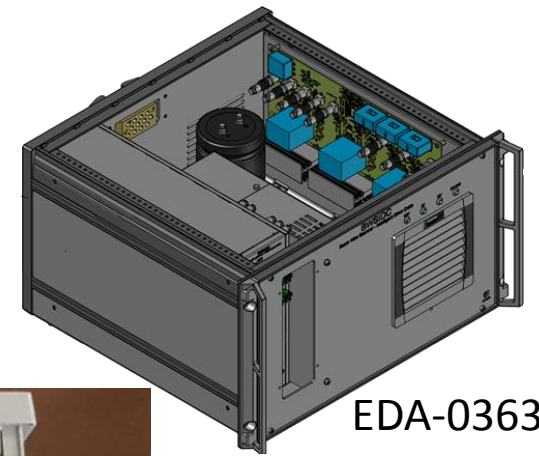
- Motor phases powering by chopping the DC-BUS (**PWM control**)
- Design for the wire-scanner repetition rate (~every few sec.)
To reduce size by 3 compared to off the shelf inverter
- CPLD based digital interface and controls
- Also replace DC-BUS control and measure card
- SPI based interface, IGBT protection, faults signalisation, PWM generation (tbc)
- Version 2 to the design office mid-February 2018





Intelligent Drive Crate (IDC)

IDC for external control system
"Dspace"

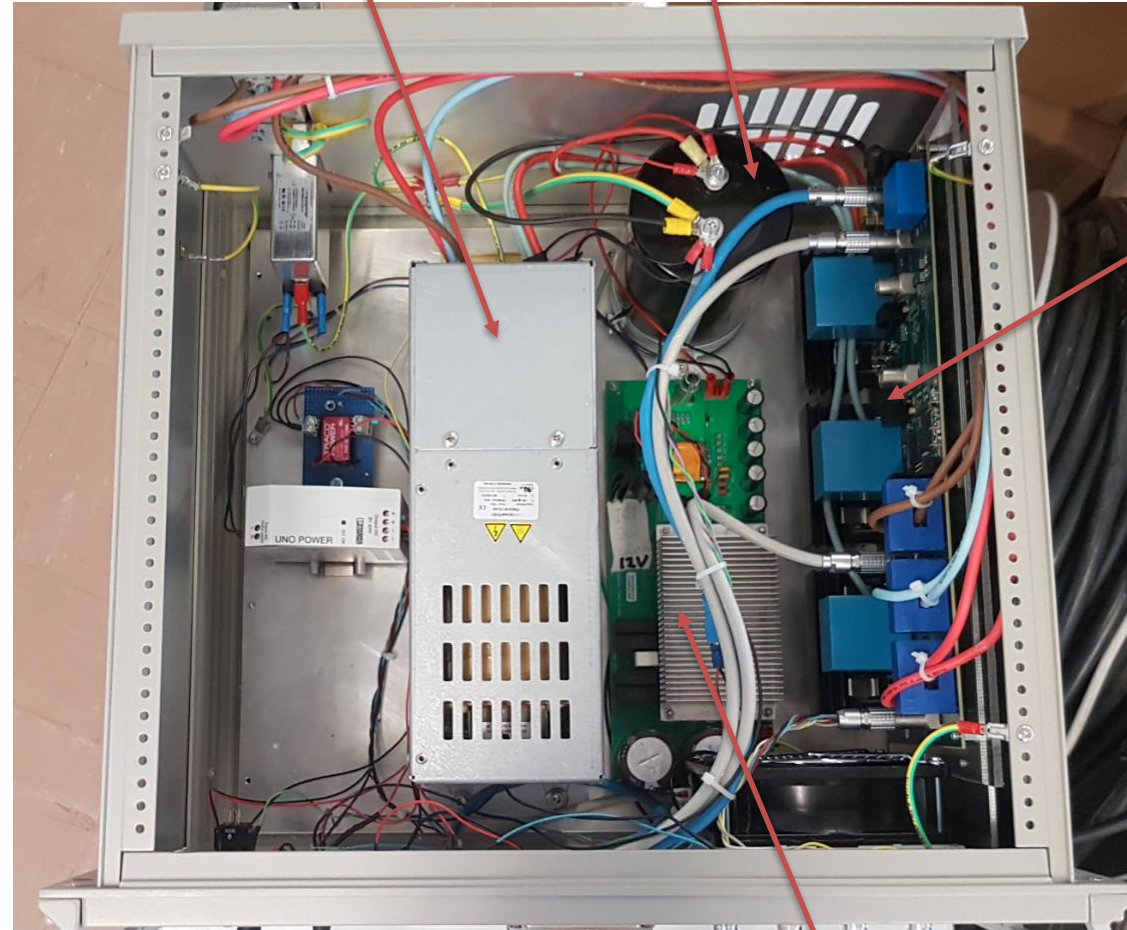


EDA-03634



Output filter "sinus"

DC-BUS Capacitor



BWSMIB
Motion Inverter Board
EDA-03519

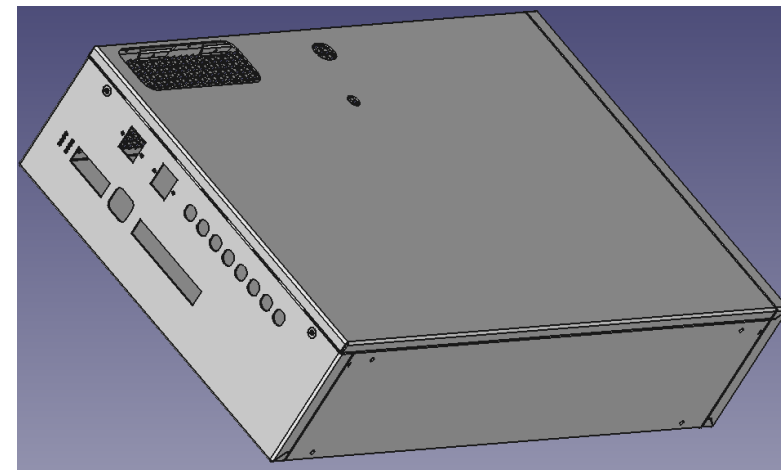
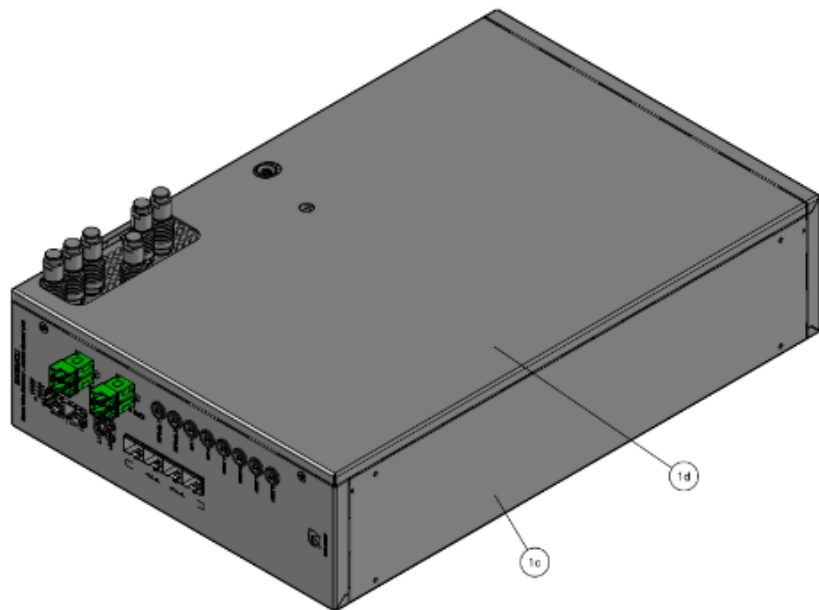
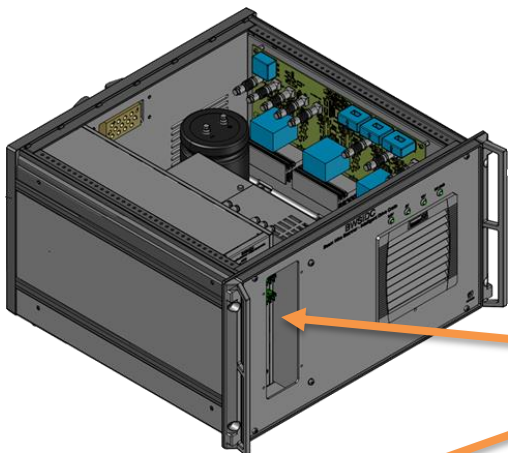


2 new Dspace
MicroLabBox
Received

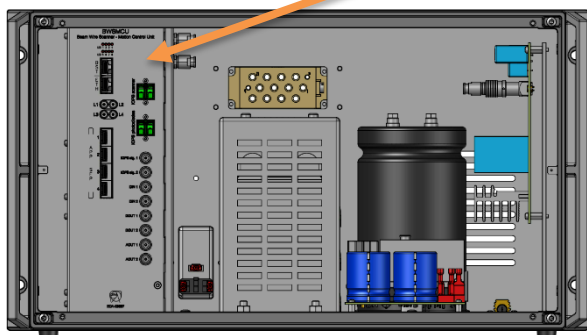


BWSMCU Motion Control Unit EDA-03697

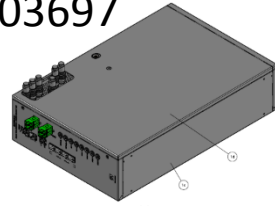
EDA-03634



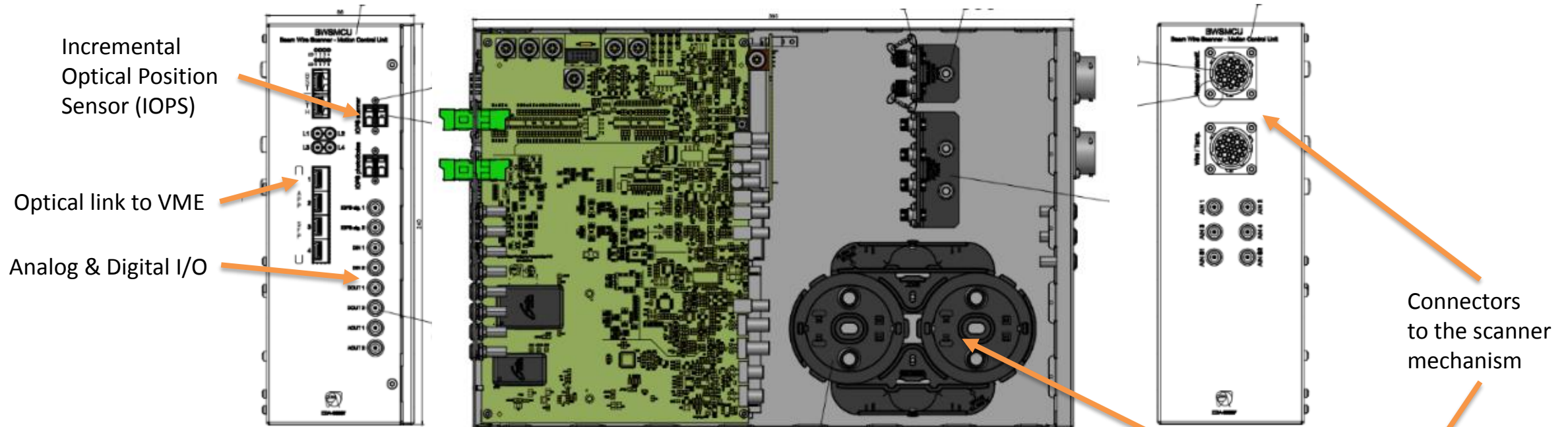
STEP MODEL



- Stand-alone control unit, external power supplies
- Ethernet for debug & Expert diagnostic
- Link to the VME using VFC to VFC serial connection
- Direct electrical and optical interfaces to the scanner
- Interfaces to the power stage (inverter)
- Numerous analog and digital I/O (isolated)
- Easy assembly and maintenance



Motion Control Unit (MCU)



VFC-HD - EDA-03133

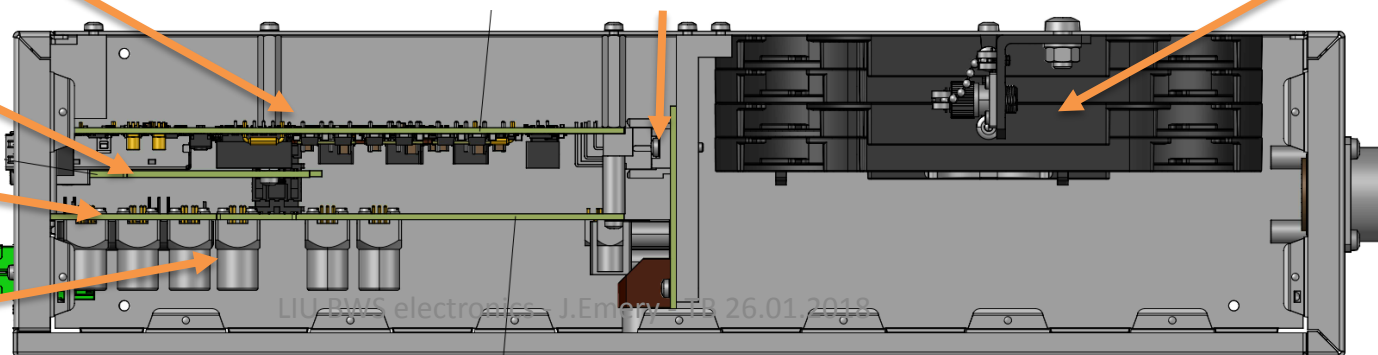
BWSVPA - VME Power Adapter
EDA-03698

Optical fibre components

BWSFHE - FMC-height-extender
EDA-03624

BWSAIF - Analog Interfaces FMC
EDA-03096

Connection to the power stage

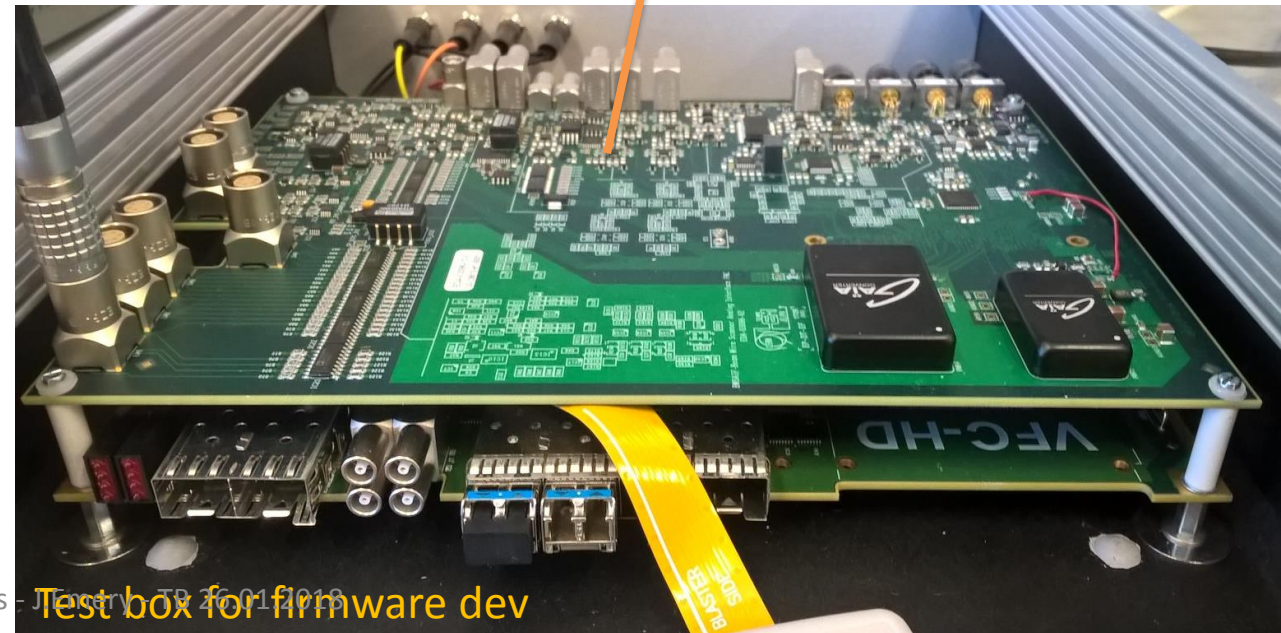
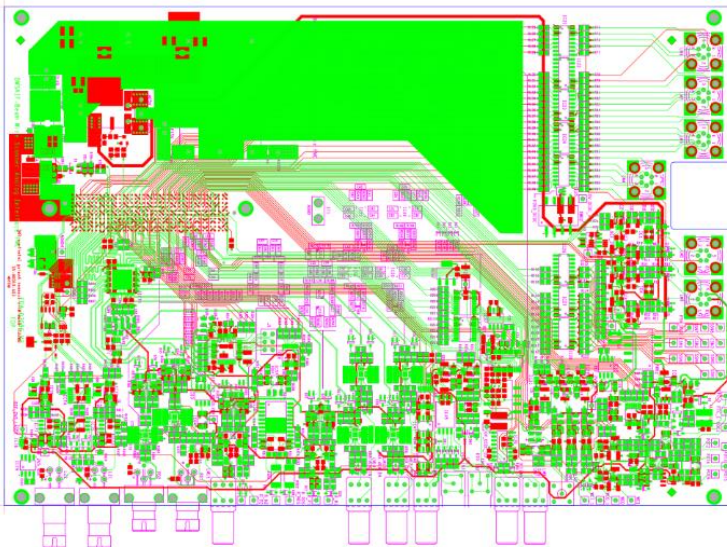
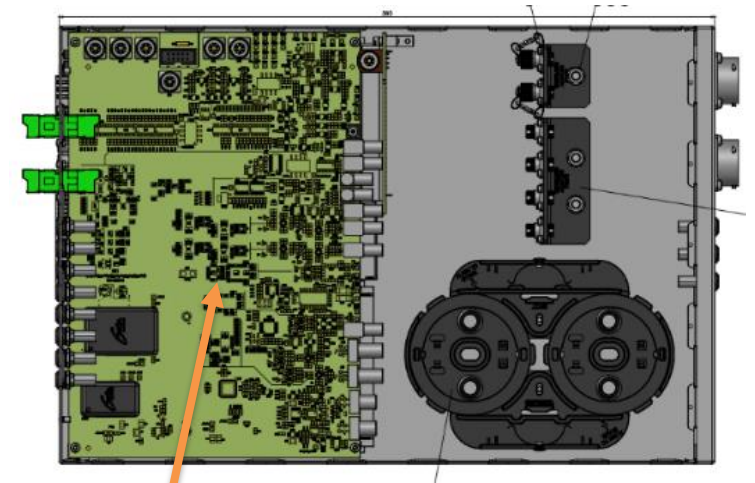




(BWSAIF)

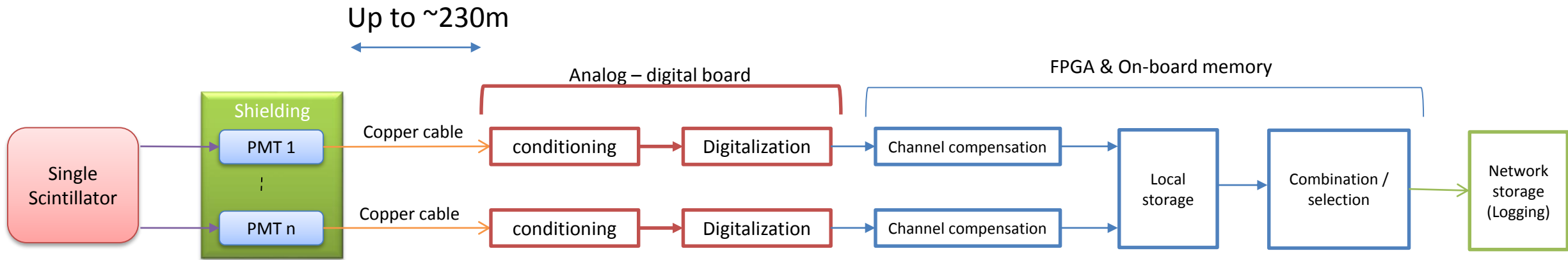
Beam Wire Scanner - Analog Interfaces FMC

- Interfaces to scanner sensors (Resolver, IOPS, Wire, PTC)
- Interfaces to the power stage (PWM, SPI, I and V)
- Too large mezzanine for the FMC standard on VFC-HD
- Custom FMC height extender
- Version 2 to the design office mid-February 2018





Secondary shower sensing



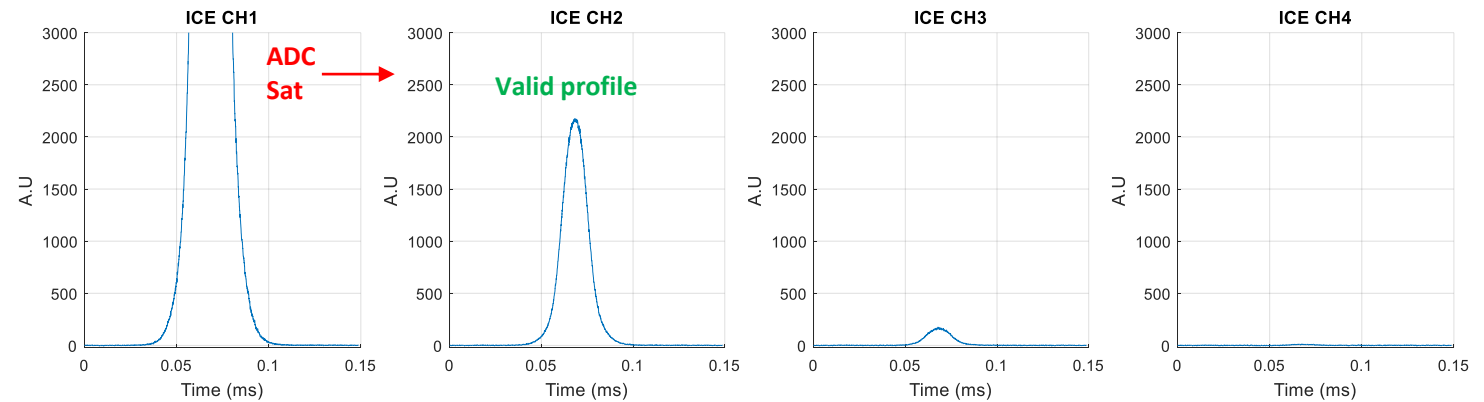
- Similar sensor as today: Scintillator + PMT
- Moving filters replaced by fixed filter and 4 PMTs
- Signal digitalization at the surface using direct digitalization on VFC
- Channel compensation, sensors combination and data reduction to be developed this year using field measurement (starting with scopes)
- Take advantage of the FBCT experience with similar architecture



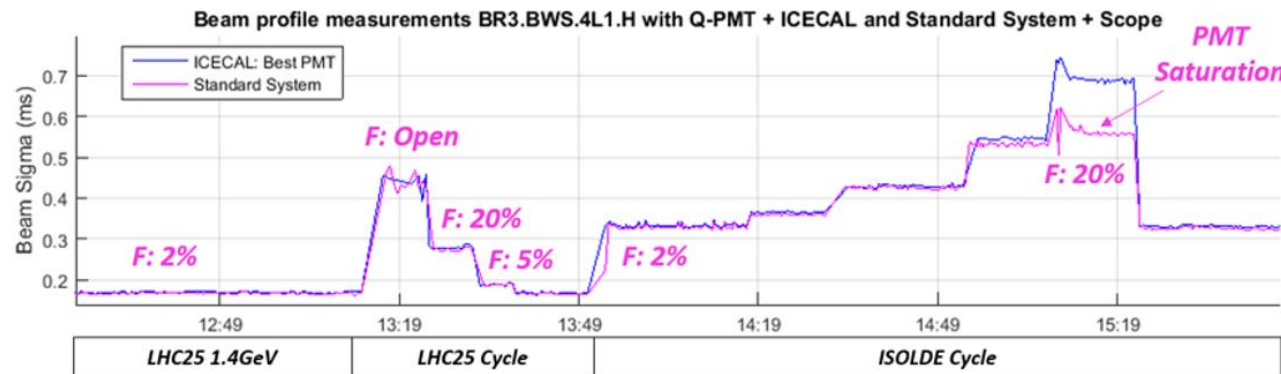
PSB Prototype Beam Tests: Results

HDR techniques evaluation: Multi-PM system

- Parallel acquisition of 4 channels with different dynamics adapted to PMT working points.
 - PMTs operate on linear range & with no saturation.
 - Static HV and Filter configuration: Operation in LHC25ns and ISOLDE cycles.
- Low noise tunnel digitalization with ICECAL Front-end & GBT link to surface.



Scanner SN:64 (2017/06/28 MD2375)

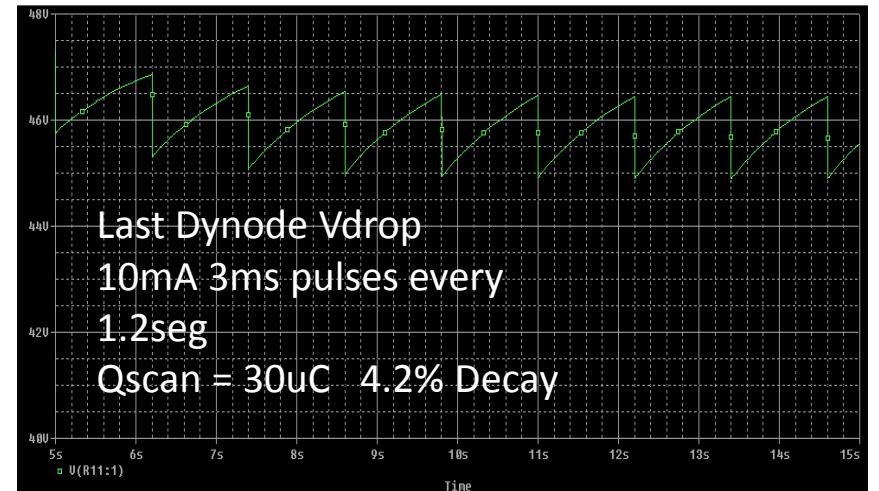
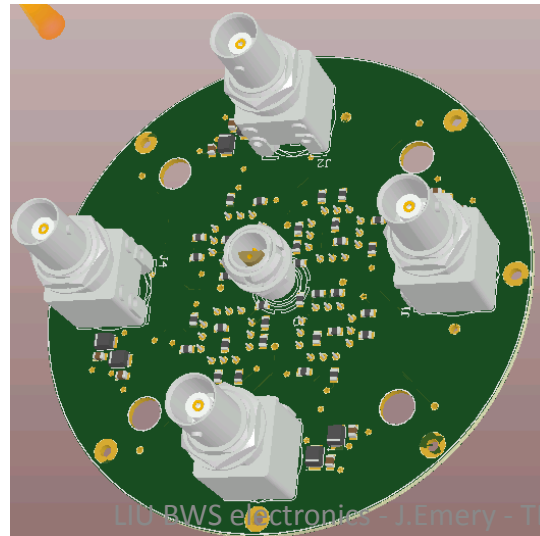
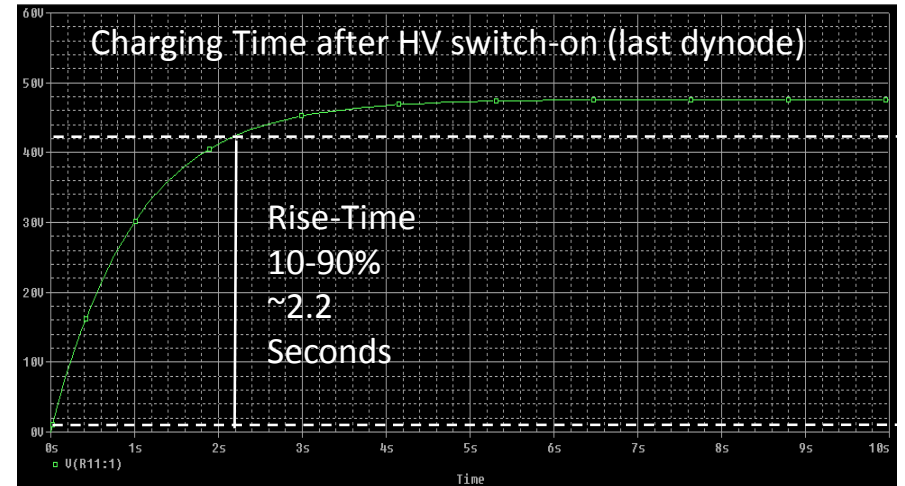
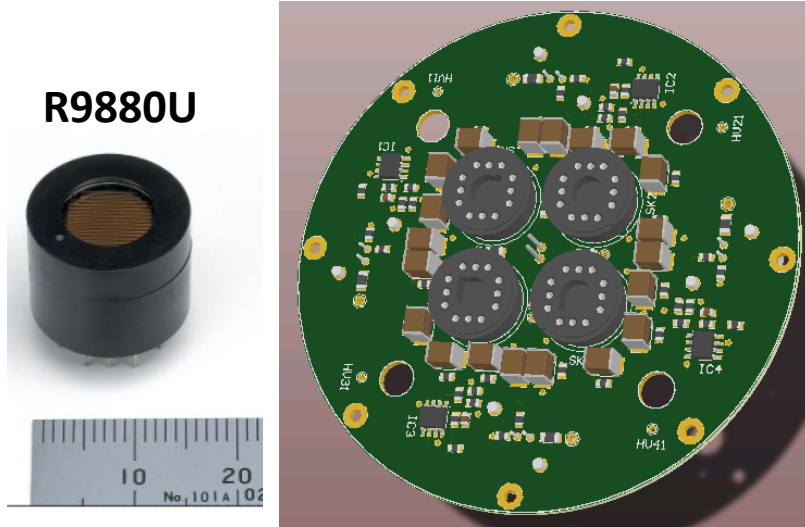


Scint. photon yield varied by 1e3:

- STD
 - Required filter changes
- HDR
 - Static configuration
 - PMTs saturation free
 - Redundancy
 - Detector x-validation



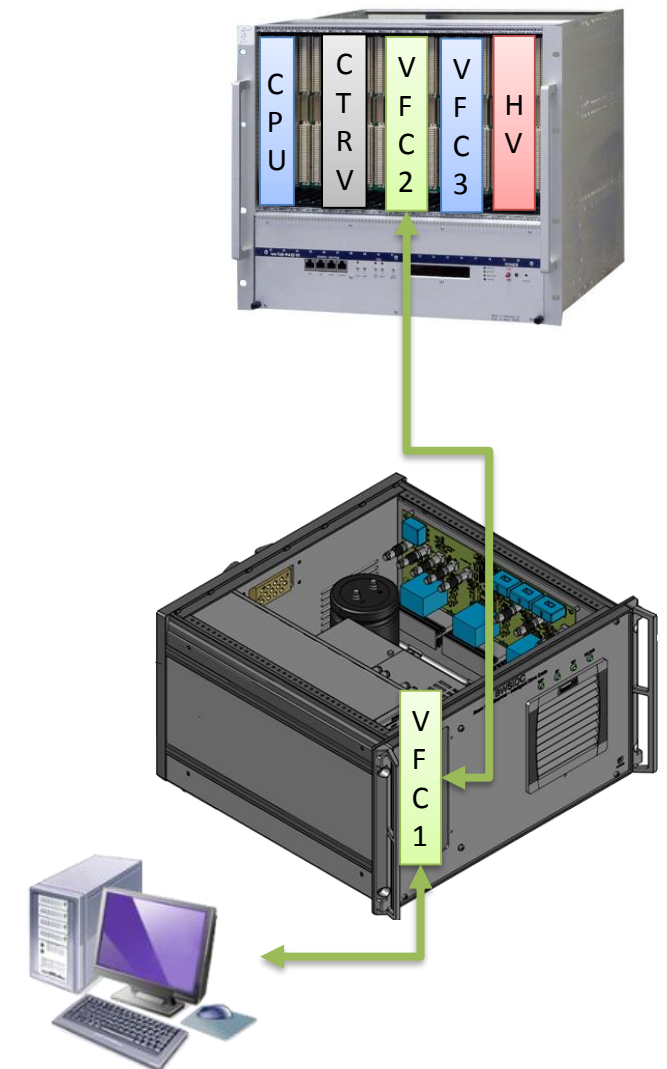
Secondary shower sensing based on Quad PMT assembly





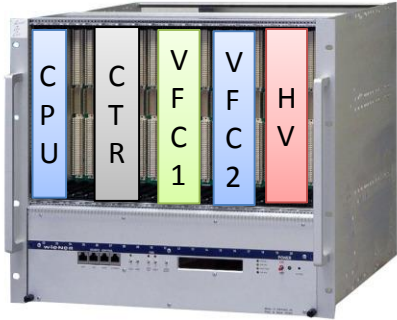
Firmware

- VFC 1 inside the drive (coding on-going):
 - Scanner motion, power stage, sensors (Resolver, IOPS, Wire, PTC) processing
 - Partial use of the existing code of the DevKit version (used in SPS and PSB)
 - Link to the power motor stage (ready)
 - Link to the VFC 2 using serial link cores developed by Cedric Vulliez (TS)
 - Link to distant expert application over Ethernet (collaboration to start in Feb)
- VFC 2 (starts March 2018):
 - Scan trigger, configuration and exposes motion and sensor data to the CPU
- VFC 3 (to be start soon):
 - PMT acquisitions and processing on 4 parallel channels, exposes data to the CPU
 - Record the 4 channels and decides which one to keep
 - Reuse code from other instruments under investigation (FBCT)
- CPLD of the motor power stage (coding on-going):
 - Powering sequence of the board, error management and components protection





Software



- One crate controls 4 scanners (8 VFC), but needs test for it:
 - Many use cases (data, repetition rate, processing)
 - Data size (PPM) and data transfer (VME and FESA)
 - Data fitting of large number of bunches
 - Potentially offline processing of the optical encoder (large data set)
- A first technical specification to be produced soon with detailed scenarios.
- Implementation could start when Firmware for the VME on-going (Mid-2018, to be agreed)



VME boards configuration
Machine Synchro triggers
PMT acquisition

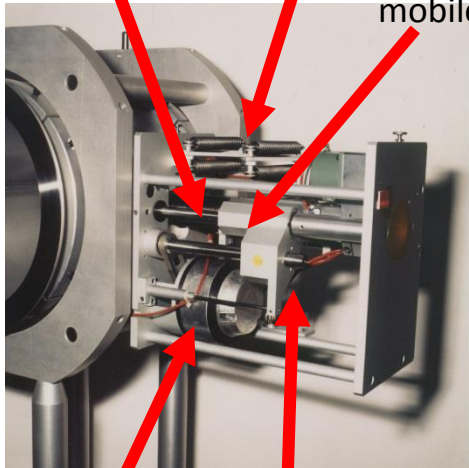


LIU control system for the Linear scanners LHC

Soufflet pour le transfert de mouvement entre l'air et le vide

Jeux de ressorts

Chariot mobile



Moteur rotatif DC

transformation de mouvement

Rotationnel a Linéaire

Potential reuse of the LIU control system for the linear scanner in the LHC:

- Motivated by limitations of
 - Today's architecture (scanner multiplexed)
 - Reliability issues (motor power stage, scanner staying IN)
 - Add high precision optical encoder (linear)
 - Various options without electronics changes
- From only firmware change to major mechanical change (still outside vacuum)

| | Description | mechanics | motor | cables | Firmware & control | Performance (to check) |
|---|---|-----------|--------------|----------|----------------------|----------------------------------|
| 1 | Keep same hardware | - | - | - | largest (PMSM to DC) | More reliability (power stage) |
| 2 | Change motor & resolver | low | DC -> PMSM | Pull new | medium | +Potentially faster speed |
| 3 | Change motor & ball screw | medium | DC -> PMSM | Pull new | low | +Faster speed |
| 4 | Change to linear motor (direct drive + lin encoder) | larger | DC -> linear | Pull new | low | +higher performance (stability?) |



Milestones for 2018

Milestone for the electronics control:

- Feb Design modification on various board
- Mar Start working on the VME side (TS)
- Apr Pre-serie production and assembly
Production test bench for power stage & charger (Stagiaire)
- June System validation using calibration bench (Bld. 867)
Motion optimization (to lower stress on mechanics and power stage)
Partial production launch of 30-40 units
- Sep System validation using installed PS scanner prototype
Complete production launch of 30-40 units

Milestone for the acquisition system:

- End 2017 Final acquisition baseline
- Sep 2018 Detector side validation (multiPMT concept) in all machines
- End 2018 Digitalization electronics validation with beam
Production launch of 20-30 units



CONTROL SYSTEM LAB TESTS



First board to board connections (2017)

VFC based control system

Motion Inverter Board



Capacitor Power Charger

Link between the [Motion Control Unit](#) and the [Motion Inverter Board](#) validated (Robust SPI)

Signal start DC-BUS sent from VFC-HD to [Capacitor Power Charger](#)

Link fully simulated in VHDL: - Transaction Level Modeling (TLM), random fault injection, reporting, etc...



Laboratory tests (January 2018)



Motor Bench

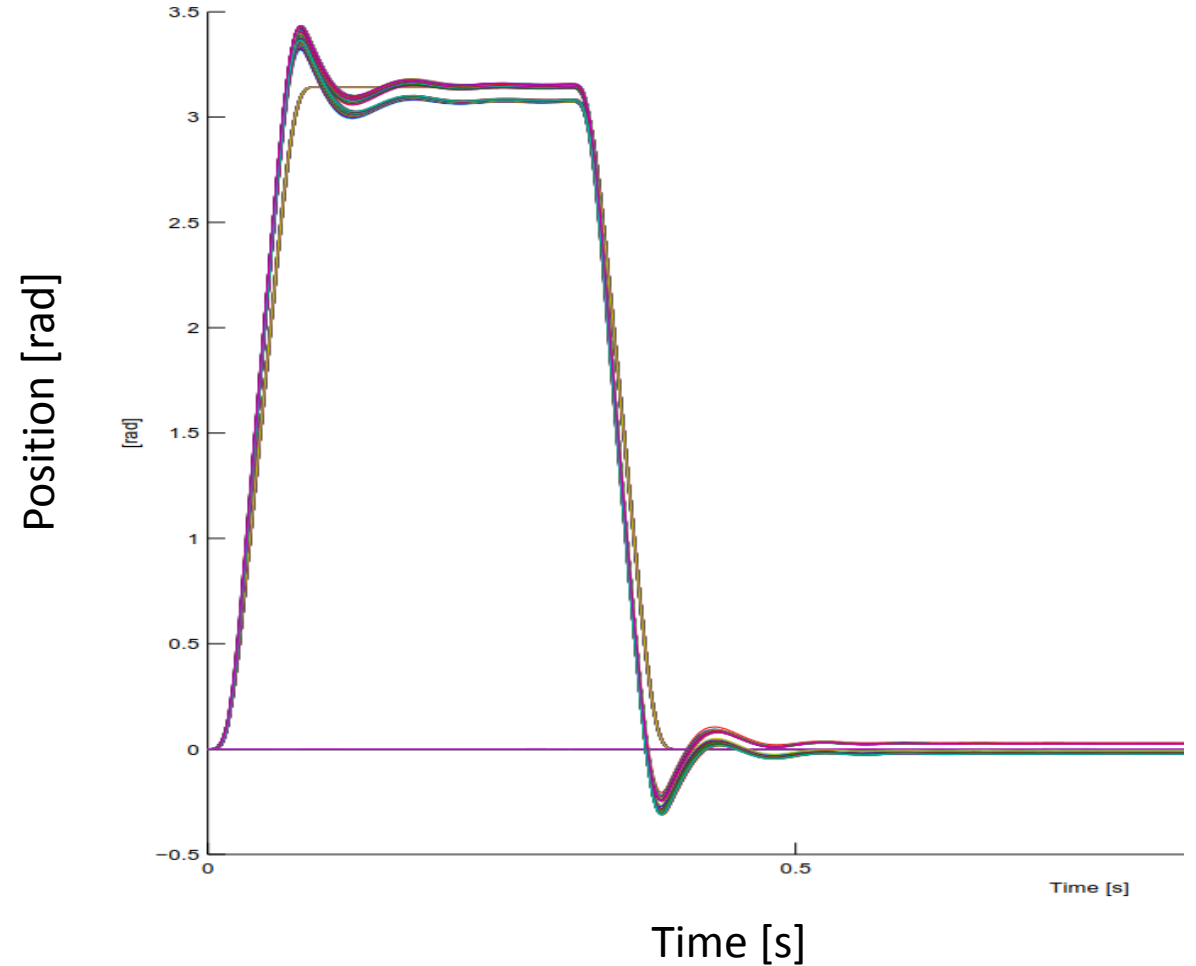
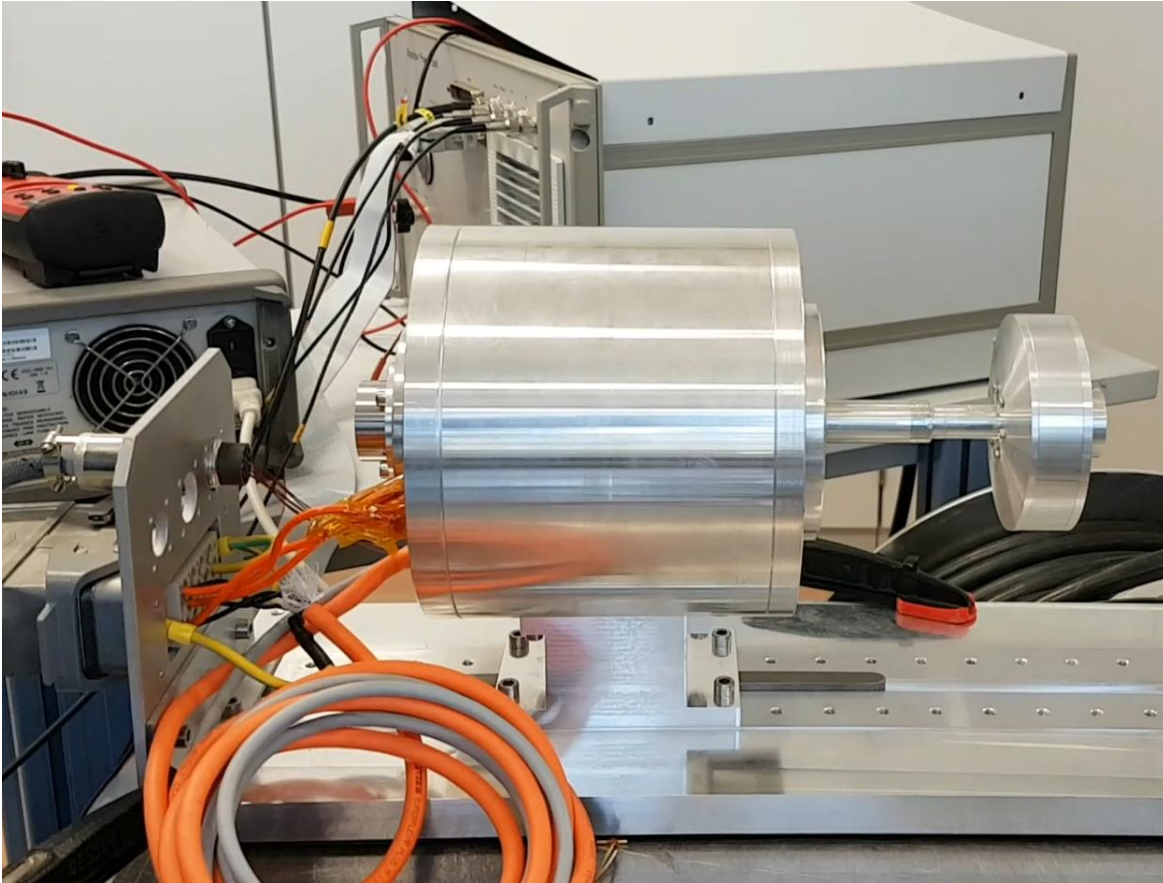
Dspace control system

VFC based control system

Intelligent Drive Crate (IDC)

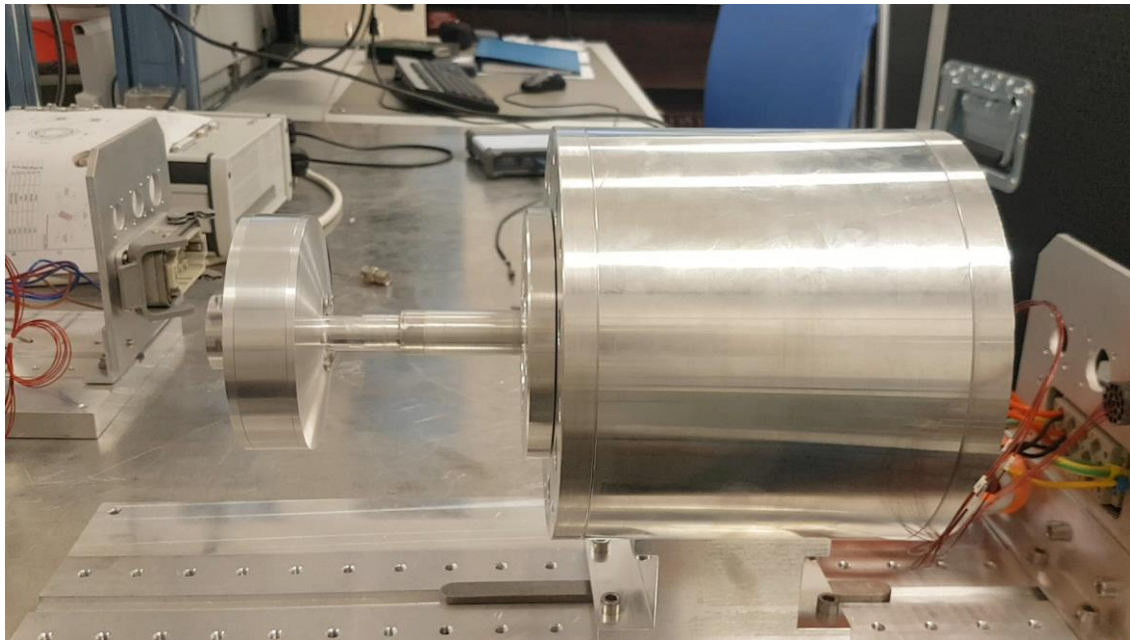


Laboratory tests: Custom power driver + Dspace control

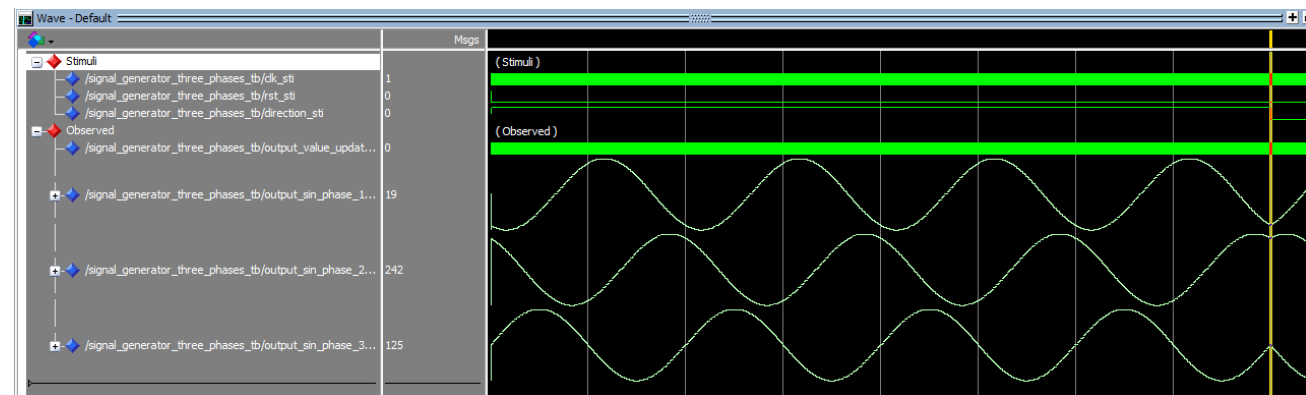




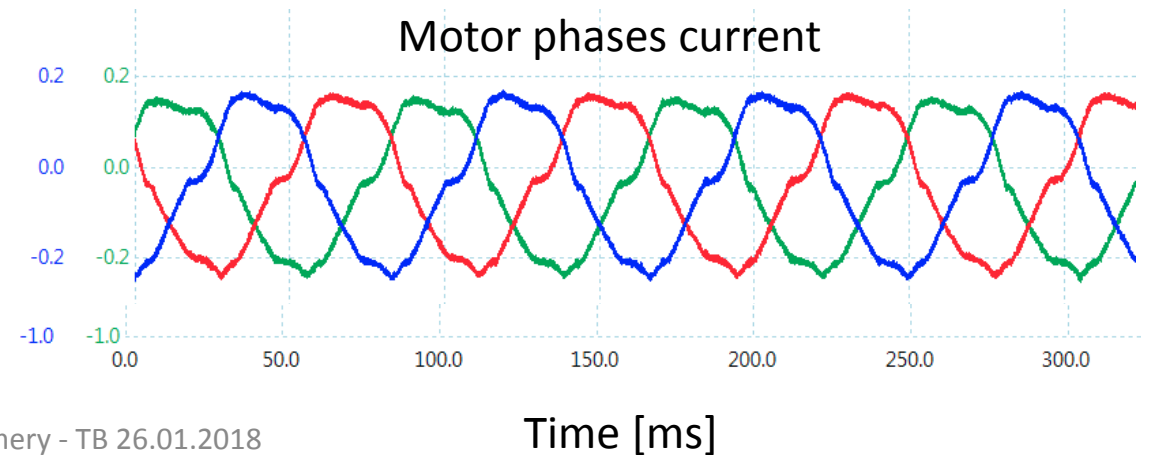
Laboratory tests: Custom power driver + VFC based control



3 phases control signals simulation in VHDL (Modelsim)



Motor phases current





ADDITIONAL SLIDES

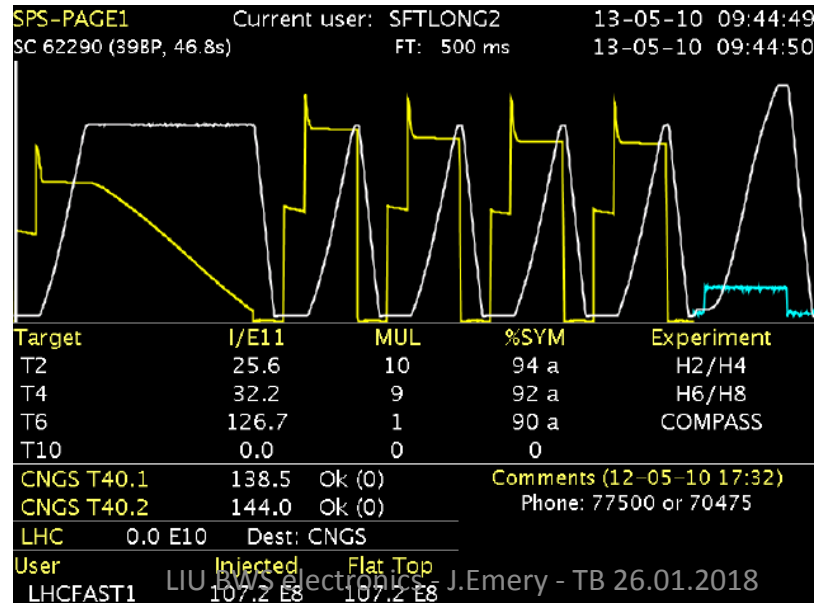
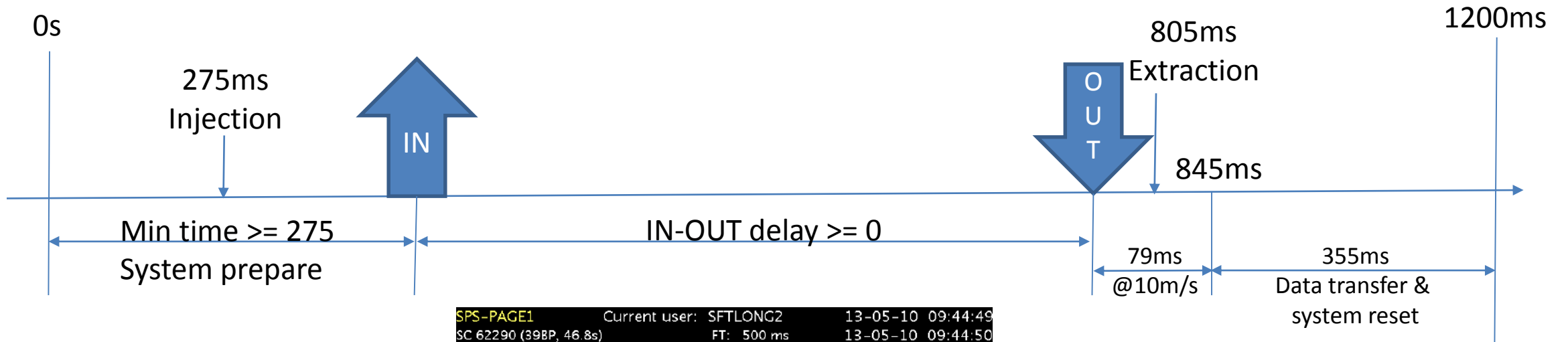


Functional system features

- Operate at various nominal speeds (1 m/s to 20m/s)
For the resolver position:
20 [m/s] -> 48 [ms] -> 767 pts
1 [m/s] -> 570 [ms] -> 9119 pts
- One scan cycle per basic period (one IN/OUT)
Adjustable in/out time, managed by the scanner itself
- Up to 5 scan cycle per user in the SPS
- Target repetition rate: every basic period (tbc)
- Scanner identification by the electronics
(for simplified calibration management)



One BWS cycle per PSB basic period (1.2s)





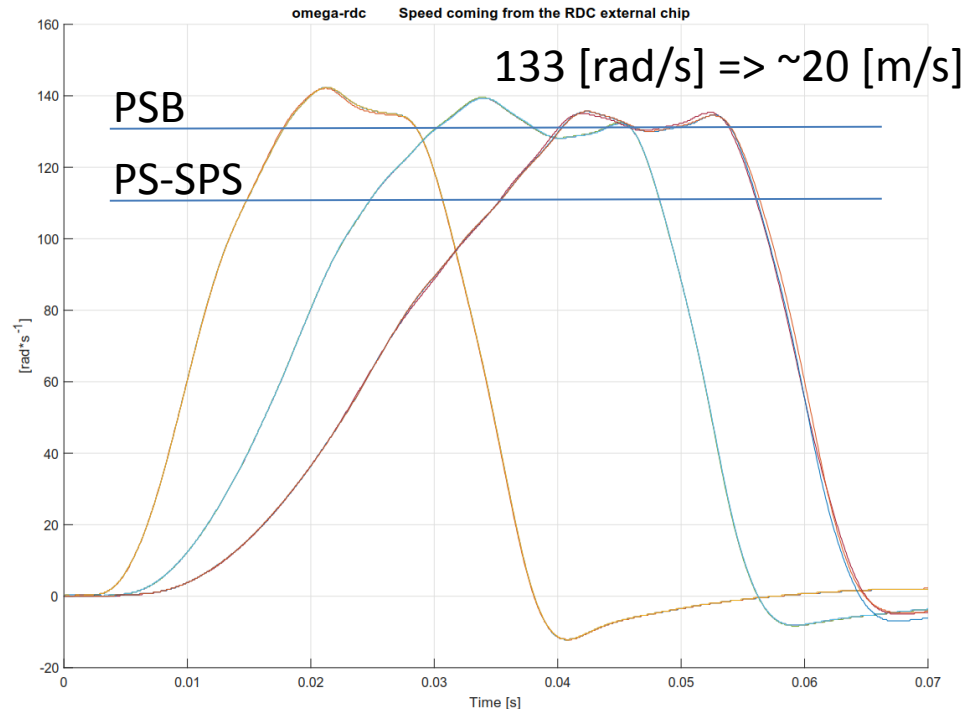
Hardware items status

| EDA | Designation | Description | Status | Planning |
|-----------|-------------|-----------------------------------|-----------------------|---------------------|
| EDA-03592 | BWSCPC | BWS – Capacitor Power Charger | V1 – tested | V2 at design office |
| EDA-03519 | BWSMIB | BWS – Motor Inverter Board | V1 – under test | V2 for mid-February |
| EDA-03096 | BWSAIF | BWS – Analog Interface FMC | V1 – under test | V2 for mid-February |
| EDA-03624 | BWSFHE | BWS – FMC Height Extender | V1 - tested | V2 at design office |
| EDA-03698 | BWSVPA | BWS – VME Power Adapter | V1 to test | |
| tbd | BWSPSA | BWS – Particle Shower Acquisition | First design ready | V1 at design office |
| | | | | |
| EDA-03634 | BWSIDC | BWS – Intelligent Drive Crate | V1 under construction | |
| EDA-03697 | BWSMCU | BWS – Motion Control Unit | V1 under construction | |



Motion performance optimisation (2017 studies)

- First motion strategy investigation this year (2017)
- Next step, impact evaluation on the scanner precision (2018)



Angular speed during a measure cycle, 'IN' part

Asymmetric motion strategies:

First to second:

Longer stroke and \sim acceleration / 2

First to third:

Longer stroke \sim acceleration / 3

110 [rad/s] for SPS

Motor design (nominal spec)

Max \sim 160 [rad/s] => 29[m/s] tang.





Motion performance optimisation (2018 studies)

- Study of different motion strategies:

- Lower the stress on the scanner mechanics, while keeping the nominal speed.

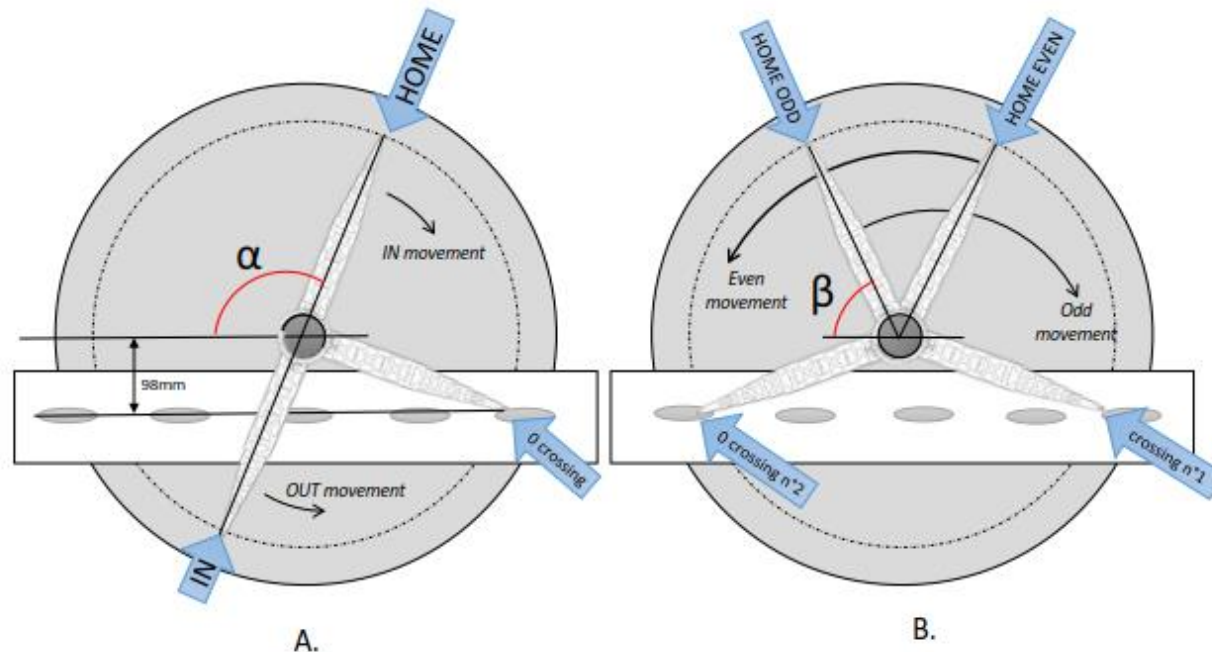
-

- Evaluate the impact of suppressing the constant speed (to lower eventual wire vibration).

-

- Increase the nominal speed to unsure a high projected speed.

=> Effect on the accuracy/precision of the scanner to be answered in 2018.



A. Classical approach

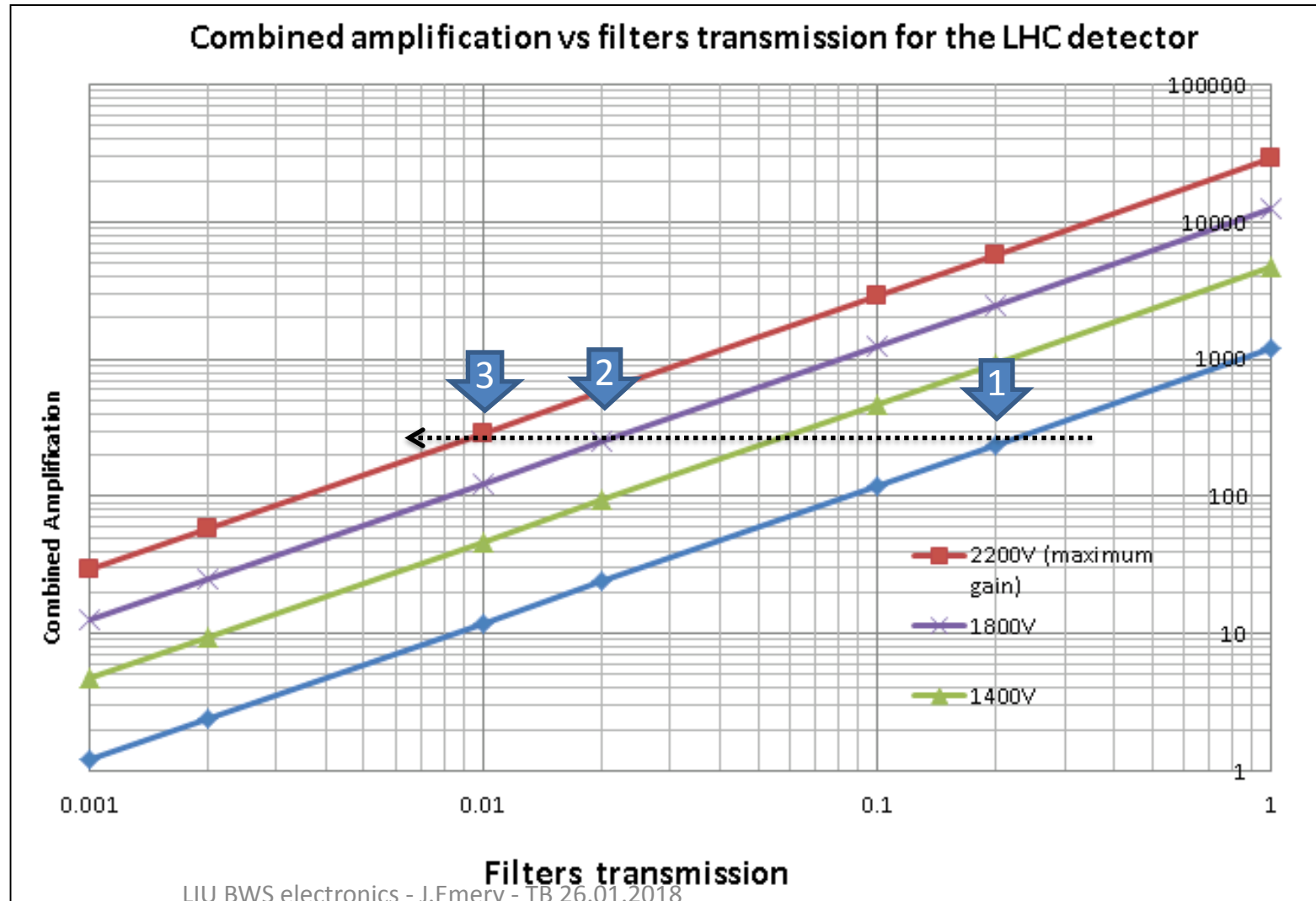
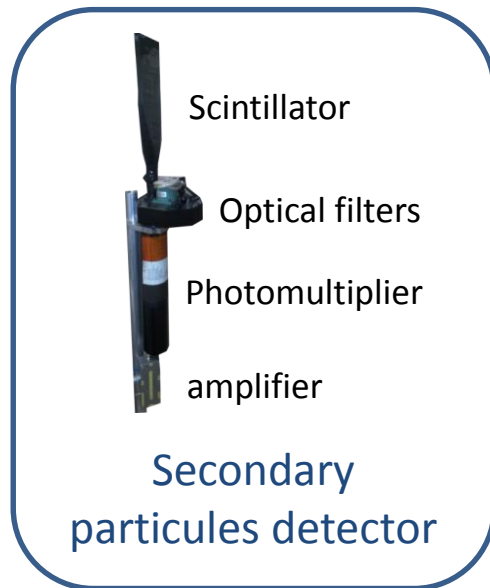
B. 2 crossing strategy:

Time between crossing 1 & 2: 15 [ms]

=> Potentially useful for operation

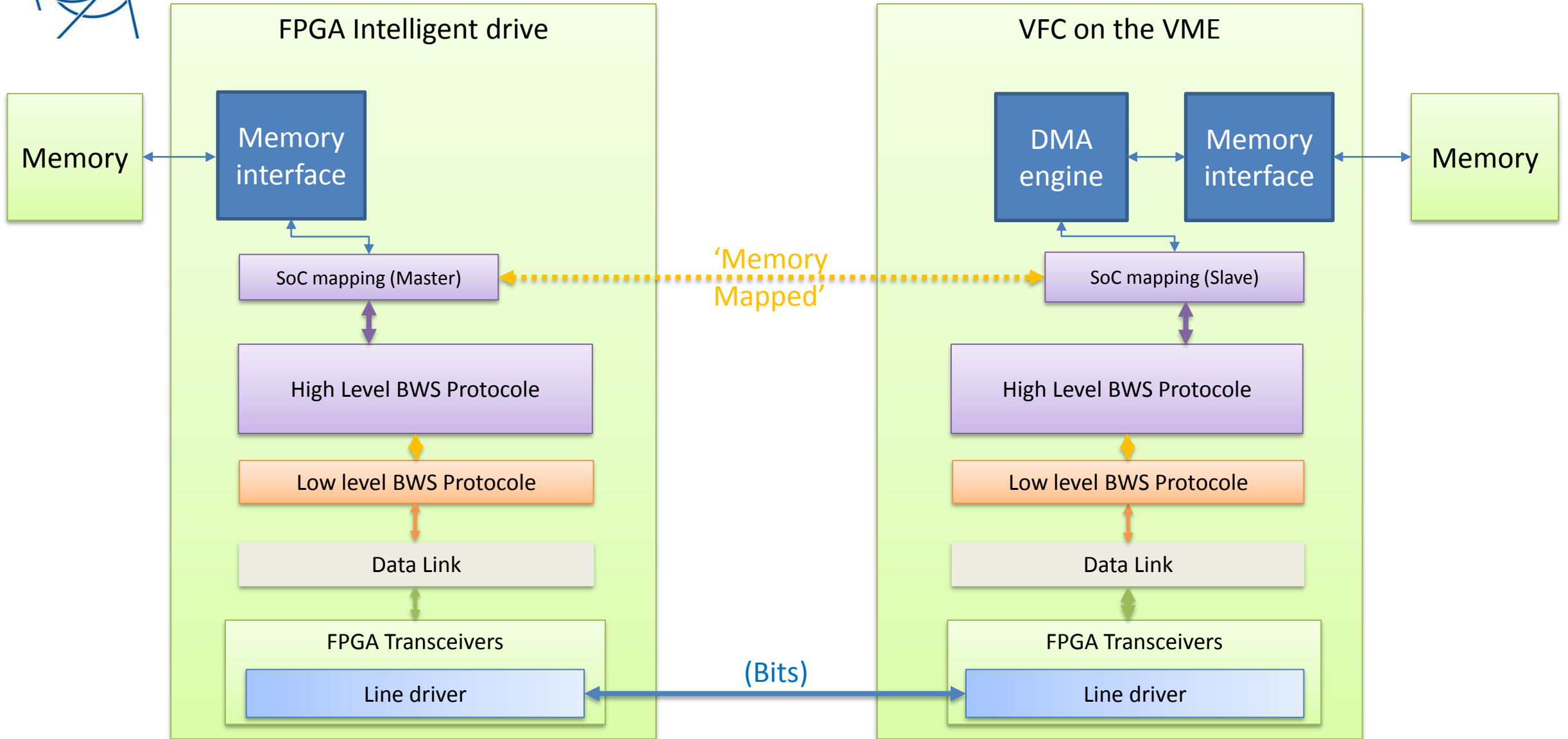


Secondary shower sensing





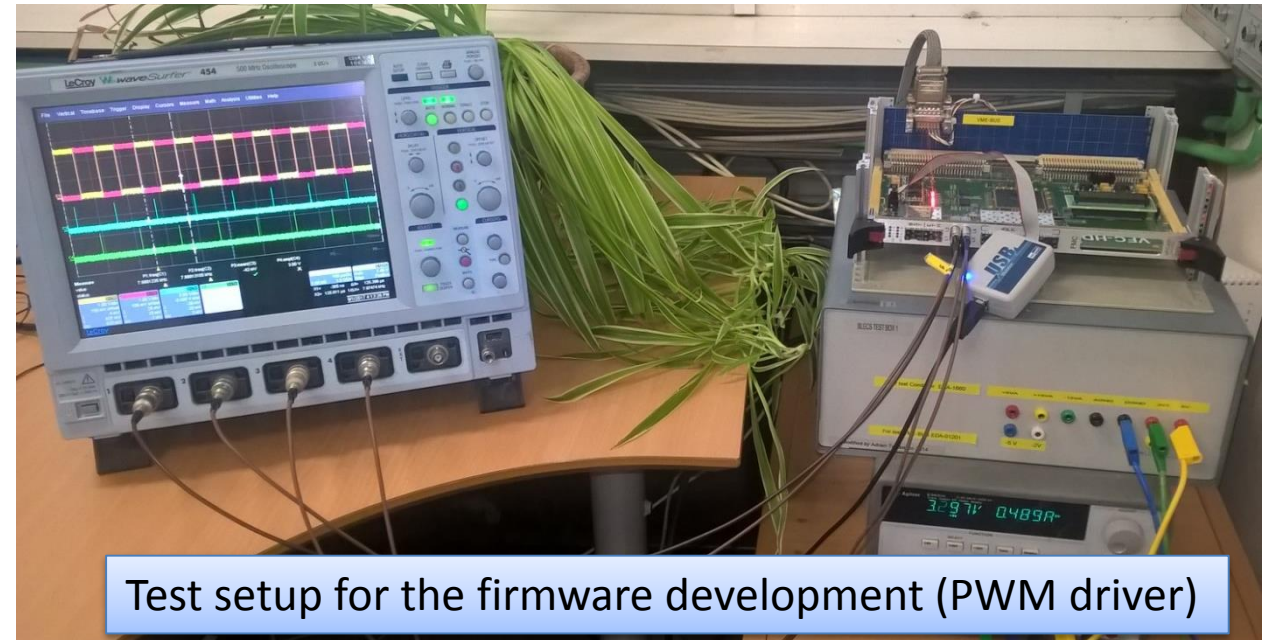
Data collection after a measurement



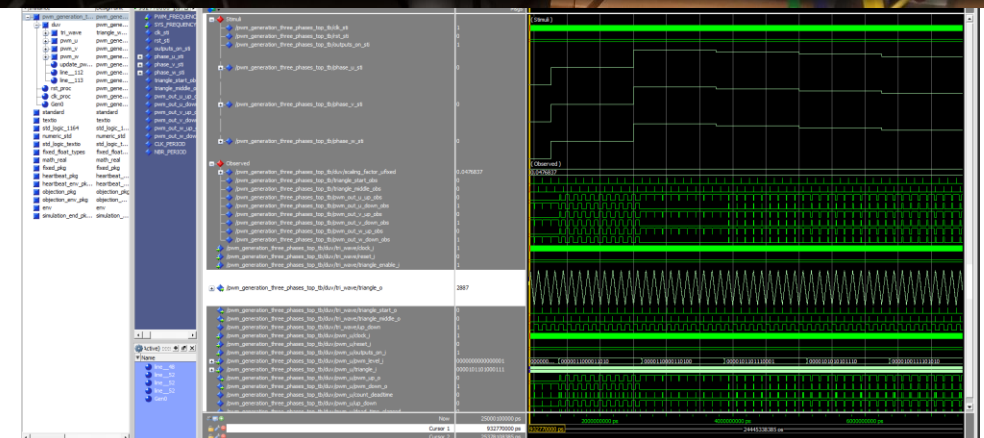


Electronics developments: VFC firmware

- Setup in the office for stand alone use (no VME backplane)
- Already testing first interface to the power board (see picture)
- Development on-going to be able to tests new coming mezzanine
- Code from the SPS prototype to be partially rewritten for reliability, efficiency and cleanness of the code
- VFC specific interfaces to be written or reused from other on-going projects



Test setup for the firmware development (PWM driver)



VHDL simulation of the new code



BWSAIF - Analog Interfaces FMC – Board validation tests

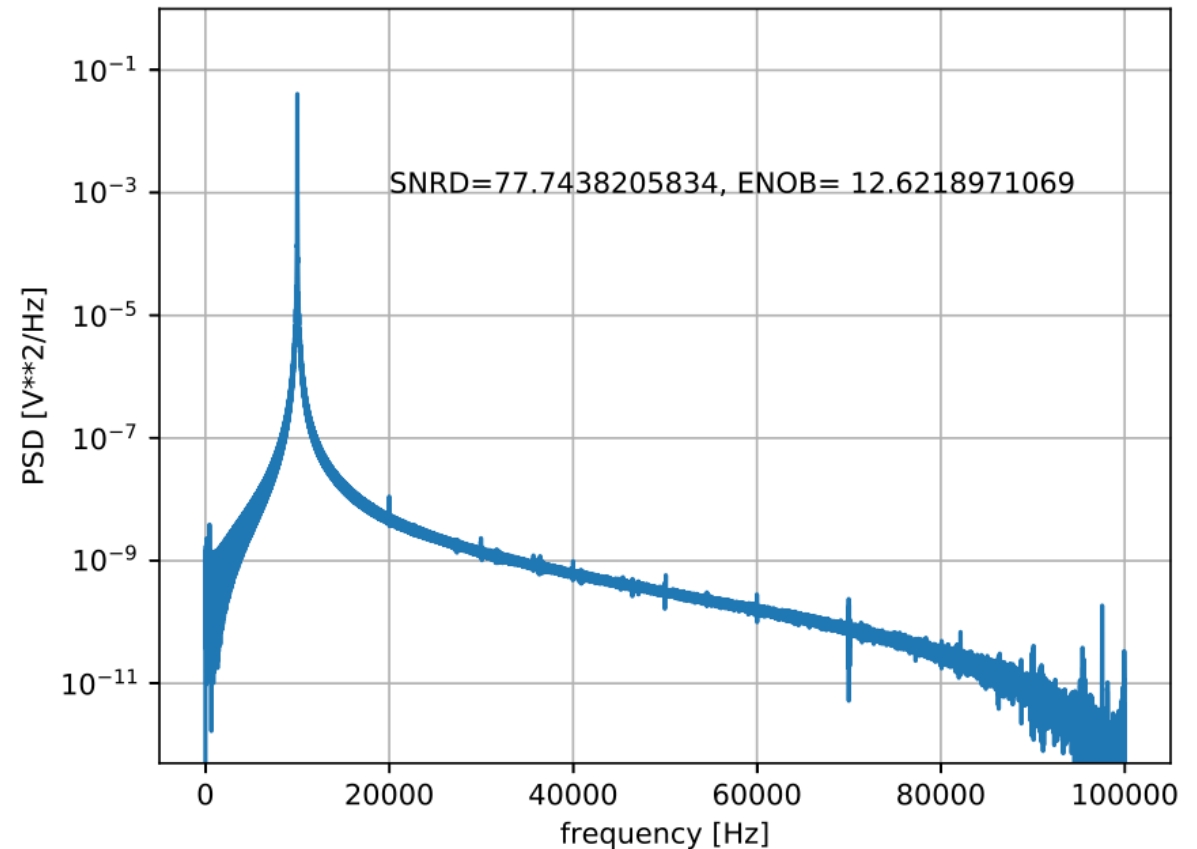
Part functioning:

- Power supplies
- Isolated digital I/O
- Isolated interfaces to the inverter
- Scanner Serial number interface
- Slow ADCs for the inverters

To do:

- Resolver interface
- DACs
- Fast ADC
- High res ADC

Gen_10k_SINUS_P_N_1V_AdvV.mif --- Power spectral density using Periodogram method



New version needed:

Slot schedule in the design office December 2017

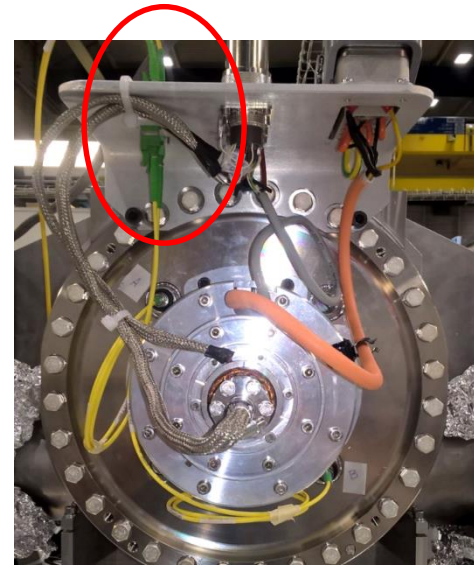
Power Spectral Density

ADC 16 bits dedicated to the measure
of one motor phase current

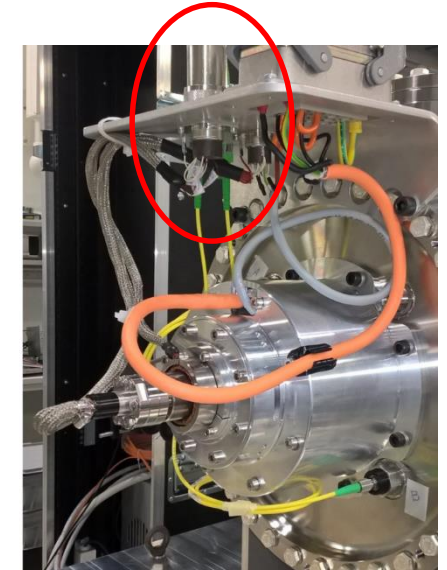


Serial number assignment and reading from the surface

- Hardware encoding of an unique serial number
- Cabled on the scanner connector (9 bits of information)
- Red from the surface electronics at any time
- Could be red automatically during the calibration process
- Calibration tables will have this number referenced in the files
- Will be used to unsure to correct assignment of the calibration table
- Remove any doubt over time
- Can be used by the electronics to adapt its behavior in function of the machine



BSM19-15



BSM19-7

| Machine (3 bits) | Version (2 bits) | Scanner number (4 bits) |
|------------------|------------------|-------------------------|
| 0. LAB | 0. Rev 0 | 0 - 15 |
| 1. PSB | 1. Rev 1 | |
| 2. PS | 2. Rev 2 | |
| 3. SPS | 3. Rev 3 | |
| 4. LHC | | |
| 5. --free | | |
| 6. --free | | |
| 7. ISS | | |