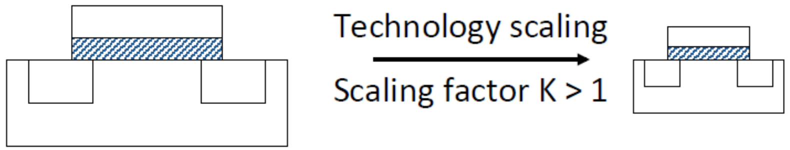
Technology Trends, Wishes and Dreams

Detection and Imaging related

Reminder

CMOS Scaling

Constant Electric Field Scaling



<u>Primary scaling factors:</u>

Tox, L, W, Xj (all linear dimensions)	$1/K$
Na, Nd (doping concentration)	K
Vdd (supply voltage)	$1/K$

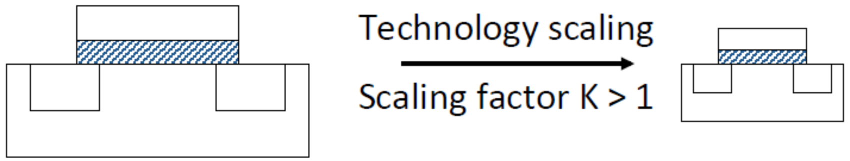
<u>Derived scaling behavior of transistor:</u>

Electric field	1
Ids	$1/K$
Capacitance	$1/K$

<u>Derived scaling behavior of circuit:</u>

Delay (CV/I)	$1/K$
Power (VI)	$1/K^2$
Power-delay product	$1/K^3$
Circuit density (α 1/A)	K^2

Constant Voltage Scaling



<u>Primary scaling factors:</u>

Tox, L, W, Xj (all linear dimensions)	$1/K$
Na, Nd (doping concentration)	K^2
Vdd (supply voltage)	1

<u>Derived scaling behavior of transistor:</u>

Electric field	K
Ids	K
Capacitance	$1/K$

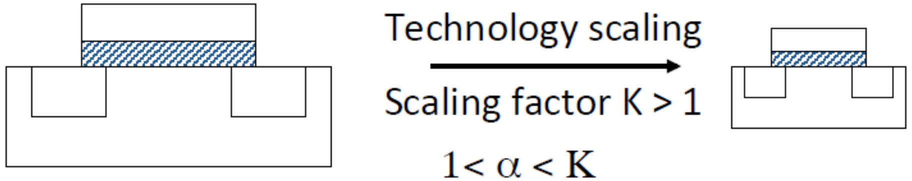
<u>Derived scaling behavior of circuit:</u>

Delay (CV/I)	$1/K^2$
Power (VI)	K
Power-delay product	$1/K$
Circuit density (α 1/A)	K^2

TABLE II
SCALING RESULTS FOR INTERCONNECTION LINES

Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	κ
Normalized voltage drop IR_L/V	κ
Line response time $R_L C$	1
Line current density I/A	κ

Generalized Scaling



$1 < \alpha < K$

Primary scaling factors:

Tox, L, W, Xj (all linear dimensions) 1/K	
Na, Nd (doping concentration)	αK
Vdd (supply voltage)	α/K

Derived scaling behavior of transistor:

Electric field	α
Ids	α^2/K
Capacitance	$1/K$

Derived scaling behavior of circuit:

Delay (CV/I)	$1/\alpha K$
Power (VI)	α^3/K^2
Power-delay product	α^2/K^3
Circuit density (α 1/A)	K^2

Non Scaling Factors

Bandgap of Silicon Eg=1.12eV

Thermal voltage kT/q

Mobility degradation

Increasing doping and electric field

Velocity saturation

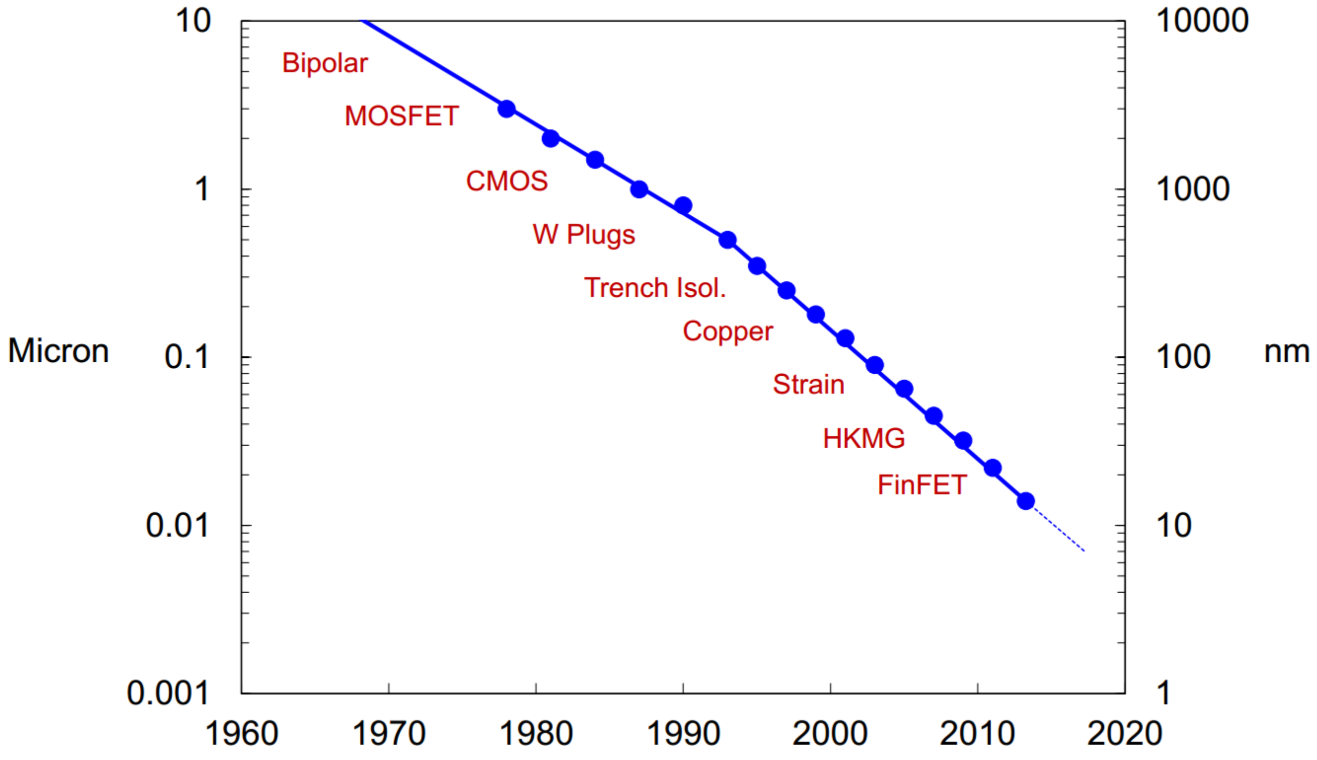
Parasitic s/d resistance

Process tolerance

R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” IEEE J. Solid-State Circuits, vol. SC-9, p. 256, 1974.

General Scaling Trends
CMOS Transistors

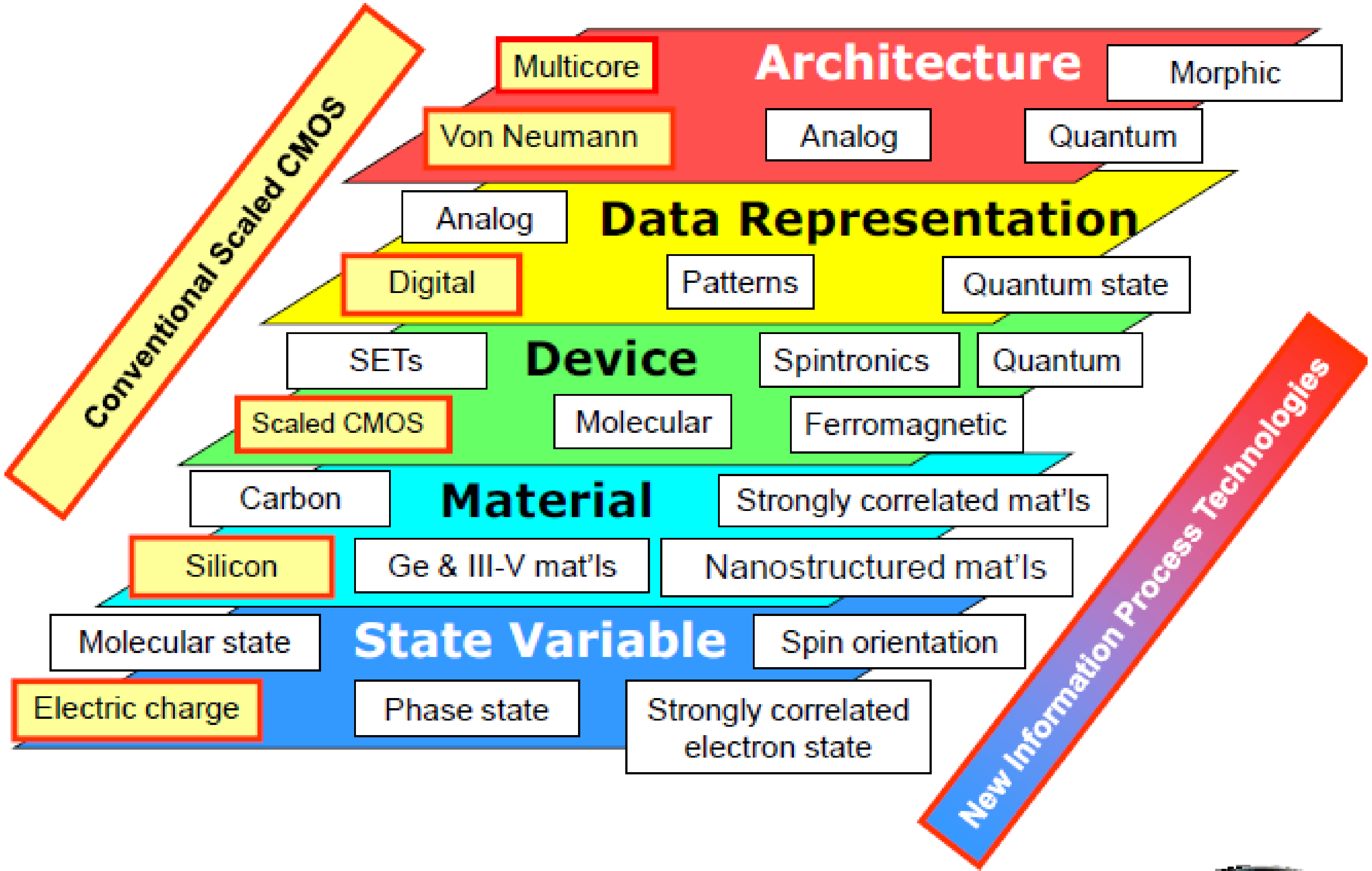
(EP1) Moore's Law Challenges Below 10nm: Technology, Design and Economic Implications



Process/device innovation has always been an indispensable part of scaling

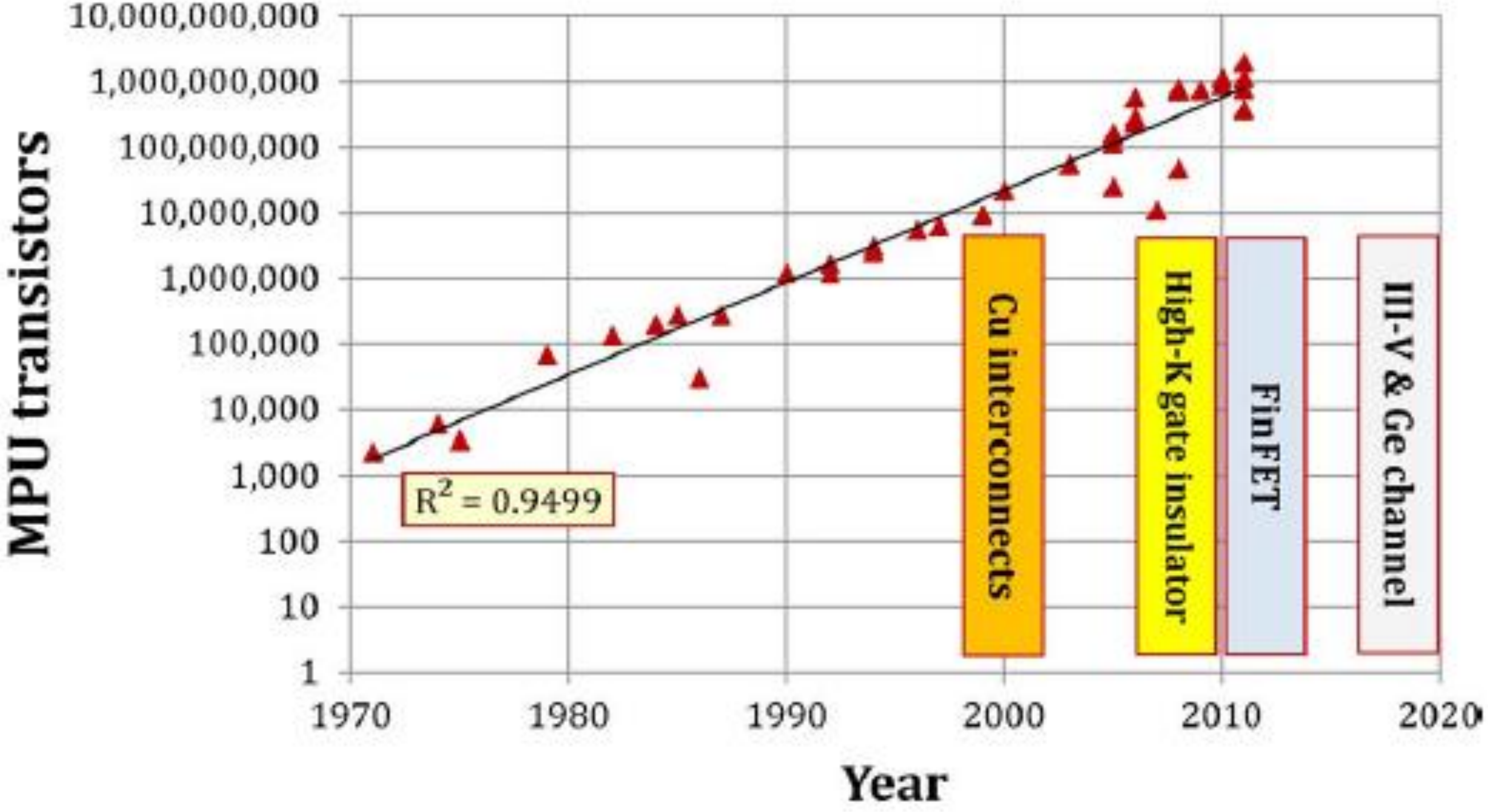
(Ref: Moore's law challenges below 10nm: Technology, design and economic implications, ISSCC (Solid- State Circuits Conference) Panel, 2015)
http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7054075

A Taxonomy for Nano Information Processing Technologies



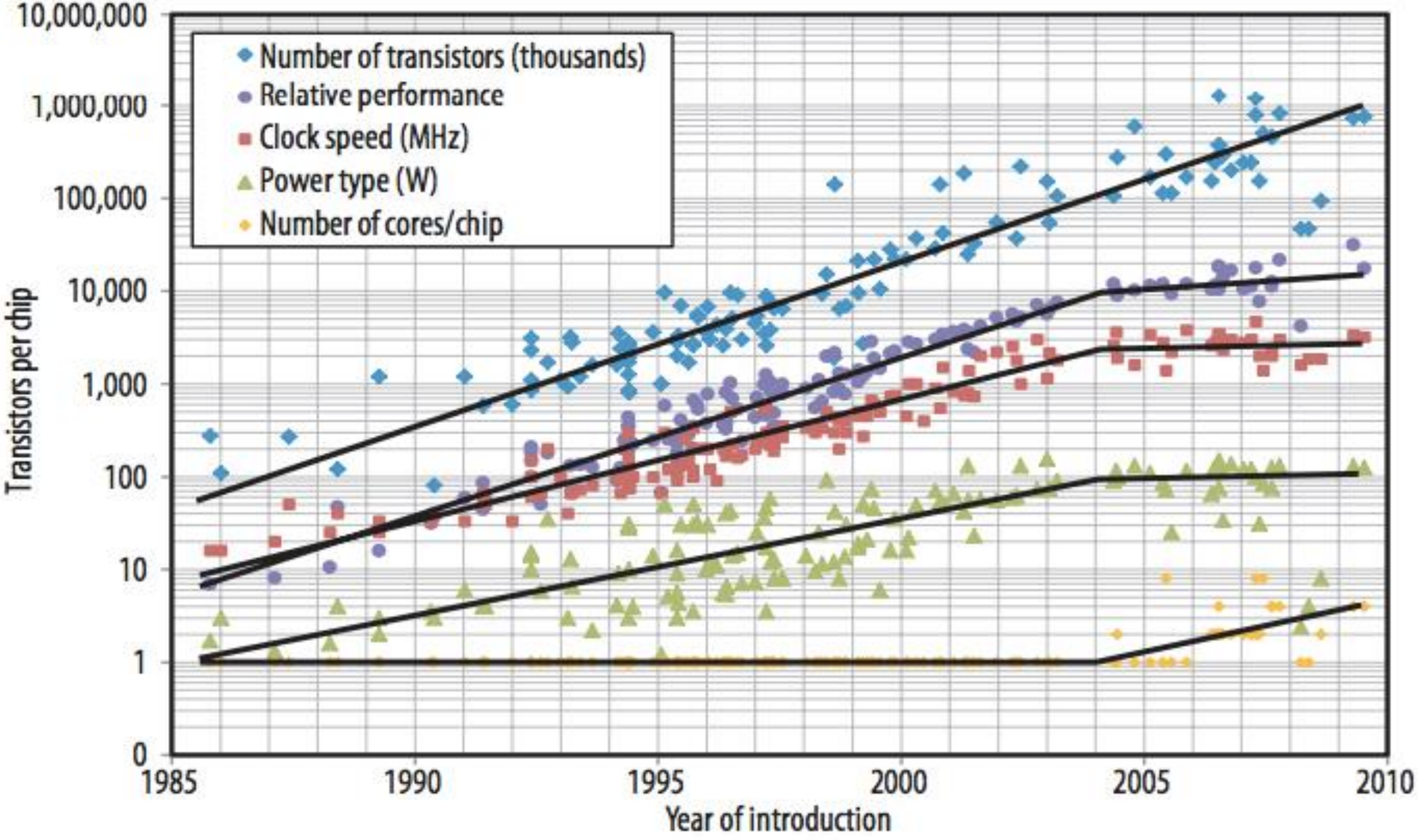
International Technology Roadmap for Semiconductors ITRS

(Ref: ITRS http://www.itrs.net/reports.html)



The number of transistors per microprocessor chip versus time, showing introduction of new enabling technologies.

(Ref: Cavin et al, Science and Engineering Beyond Moore's Law, Proceedings of the IEEE | Vol. 100, May 13th, 2012)



The number of transistors per microprocessor chip versus time, showing introduction of new enabling technologies.

(Ref: National Research Council, The Future of Computing Performance: Game Over or Next Level? Nat'l Academies Press, 2010)

Trends & Wishes

(various technologies linked to detection and imaging)

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2013 EDITION

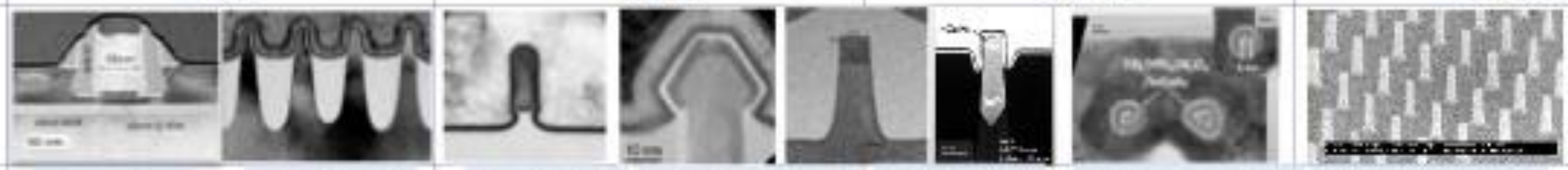
CMOS Scaling Roadmap

Year of Production	*2013*	*2015*	*2017*	*2019*	*2021*	*2023*	*2025*	*2028*
Logic Industry "Node Name" Label	"16/14"	"10"	"7"	"5"	"3.5"	"2.5"	"1.8"	
Logic ½ Pitch (nm)	40	32	25	20	16	13	10	7
Flash ½ Pitch [2D] (nm)	18	15	13	11	9	8	8	8
DRAM ½ Pitch (nm)	28	24	20	17	14	12	10	7.7
FinFET Fin Half-pitch (new) (nm)	30	24	19	15	12	9.5	7.5	5.3
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0
6-t SRAM Cell Size(um2) [@60f2]	0.096	0.061	0.038	0.024	0.015	0.010	0.0060	0.0030
MPU/ASIC HighPerf 4t NAND Gate Size(um2)	0.248	0.157	0.099	0.062	0.039	0.025	0.018	0.009
4-input NAND Gate Density (Kgates/mm) [@155f2]	4.03E+03	6.37E+03	1.01E+04	1.61E+04	2.55E+04	4.05E+04	6.42E+04	1.28E+05
Flash Generations Label (bits per chip) (SLC/MLC)	64G /128G	128G /256G	256G / 512G	512G / 1T	512G / 1T	1T / 2T	2T / 4T	4T / 8T
Flash 3D Number of Layer targets (at relaxed Poly half pitch)	16-32	16-32	16-32	32-64	48-96	64-128	96-192	192-384
Flash 3D Layer half-pitch targets (nm)	64nm	54nm	45nm	30nm	28nm	27nm	25nm	22nm
DRAM Generations Label (bits per chip)	4G	8G	8G	16G	32G	32G	32G	32G
450mm Production High Volume Manufacturing Begins (100Kwspm)				2018				
Vdd (High Performance, high Vdd transistors)[**]	0.86	0.83	0.80	0.77	0.74	0.71	0.68	0.64
1/(CV/I) (1/psec) [**]	1.13	1.53	1.75	1.97	2.10	2.29	2.52	3.17
On-chip local clock MPU HP [at 4% CAGR]	5.50	5.95	6.44	6.96	7.53	8.14	8.8	9.9
Maximum number wiring levels [unchanged	13	13	14	14	15	15	16	17
MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	28	22	18	14	11	9	7	5
MPU High-Performance Physical Gate Length (GLph) (nm) [**]	20	17	14	12	10	8	7	5
ASIC/Low Standby Power (LP) Physical Gate Length (nm) (GLph)[**]	23	19	16	13	11	9	8	6

*** Note: from the PIDS working group data; however, the calibration of Vdd, GLph, and I/CV is ongoing for improved targets in 2014 ITRS work*

IMEC LOGIC DEVICE ROADMAP

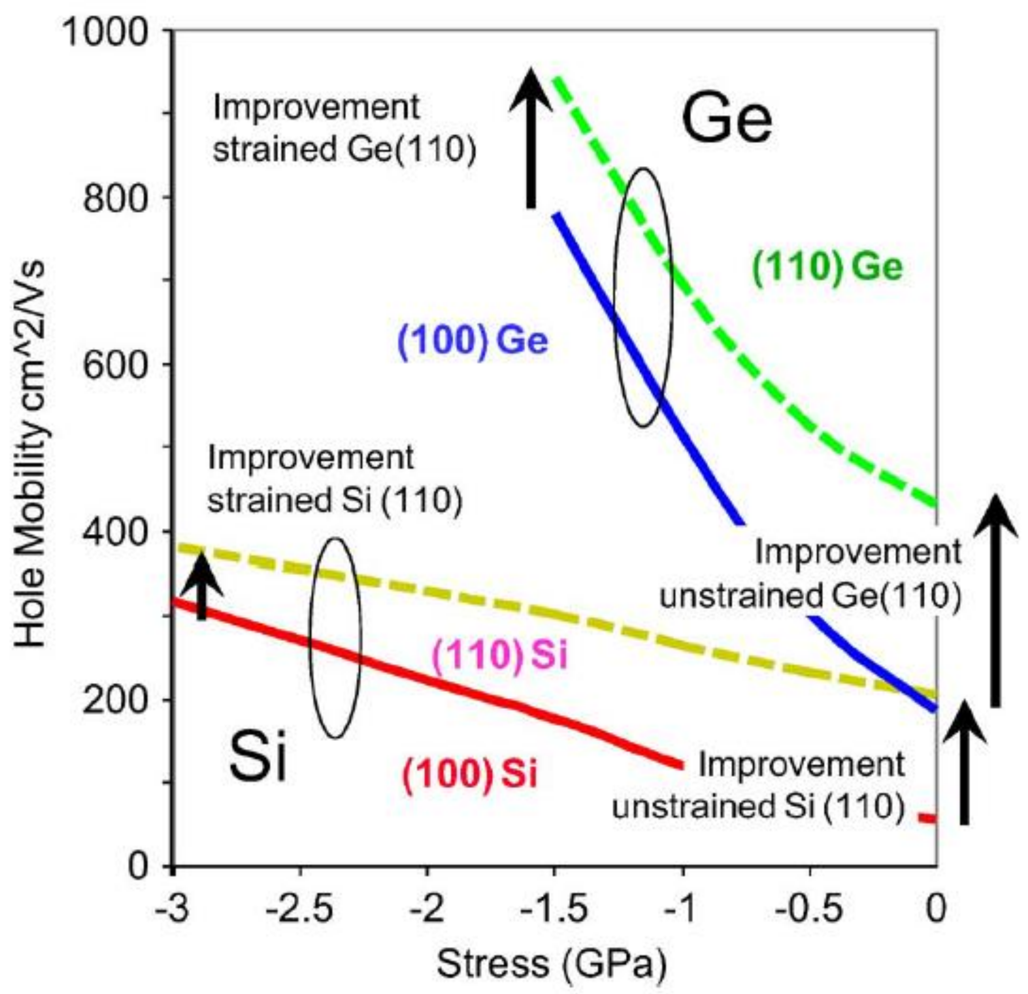
DEVICE TECHNOLOGY FEATURES

Early production	2013 - 2014	2015 - 2016	2017 - 2018	2019 - ...
	16 -14nm	10nm	7nm	5nm
Vdd (V)	0.8	0.8-0.7	0.7-0.5	0.7-0.5
				
	Planar SOI *Bulk FinFET*	*SOI FinFET* *SiGe/Ge channel*	*IIIV channel* *Lateral Nanowire*	*Vertical Nanowire*
Device	FinFET (Bulk, SOI), FDSOI	FinFET (Bulk, SOI)	FinFET (GAA, QW, SOI)	GAA lateral NW; (Vert. NW)

Improve Electrostatics

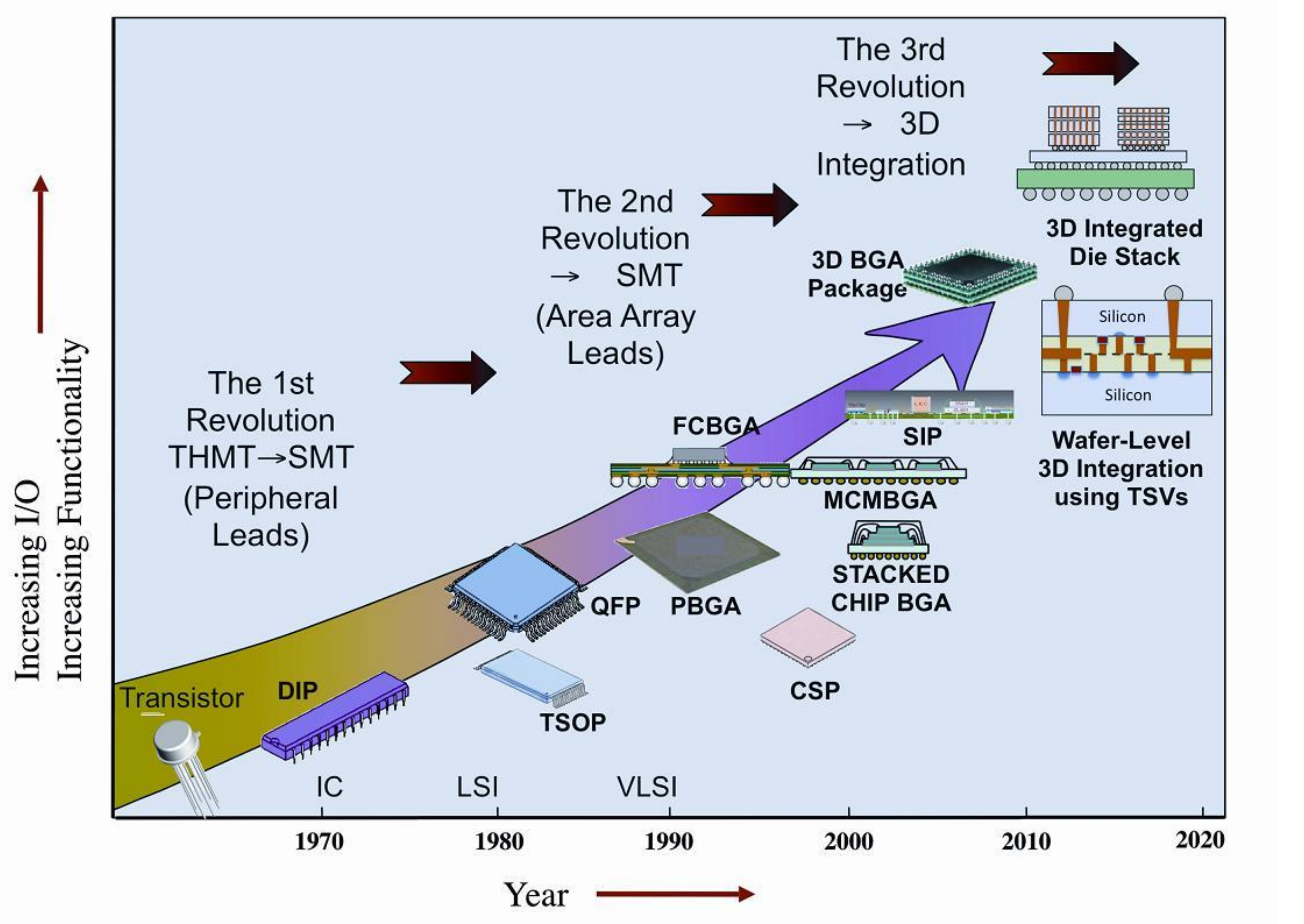
Channel n/p	Si / Si	Si / SiGe	Si / SiGe (Ge)	Si / SiGe (IIIV / Ge)
S/D Strain	N S/D Si:P P S/D eSiGe (55%) Low-k spacer	N S/D Si:P:C P S/D eSiGe (>60%) Low-k spacer	N S/D Si:P:C P S/D eSiGe (>60%) Low-k spacer	TBD

Improve Performance



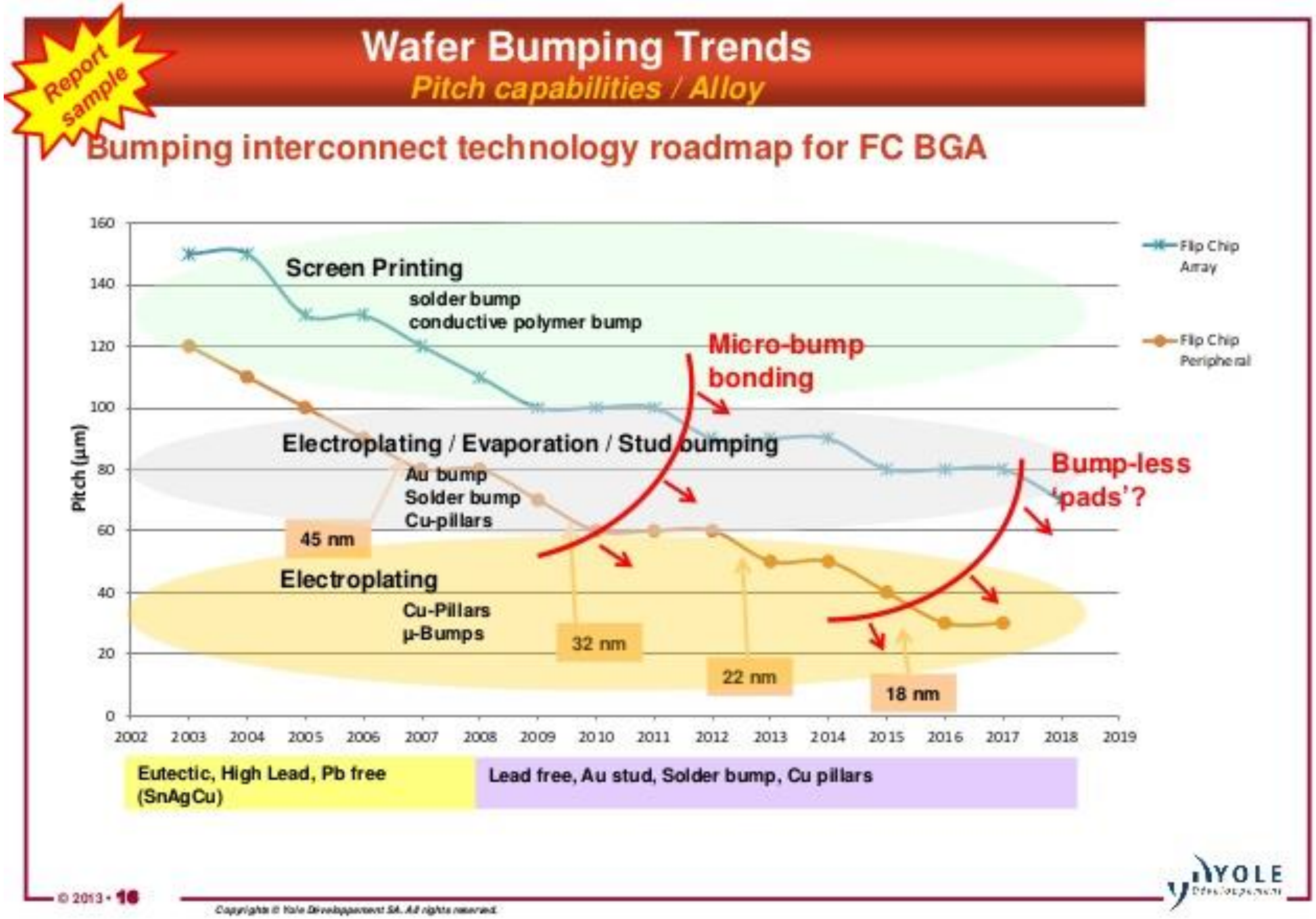
Mobility and strain in Si and Ge as a function of stress and wafer orientation illustrating the reduction in improvement between (100) and (110) material (with a <110> channel direction) as a function of stress.

(Ref: Kelin J. Kuhn, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 7, JULY 2012)



IC packaging Roadmap

(Ref: Electronics Cooling Magazine 2015, http://www.electronics-cooling.com/)

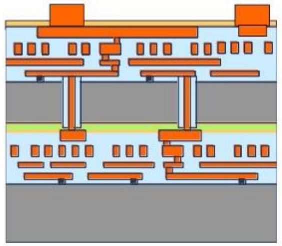
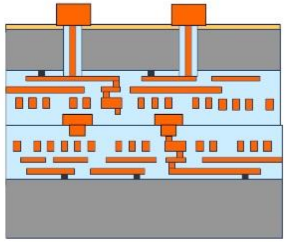
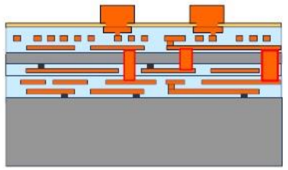
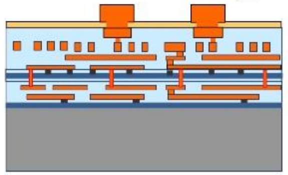
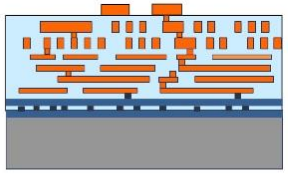


Flip Chip Market trend

(Ref: Yole Developpement http://www.yole.fr/)

3D TECHNOLOGY LANDSCAPE

imec

	3D-SIC	3D-SOC			3D-IC
wiring level	Global	Semi-global	Intermediate	Local	FEOL
2-tier stack				2nd FEOL after stacking 	Multi-tier FEOL 
Contact Pitch *Relative density:*	40 ⇒20 ⇒10 ⇒*5μm* 1/16⇒¼ ⇒1 ⇒ 4	5 ⇒ 1 μm 4 ⇒ 100	2 μm ⇒ 0.5 μm 50 ⇒ 400	200 ⇒ 100 nm 5000 ⇒ 10000	< 100 nm > 10000
Partitioning	Die	**blocks** of standard cells		**Gates**	**Transistors**

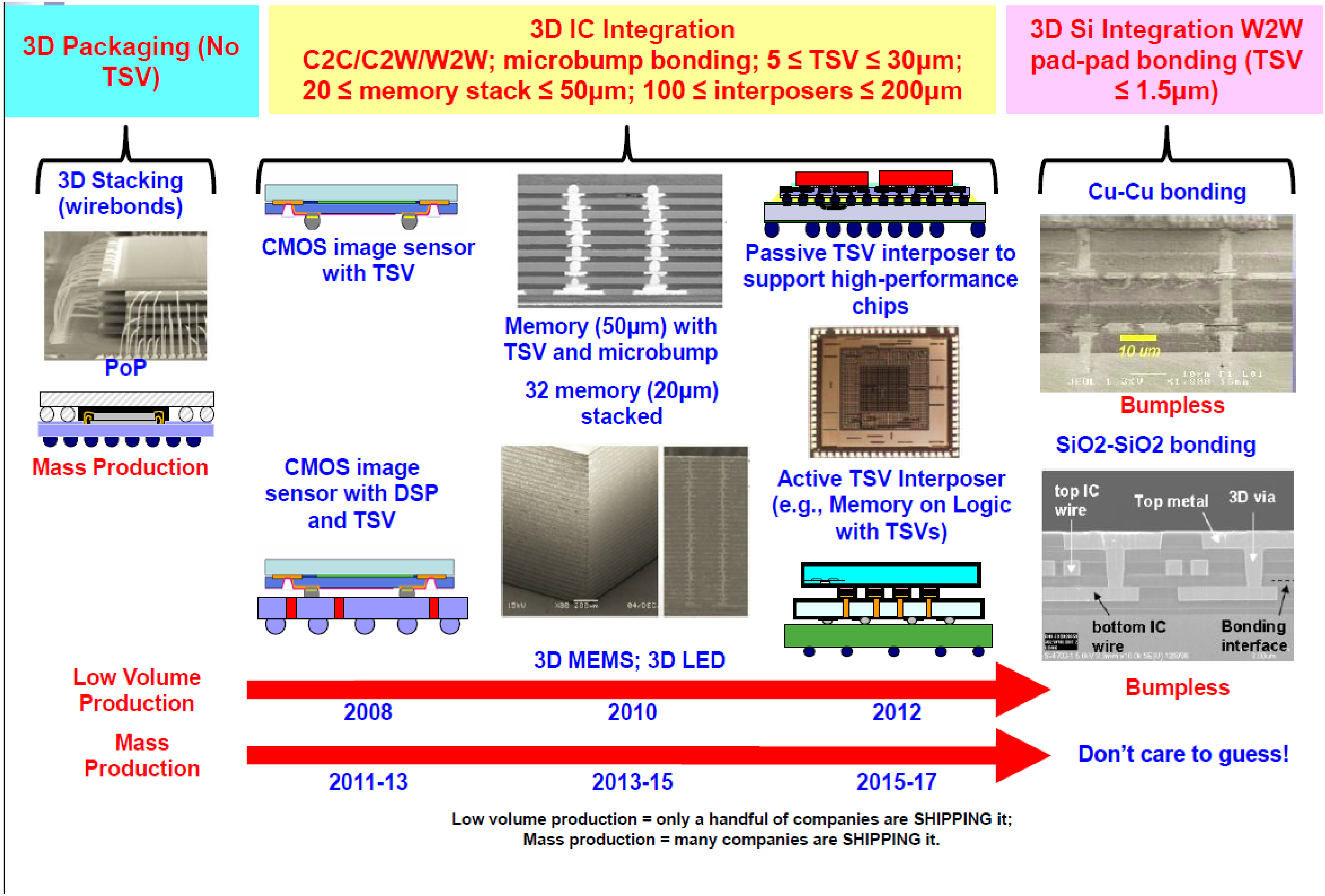
Block-level partitioning

Block size depends on R,C of the 3D interconnect structure

Partitioning/ placement →EDA problem

Standard cell design →device/cell problem

Today's 3D technology landscape segmented by wiring-level, showing cross-sections of typical 2-tier circuit stacks, and indicating planned reductions in contact pitches. (Source: IMEC)



3D Integration Roadmap

(Ref: International Electronics Manufacturing Initiative (iNEMI), 2013 http://www.inemi.org/about-us)

TSV AND Si INTERPOSER FORECAST

	Bn Packages		TSV Die/ Package		Bn Die		Die per 300mm Wafer	M Wafers (300mm Equiv.)		Typical Wafer Size
	2014	2016	2014	2016	2014	2016		2014	2016	
DRAM/NAND (plus control die)	0.2	1	3	2.3	0.6	2.3	650	0.9	3.5	300
Logic and Memory	0	0.25	1	1	0	0.25	390	0.0	0.6	300
Si Interposer for Logic	0.05	0.16	1	1	0.05	0.16	300	0.2	0.5	200/300/ panel
RF/Discrete/LED/	1.7	2.5	1	1	1.7	2.5	7000	0.24	0.4	150/200/300
Image Sensor	2.6	2.9	1	1	2.55	2.85	3000	0.85	1.0	200/300
Total	4.5	6.8			4.9	8.1		2.2	6.0	

3D Integration Roadmap

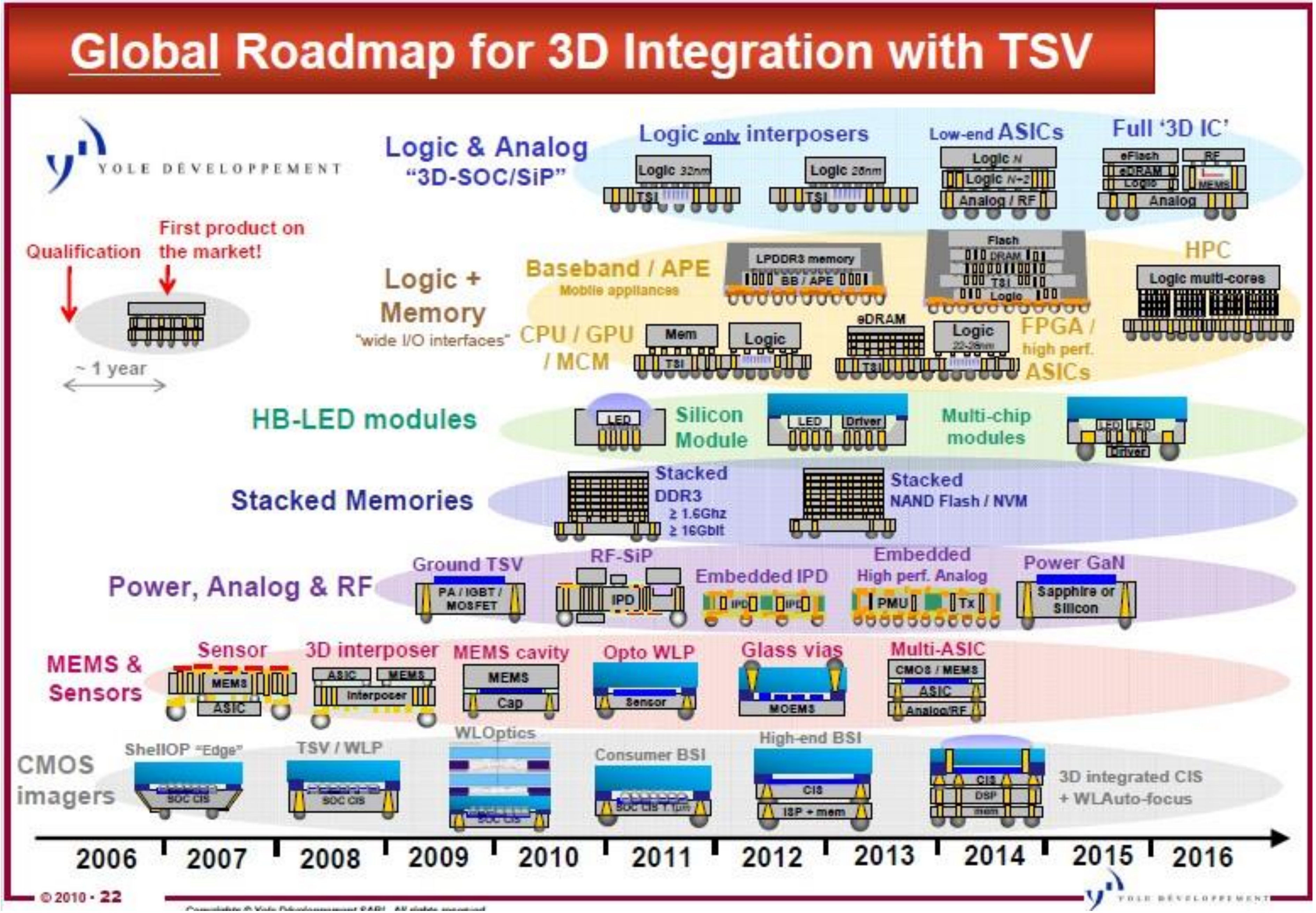
(Ref: International Electronics Manufacturing Initiative (iNEMI), 2013 http://www.inemi.org/about-us)

Draft Interposer Table

Base Silicon Interposer	Year of Production	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
TSV	Minimum TSV pitch (um)	40	40	30	30	30	20	20	20	20	20	20
	Minimum TSV diameter(um) (D)	20	20	15	15	15	10	10	10	10	10	10
	TSV maximum aspect ratio (L/D)	5	5	7	7	7	10	10	10	10	10	10
	Minimum Si Wafer final thickness (um) (3)	100	100	100	100	100	100	100	100	100	100	100
	TSV Methods and Materials											
	Via fill method	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill	Cu ECD Fill
	TSV Fill	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other	Cu / Other
3D Integration	Alignment requirement, um (assume 25% exit dia)	5	5	3.75	3.75	3.75	2.5	2.5	2.5	2.5	2.5	2.5
	Maximum Number of RDL Layers - Top side	4	4	4	4	4	4	4	4	4	4	4
	Maximum Number of RDL Layers - Bottom side	2	2	2	2	2	2	2	2	2	2	2
	Interconnect methods - Top side (5)	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu	Cu-Cu, Cu-Sn-Cu, Cu-Ni/Au-SnAg, AuSn, Cu-In-Cu
	Interconnect methods - Bottom side	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder	Solder Cu Pillar/Solder

3D Integration Roadmap

(Ref: International Electronics Manufacturing Initiative (iNEMI), 2013 http://www.inemi.org/about-us)

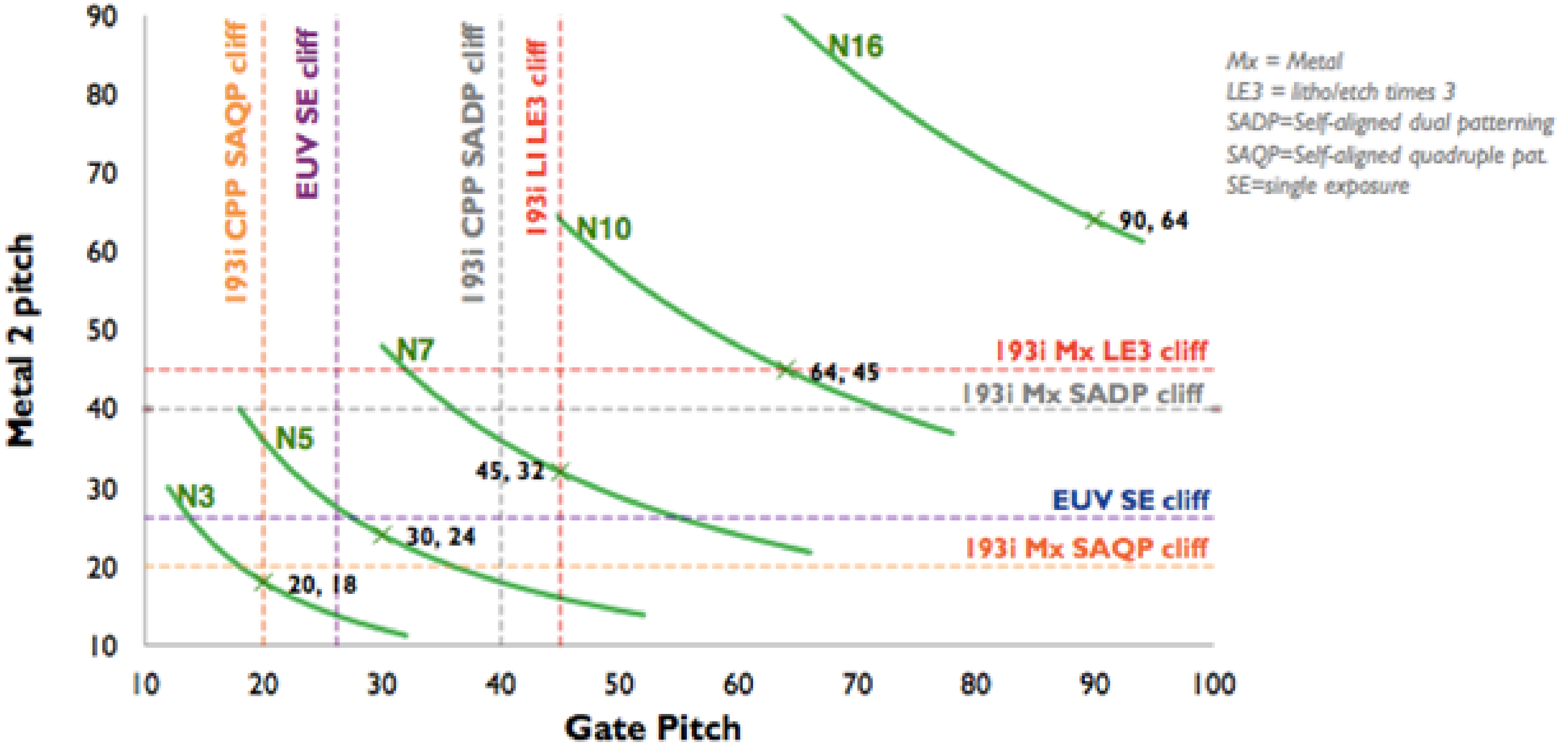


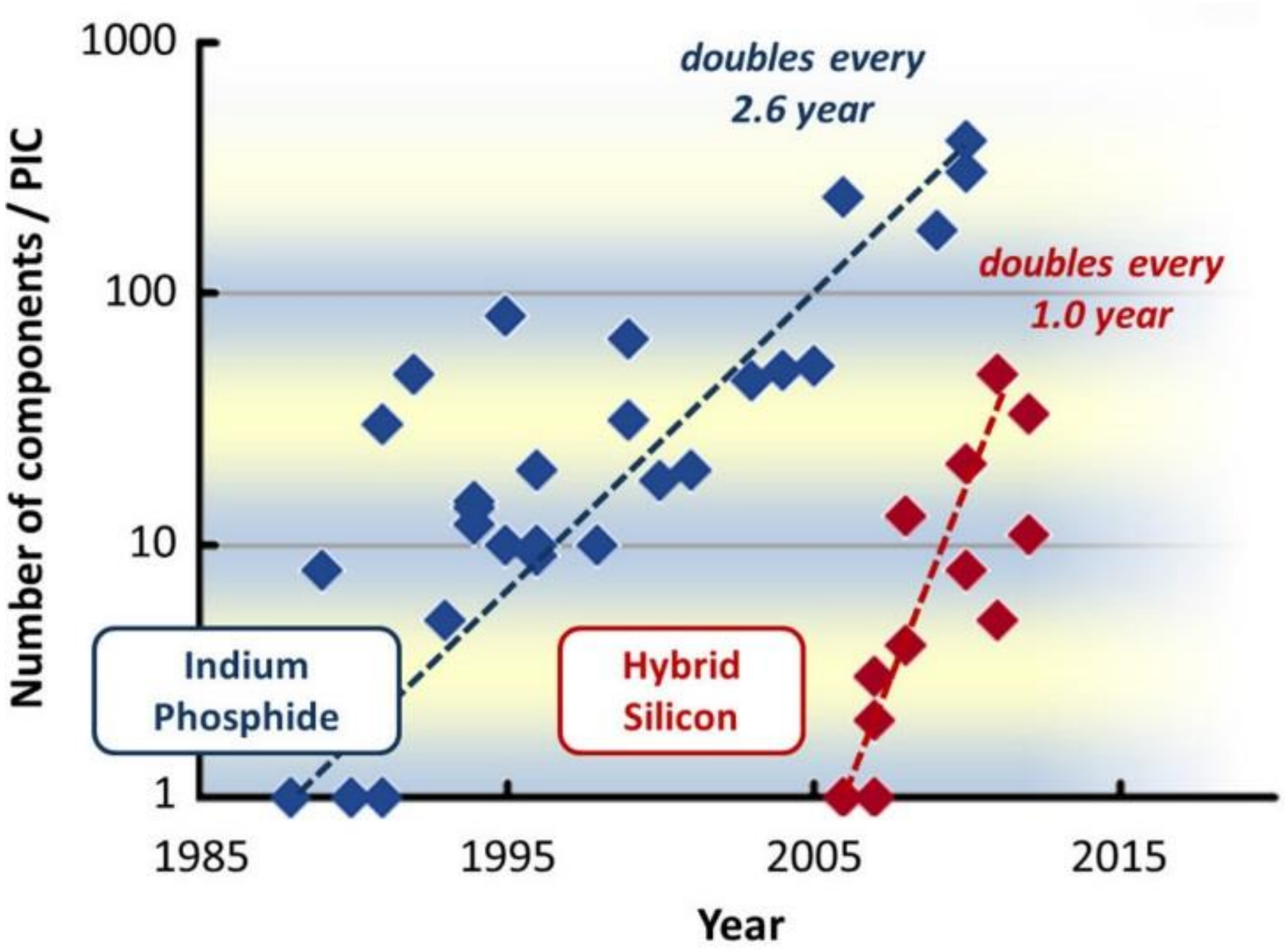
(Ref: Yole Developpement http://www.yole.fr/)

IMEC LOGIC LITHOGRAPHY ROADMAP

KEY TRANSISTOR DIMENSIONS

Early production	2013 - 2014	2015 - 2016	2017 - 2018	2019 - ...
	16 -14nm	10nm	7nm	5nm
FinFET pitch (nm)	42-48nm	30-32nm	21-24nm	14-16nm
Gate Pitch (nm)	64-80nm	50-64nm	40-45nm	22-32nm
Contact pitch (nm)	64-80nm	50-64nm	40-45nm	22-32nm
Metal pitch (nm)	56-64nm	40-45nm	28-32nm	20-22nm





Development of chip complexity measured as the number of components per chip. Data for indium-phosphide-based photonic integrated circuits (PICs, blue) and for hybrid-silicon PICs (red) which fit to exponential growth curves (dashed).

(Ref: M. J. R. Heck, M. L. Davenport, and J. E. Bowers, "Progress in hybrid-silicon photonic integrated circuit technology," SPIE Newsroom, doi:10.1117/2.1201302.004730 (2013)).

Chip Name	Measured quantity	Application	Input configuration	Technology
FLC_SiPM	Pulse charge	ILC Analog HCAL	Current input	CMOS 0,8 μm
MAROC	Pulse charge, trigger	ATLAS luminometer	Current input	SiGe 0,35 μm
SPIROC	Pulse charge, trigger, time	ILC HCAL	Current input	SiGe 0,35 μm
NINO	Trigger, pulse width	ALICE TOF	Differential input	CMOS 0,25 μm
PETA	Pulse charge, trigger,time	PET	Differential input	CMOS 0,18 μm
BASIC	Pulse height, trigger	PET	Current input	CMOS 0,35 μm
SPIDER (VATA64-HDR16)	Pulse height, trigger, time	SPIDER RICH	Current input	
RAPSODI	Pulse height, trigger	SNOOPER	Current input	CMOS 0,35 μm

SiPM for HEP detectors

(Ref: Erika Garutti, Silicon photomultipliers for high energy physics detectors, Journal of Instrumentation, Volume 6, October 2011)

Chip Name	# of channels	Digital output	Power supply	Area [sqr mm]	Dynamic range	Input resistance	Timing jitter	Year
FLC_SiPM	18	n	5V (0,2W)	10			-	2004
MAROC2	64	y	5 V	16	80 pC	50 Ω		2006
SPIROC	36	y	5 V	32				2007
NINO	8	n	(0,24W)	8	2000 pe	20 Ω	260 ps	2004
PETA	40	y	(1,2W)	25	8 bit		50 ps	2008
BASIC	32	y	3,3 V	7	70 pC	17 Ω	~120 ps	2009
SPIDER (VATA64-HDR16)	64	n		15	12 pC			2009
RAPSODI	2	y	3,3 V (0,2W)	9	100 pC	20 Ω	-	2008

SiPM for HEP detectors

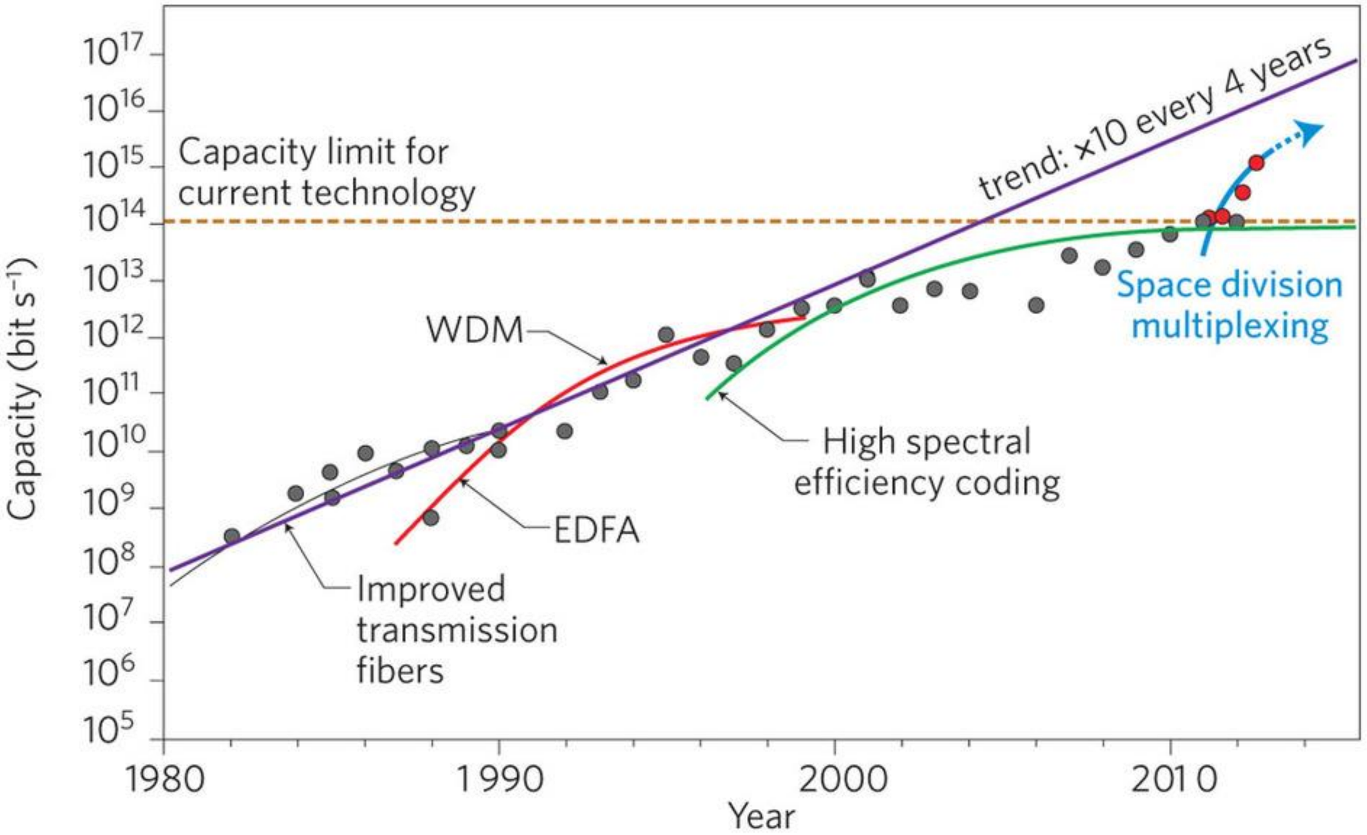
(Ref: Erika Garutti, Silicon photomultipliers for high energy physics detectors, Journal of Instrumentation, Volume 6, October 2011)

Estimated Year of Production	2007	2008	2009	2010	2011	2012	2013
High Performance MPU properties							
MPU/ASIC metal 1 1/2 pitch (nm)	68	59	52	45	40	36	32
V_{dd} (high performance) (V)	1.1	1	1	1	1	0.9	0.9
On chip local clock (MHz)	9,285	10,972	12,369	15,079	17,658	20,065	22,980
MTransistors per cm^2	357	449	566	714	899	1,133	1,427
NMOS intrinsic delay τ (ps)	0.64	0.54	0.46	0.4	0.34	0.29	0.25
Clock Period (ps)	108	91	81	66	66	50	44
Global Electronic Interconnect							
Minimum global pitch (nm)	210	177	156	135	120	108	96
Conductor resistivity ($\mu\Omega$-cm)	2.73	2.87	3	3.1	3.22	3.39	3.52
RC for 1mm global wire (ps)	209	316	410	523	687	787	977
bit hop length: RC = clock period (μ)	719	537	444	355	310	252	211
ave electron bit hops to cross chip	24	33	39	49	56	69	83
ave delay or latency (ns)	2.6	3.0	3.2	3.3	3.7	3.5	3.6
MTransistors within bit hop radius	6	4	4	3	3	2	2
Power for bits at clock speed (mW)	1.36	1.02	0.91	0.83	0.72	0.55	0.50
Energy per bit per hop (pJ)	0.147	0.093	0.074	0.055	0.048	0.028	0.022
Bit flux/Watt (**Tbit**/sec/cm/W)	0.140	0.166	0.172	0.186	0.186	0.261	0.276
Global Photonic Interconnect							
Meindl partition length (μ), N=1	1,287	1,184	1,115	1,010	933	876	818
Light speed * clock period/3 (μ)	10,800	9,100	8,100	6,600	6,600	5,000	4,352
ave hops to chip edge for photons	2	2	2	3	3	4	4
Mtransistors within photon hop radius	1,308	1,168	1,166	977	1,230	889	849
ave delay or latency (ns)	0.09	0.09	0.09	0.09	0.09	0.09	0.09
Energy per bit to cross chip (aJ)	90	90	90	90	90	90	90
Potential Bit flux/Watt (**Pbit**/sec/cm/W)	11	11	11	11	11	11	11

(a)

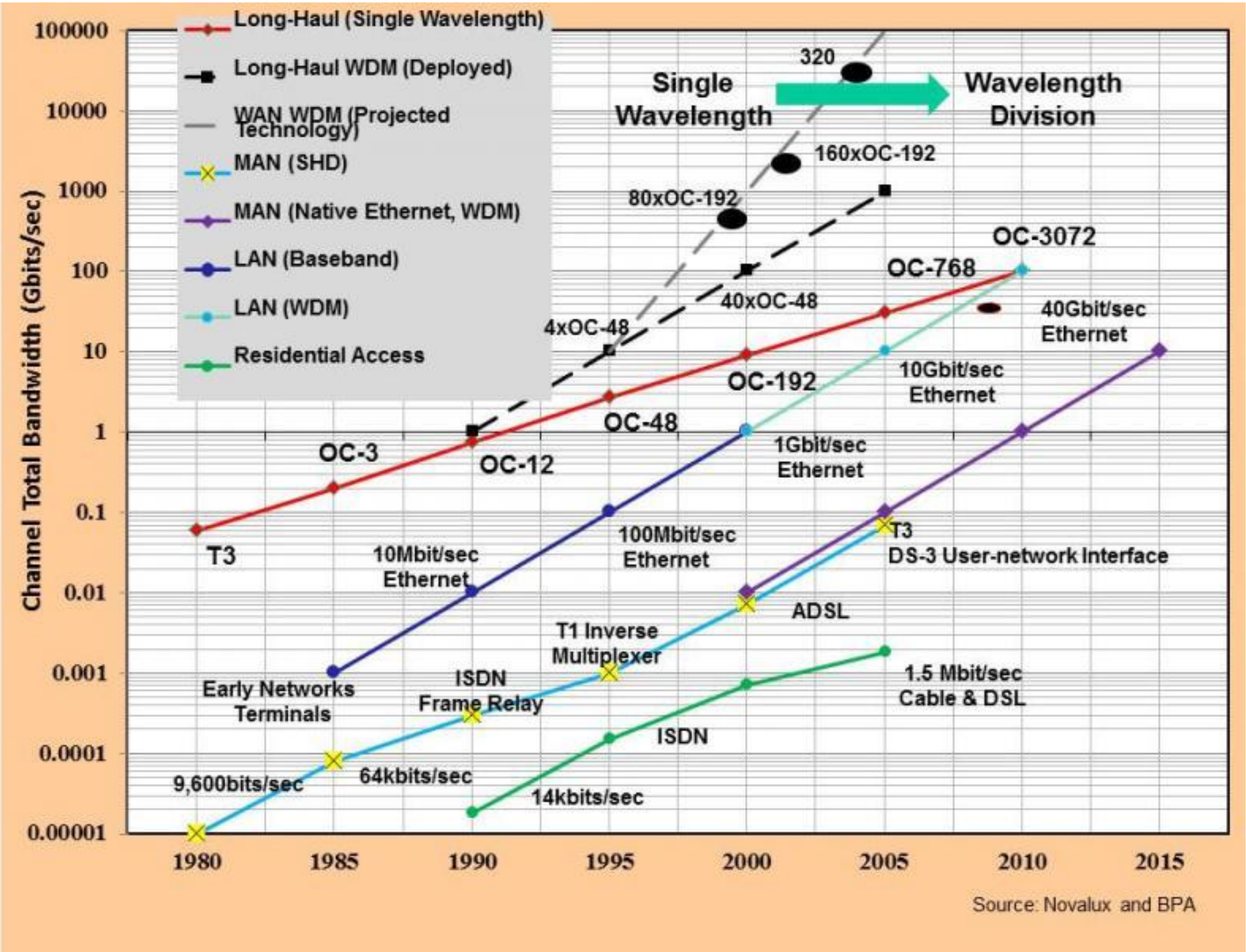
Photonic Interconnect Comparison

(Ref: Raymond G. Beausoleil et al. Proceedings of the IEEE, Vol. 96, No. 2, February 2008)

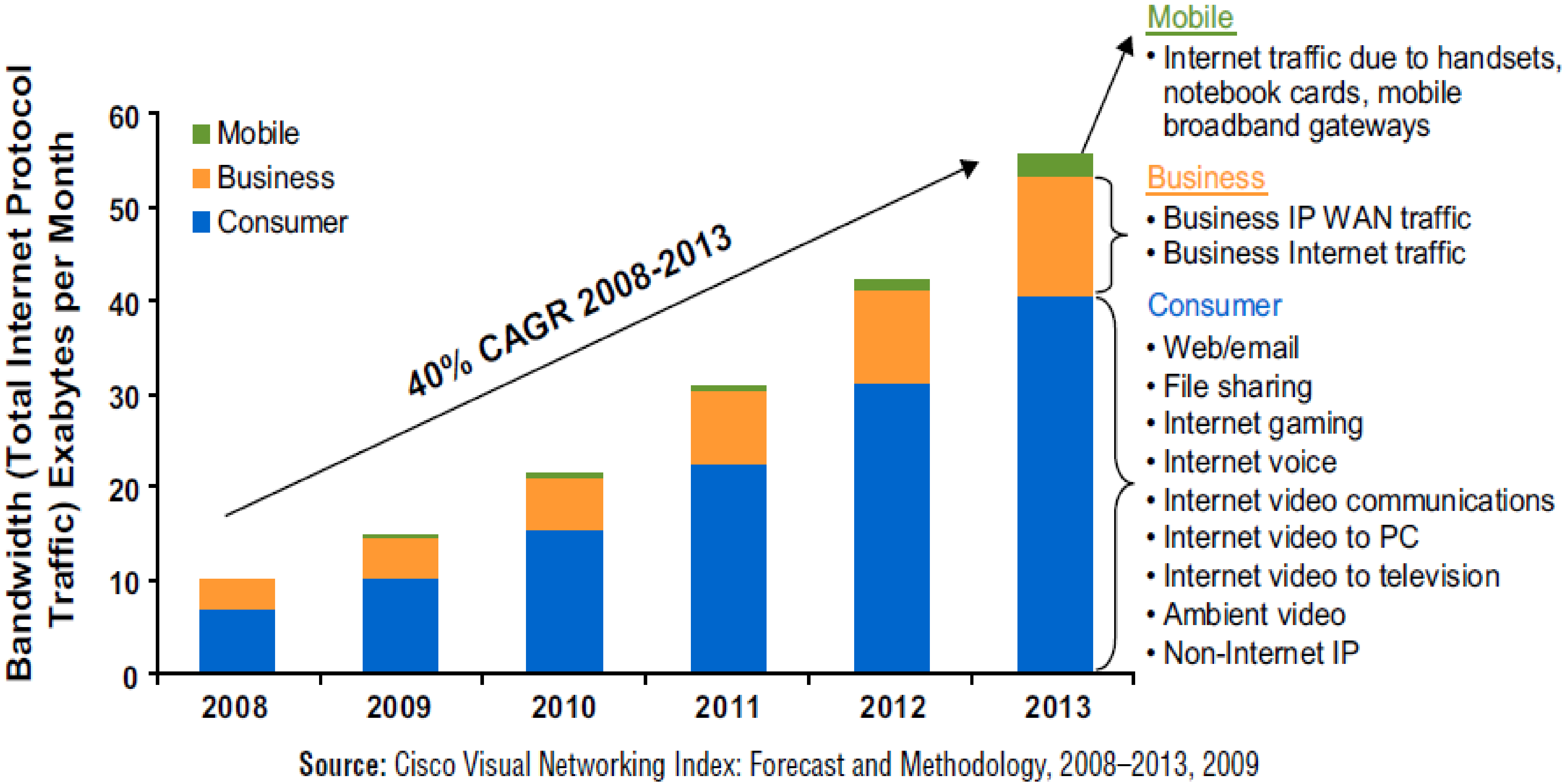


The data points represent the highest capacity transmission numbers (all transmission distances considered) reported at the post-deadline sessions of the annual Optical Fiber Communications Conference over the period 1982 to the present. The transmission capacity of a single fibre increases by a factor of approximately 10 every four years. Key previous technological breakthroughs include the development of low-loss SMFs, the EDFA, WDM and high-spectral-efficiency coding through DSP-enabled coherent transmission. The data points for SDM also include results from the post-deadline session of the annual European Conference on Optical Communications in 2011 and 2012. SDM seems poised to provide the next big jump in transmission capacity.

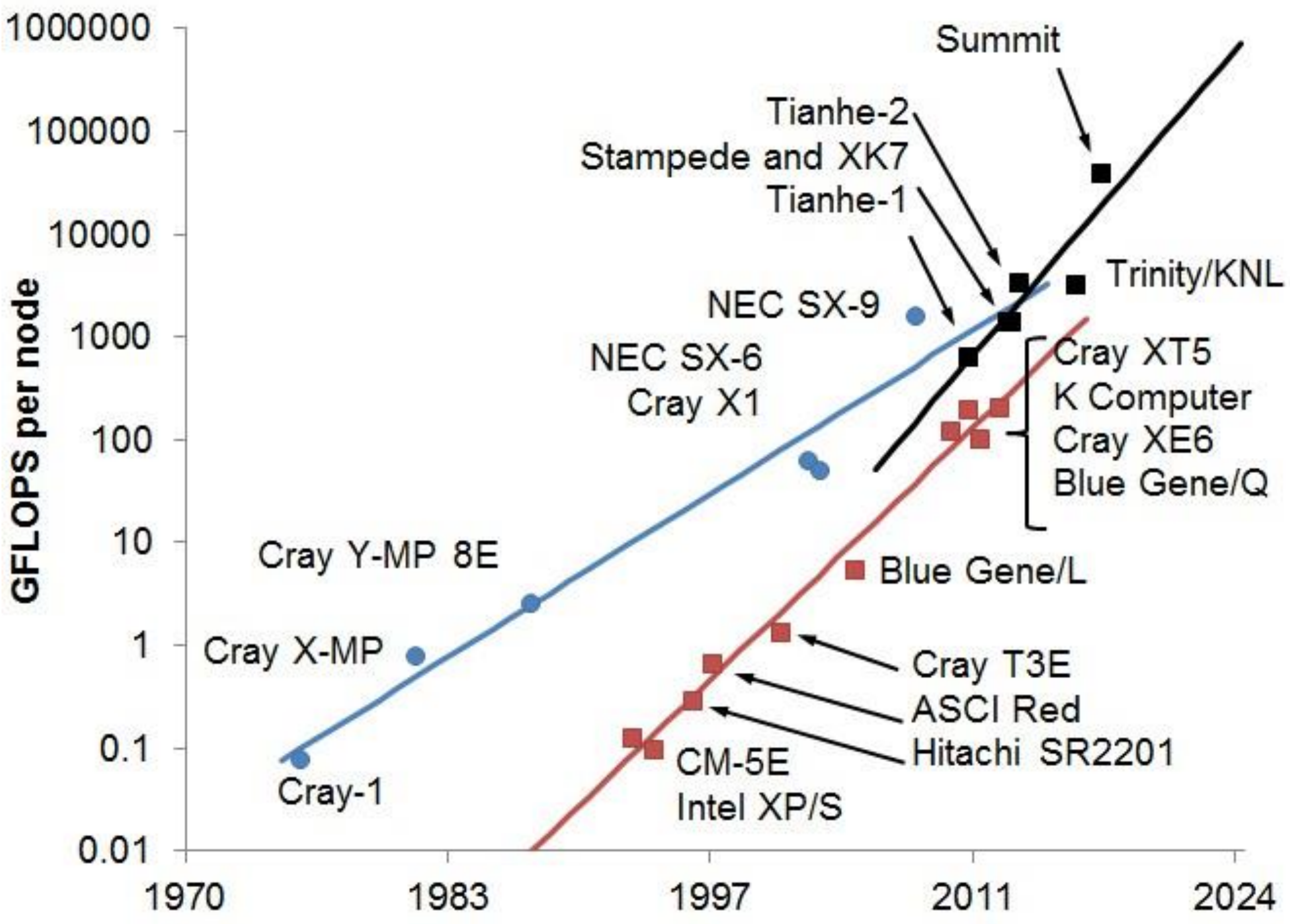
(Ref: D. J. Richardson, J. M. Fini & L. E. Nelson, Nature Photonics 7, 354–362 (2013) doi:10.1038/nphoton.2013.94 Published online 29 April 2013)



Projected high-speed I/O data bandwidth trends for popular communication standards.
(Ref: ITRS http://www.itrs.net/)



Global Internet Protocol Traffic Growth, 2008–2013

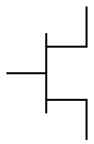
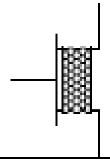
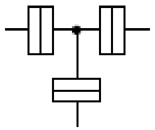
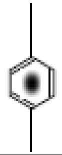
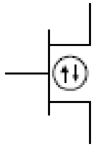


Exascale HPC evolution. The blue line shows the trend for vector machines, the first supercomputers, and the red line for massively parallel machines, which followed them architecturally. The black line shows the more modern hybrid, many core machine.

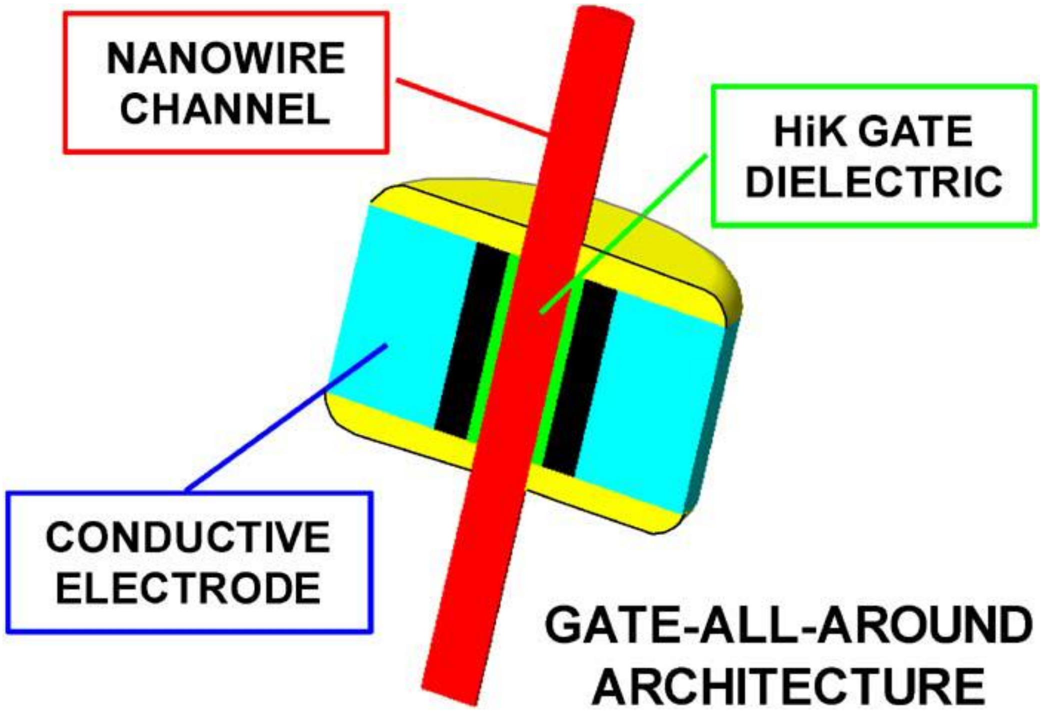
(Ref: The National Energy Research Scientific Computing Center (NERSC), US, 2015, https://www.nersc.gov/about/)

Dreams
(various technologies)

Table ERD7a Emerging Research Logic Devices—Demonstrated and Projected Parameters

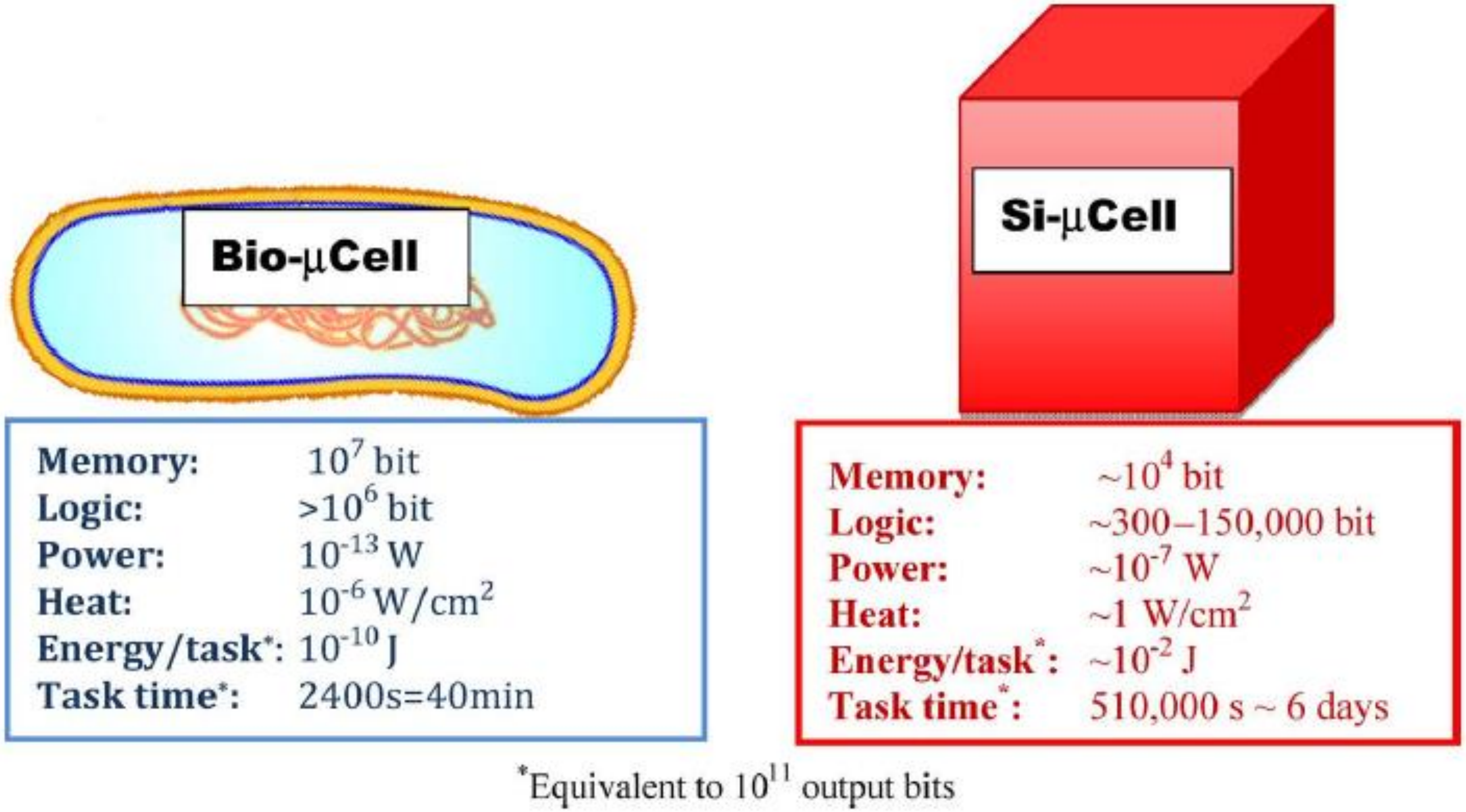
Device								
								
			FET Extension					
		FET [A]	*1D structures*	*Channel replacement*	*SET*	*Molecular*	*Ferromagnetic logic*	*Spin transistor*
Typical example devices		Si CMOS	CNT FET NW FET NW hetero-structures Nanoribbon transistors with graphene	III-V compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque Transistor
Cell Size (spatial pitch) [B]	Projected	100 nm	100 nm [D]	300 nm [I]	40 nm [O]	10 nm [U]	140 nm [Y]	100 nm [C]
	Demonstrated	590 nm	~1.5 µm [E]	1700 nm [J]	~200 nm [K, L]	~2 µm [V]	250 nm [Z, AA]	100 µm [AB]
Density (device/cm^2)	Projected	1E10	4.5E9	6.1E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	3.5E7	~2E9	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [F]	>1 THz	10 THz [Q]	1 THz [W]	1 GHz [Y]	40 GHz [AC]
	Demonstrated	1.5 THz	200 MHz [G]	>300 GHz	2 THz [R]	100 Hz [V]	30 Hz [Z, AA]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [O]	1 GHz [U]	10 MHz [Y]	Not known
	Demonstrated	5.6 GHz	220 Hz [H]	Data not available	1 MHz [P]	100 Hz [V]	30 Hz [Z]	Not known
Switching Energy, J	Projected	3E-18	3E-18	3.00E-18	1×10^{-18} [O] [$>1.5\times10^{-17}$] [S]	5E-17 [X]	~1E-17 [Z]	3E-18
	Demonstrated	1E-16	1E-11 [H]	1E-16 [J]	8×10^{-17} [T] [$>1.3\times10^{-14}$] [S]	3E-7 [V]	6E-18 [AA]	Not known
Binary Throughput, GBit/ns/cm^2	Projected	238	238	61	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	Data not available	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	RT	RT [M, N]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	InGaAs, InAs, InSb	III-V, Si, Ge,	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides
Research Activity [AD]			379	62	91	244	32	122

(Ref: ITRS http://www.itrs.net/reports.html)



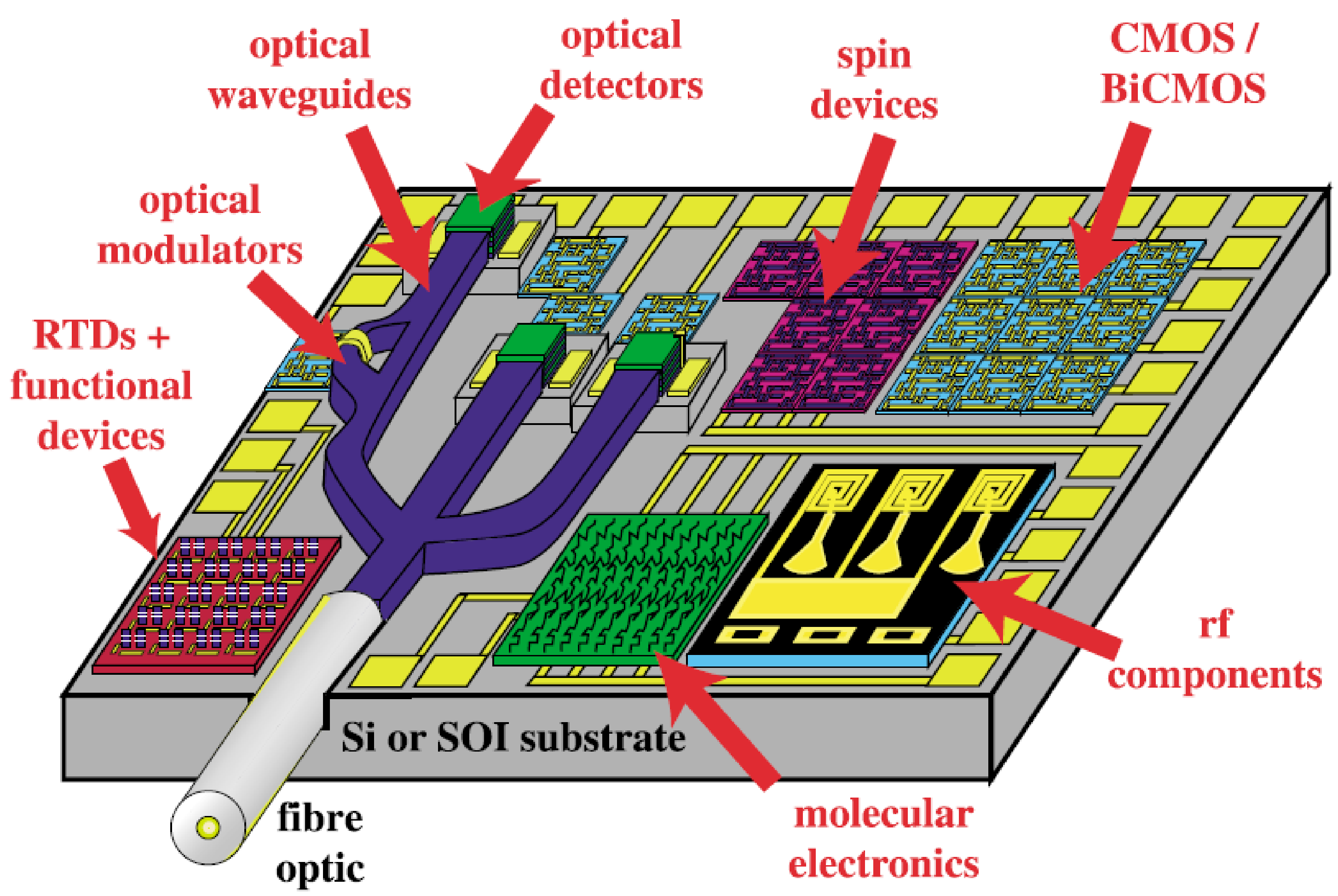
Ultimate CMOS Device with a nanowire channel, a gate-all-around (GAA) architecture, a high-k gate dielectric, and a conductive gate electrode stack. The minimum channel dimensions will be determined by quantum confinement effects and scattering at atomic dimensions. The nanowire architecture is determined by electrostatic requirements to achieve the best possible short-channel control. Each of the various gate layers (interface layer (IL), high-k layer, threshold voltage (VT) control layer, primary work function layer, conduction layer, and so on) is limited by material properties at atomic dimensions.

(Ref: Kelin J. Kuhn, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 7, JULY 2012)



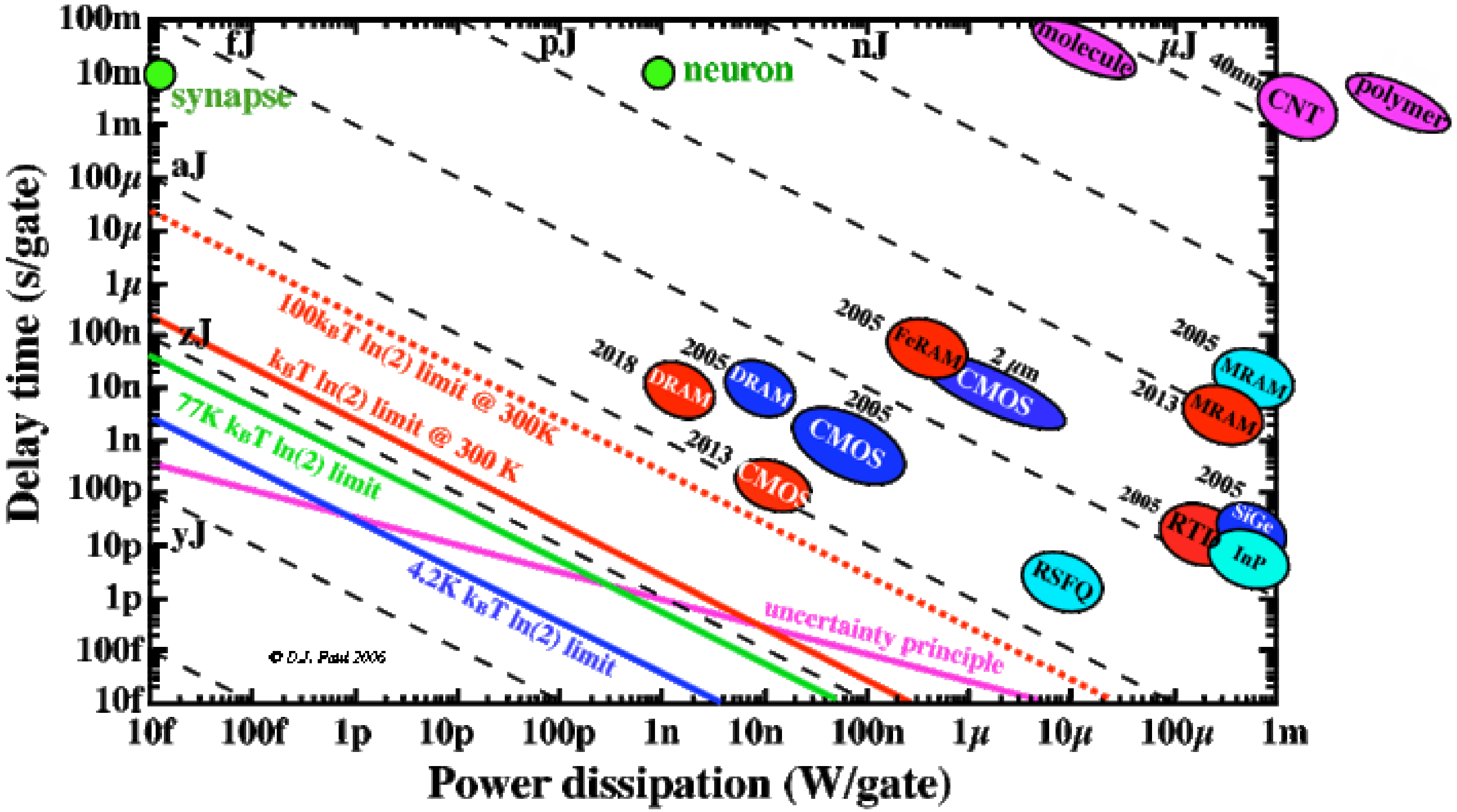
Comparison of significant parameters of the bio-μcell and the Si-μcell.

(Ref: Cavin et al, Science and Engineering Beyond Moore's Law, Proceedings of the IEEE | Vol. 100, May 13th, 2012)



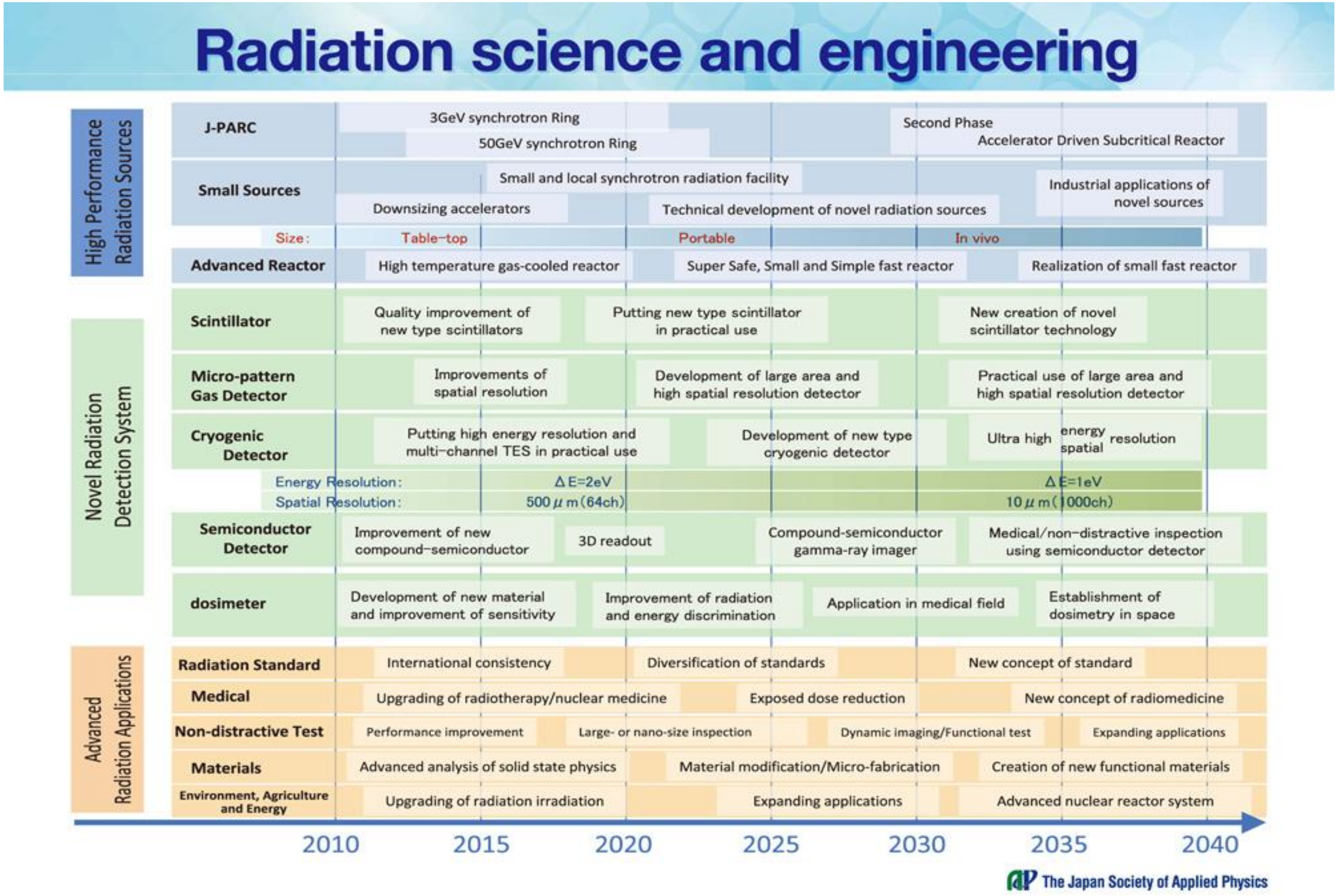
The system-on-a-chip of the future? The ability to integrate new technologies with CMOS or BiCMOS is important but may be too expensive for some technologies or suffer technological problems such as crosstalk like rf solutions. Multi-chip modules may therefore be a more adequate solution for specific applications.

(Ref: European Commission, IST programme, Future and Emerging Technologies, Technology Roadmap for Nanoelectronics, Second Edition, November 2000, Editor: R. Compañó, http://nanotech.law.asu.edu/Documents/2009/09/fetnidrm_239_7700.pdf)

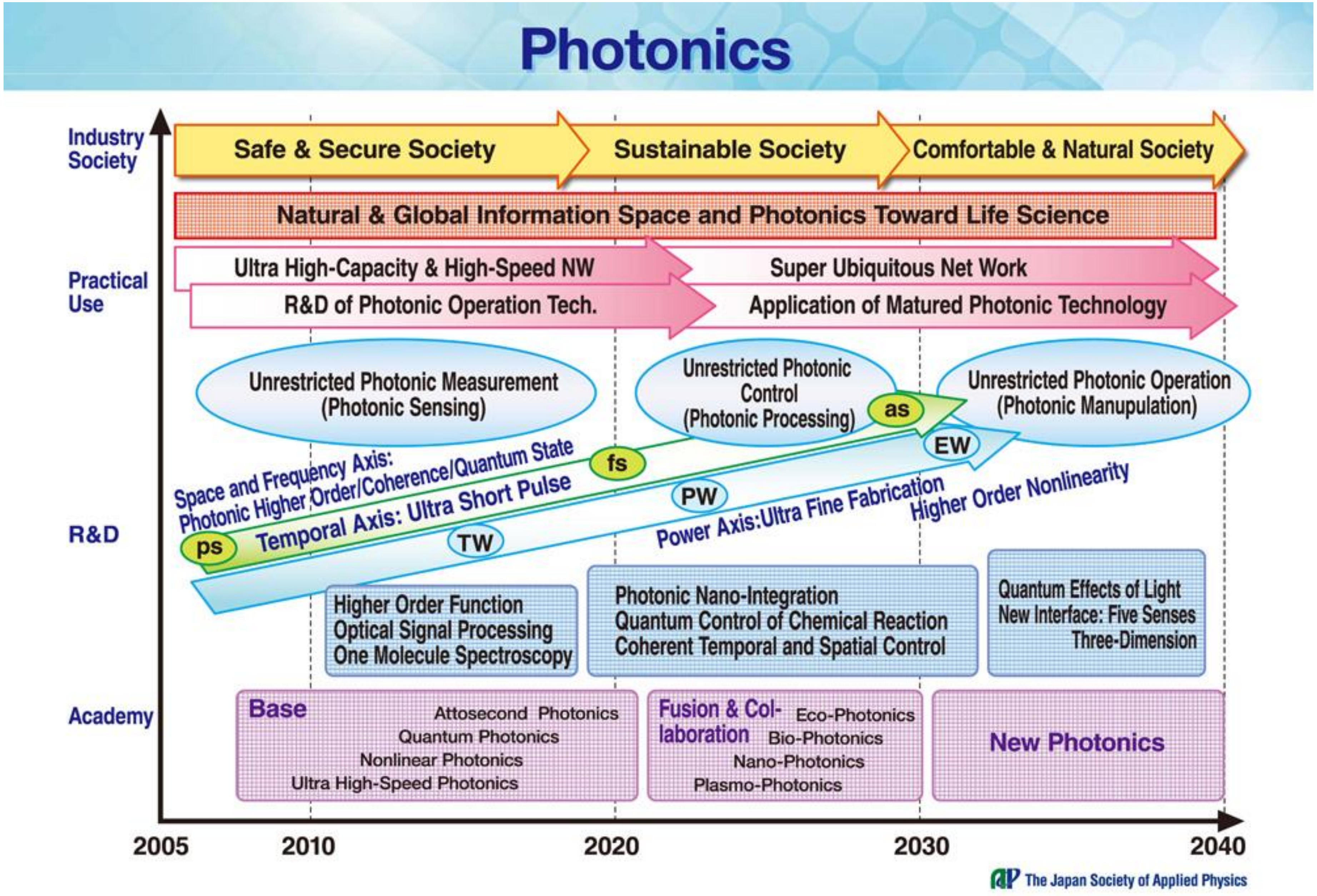


The above figure plots the delay time per transistor (using CVDD/Ion) versus the power dissipation (Ion VDD for the transistors) using either a CMOS inverter, a n-MOS inverter or a p-MOS inverter as appropriate for the technology. To provide a fair comparison, a noise margin required to transmit 1 bit of information down a 1 mm long level-7 interconnect made of copper from a CMOS processor has been assumed for the logic so that the correct scaling of gate width can be accounted for. All devices use EXTRINSIC I-V characteristics from the literature since for CMOS most of the performance limitations are related to contact resistivity, access resistance, parasitic RC time constants etc...... Therefore all comparisons are fair for making circuits from the technology base.)

Semiconductor Group, Glasgow University, (http://userweb.eng.gla.ac.uk/douglas.paul/SiGe/limits.html)



Japan Society of Applied Physics (Academic Roadmap https://www.jsap.or.jp/english/aboutus/academic-roadmap.html)



Japan Society of Applied Physics (Academic Roadmap https://www.jsap.or.jp/english/aboutus/academic-roadmap.html)

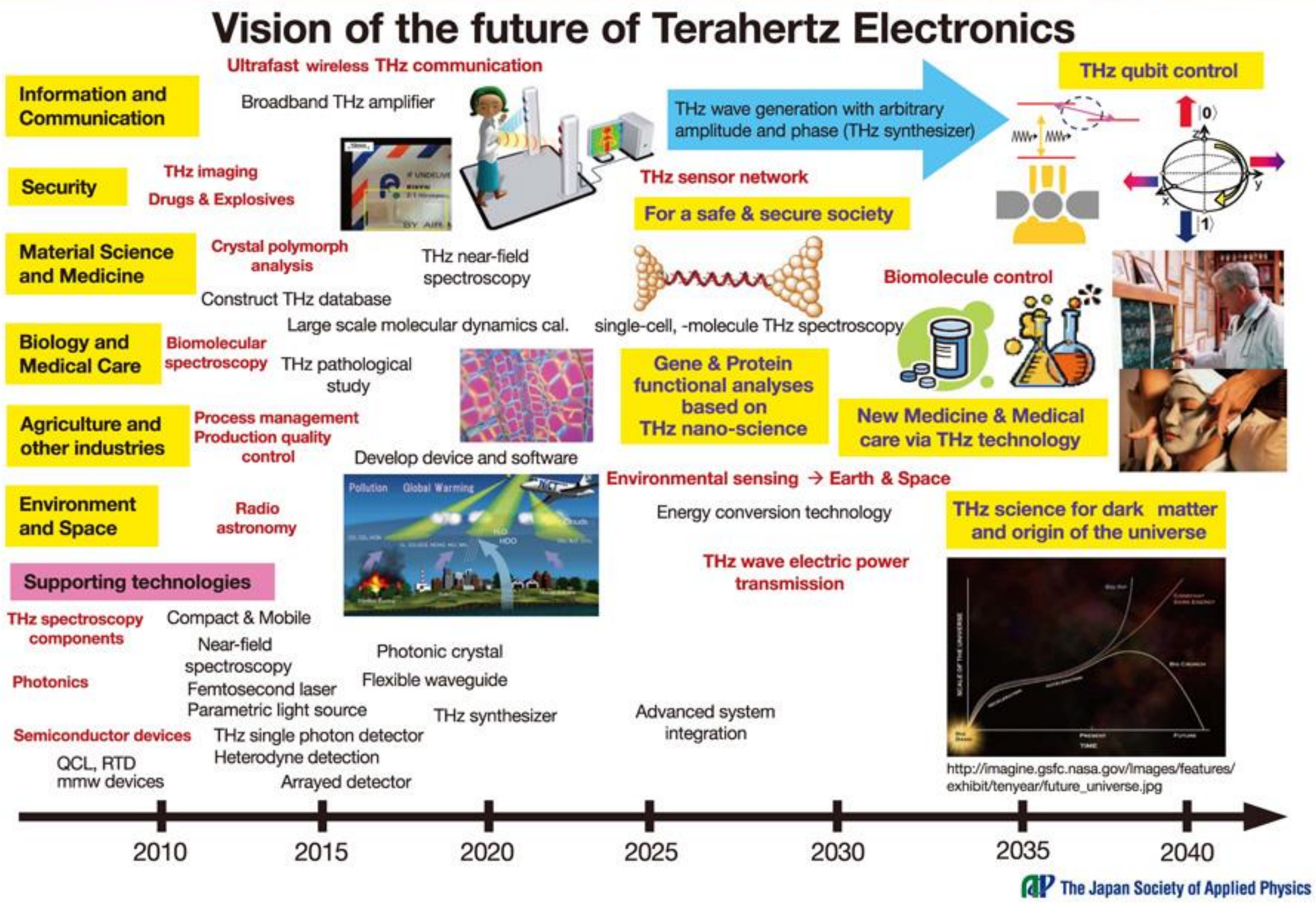
Estimated Year of Production	2014	2015	2016	2017	2018	2019	2020
High Performance MPU properties							
MPU/ASIC metal 1 1/2 pitch (nm)	28	25	22	20	18	16	14
V_{dd} (high performance) (V)	0.8	0.8	0.8	0.7	0.7	0.7	0.7
On chip local clock (MHz)	22,980	33,403	39,683	39,683	53,207	62,443	73,122
MTransistors per cm^2	1,798	2,265	2,854	3,596	4,537	5338	7193
NMOS intrinsic delay τ (ps)	0.21	0.18	0.15	0.13	0.11	0.1	0.08
Clock Period (ps)	44	30	25	25	19	16	14
Global Electronic Interconnect							
Minimum global pitch (nm)	84	75	66	60	54	48	42
Conductor resistivity ($\mu\Omega$-cm)	3.73	3.93	4.2	4.39	4.58	4.93	5.38
RC for 1mm global wire (ps)	1353	1601	2210	2794	2983	4064	5795
bit hop length: RC = clock period (μ)	179	137	107	95	79	63	49
ave electron bit hops to cross chip	98	128	164	184	220	279	360
ave delay or latency (ns)	4.2	3.8	4.1	4.6	4.1	4.5	4.9
MTransistors within bit hop radius	2	1	1.0	1.0	0.9	0.7	0.5
Power for bits at clock speed (mW)	0.34	0.33	0.31	0.21	0.20	0.18	0.17
Energy per bit per hop (pJ)	0.015	0.010	0.008	0.005	0.004	0.003	0.002
Bit flux/Watt (**Tbit**/sec/cm/W)	0.349	0.390	0.390	0.509	0.614	0.614	0.614
Global Photonic Interconnect							
Meindl partition length (μ), N=1	818	679	623	623	538	496	459
Light speed * clock period/3 (μ)	4,352	2,994	2,520	2,520	1,879	1,601	1,368
ave hops to chip edge for photons	4	6	7	7	9	11	13
Mtransistors within photon hop radius	1,069	637	569	717	503	430	422
ave delay or latency (ns)	0.09	0.09	0.09	0.09	0.09	0.09	0.09
Energy per bit to cross chip (aJ)	90	90	90	90	90	90	90
Potential Bit flux/Watt (**Pbit**/sec/cm/W)	11	11	11	11	11	11	11

(b)

Photonic Interconnect Comparison

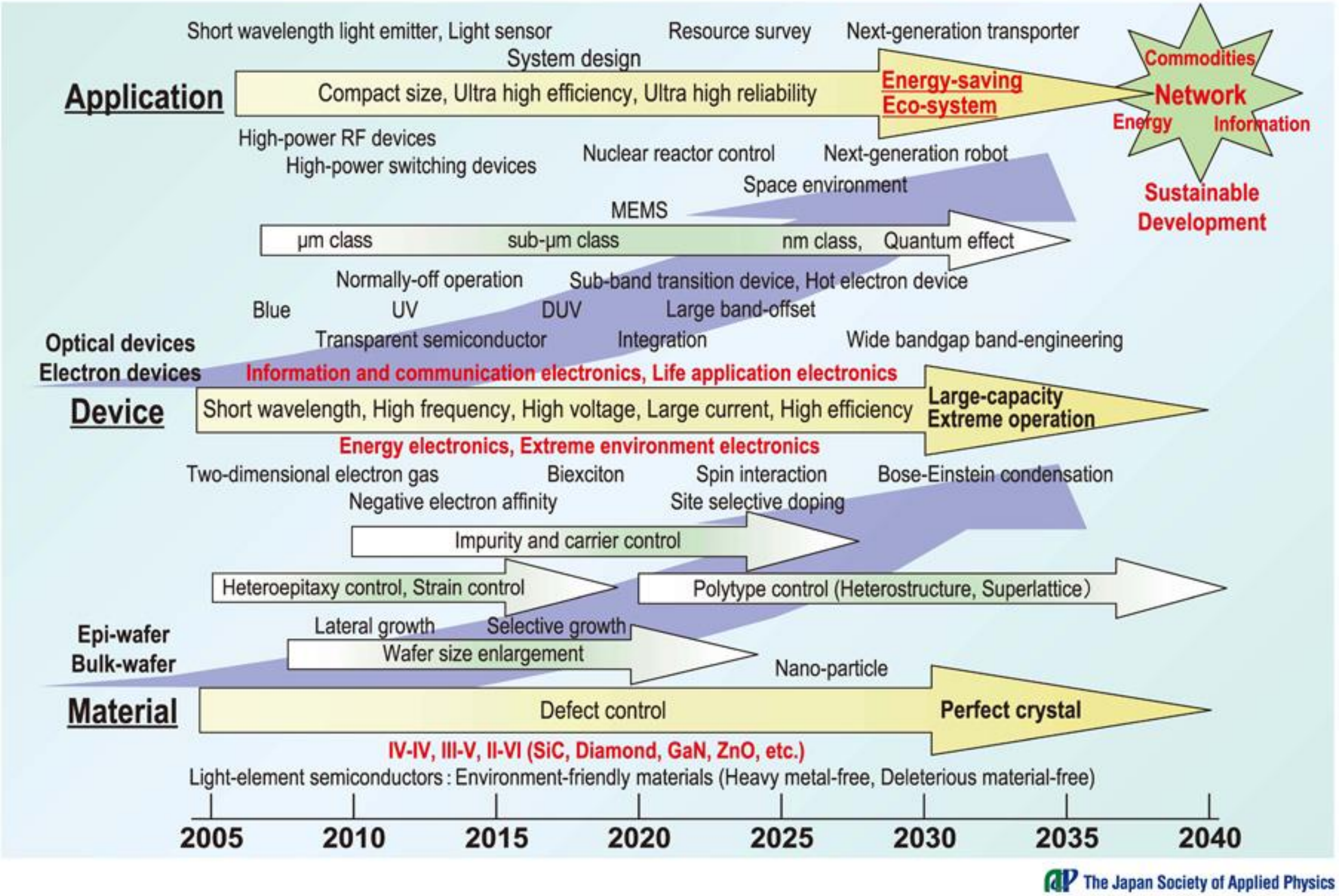
(Ref: Raymond G. Beausoleil et al. Proceedings of the IEEE, Vol. 96, No. 2, February 2008)

Terahertz Electronics



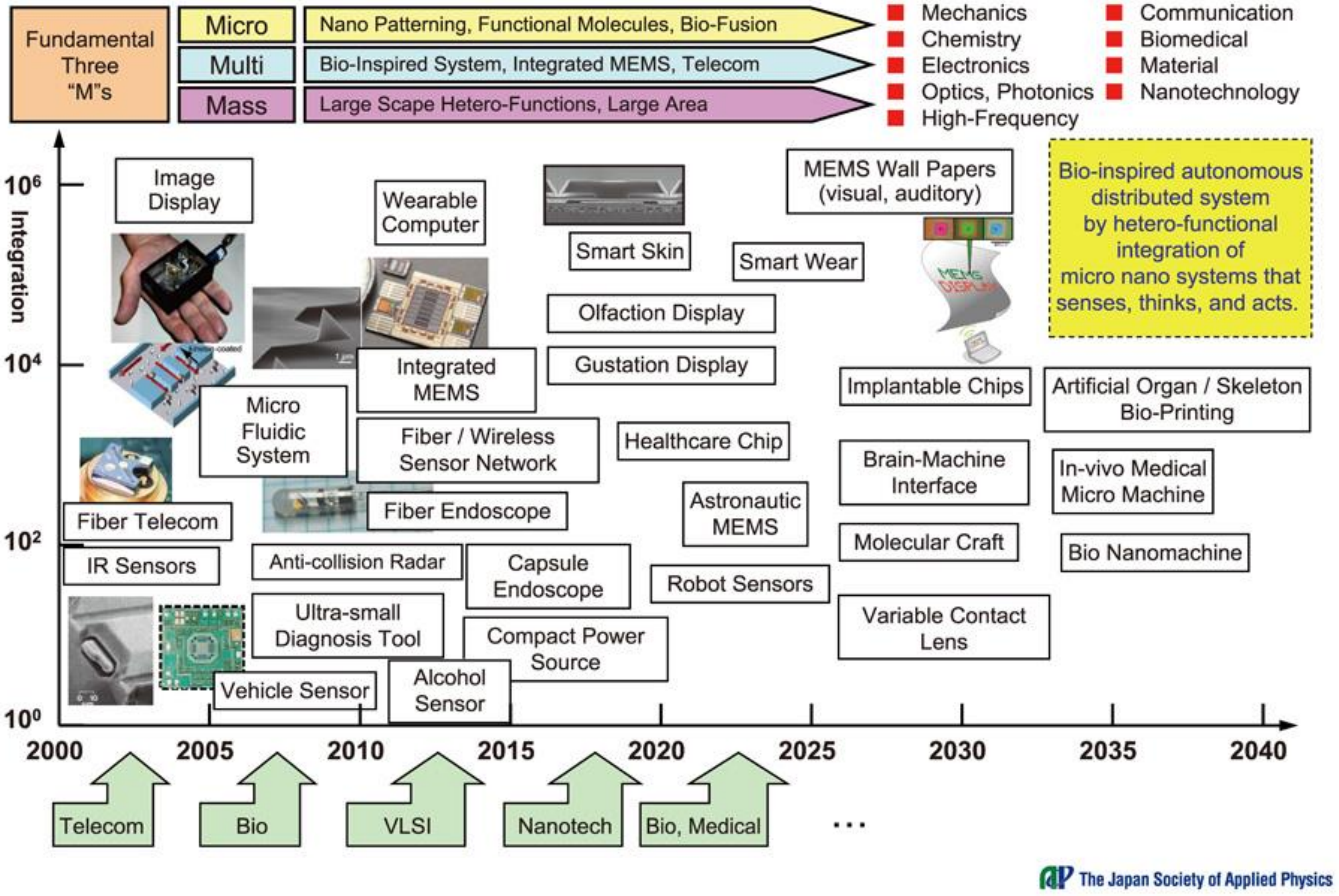
Japan Society of Applied Physics (Academic Roadmap https://www.jsap.or.jp/english/aboutus/academic-roadmap.html)

Widegap Semiconductor Electronics



Japan Society of Applied Physics (Academic Roadmap https://www.jsap.or.jp/english/aboutus/academic-roadmap.html)

Micro/Nano-Mechatronics



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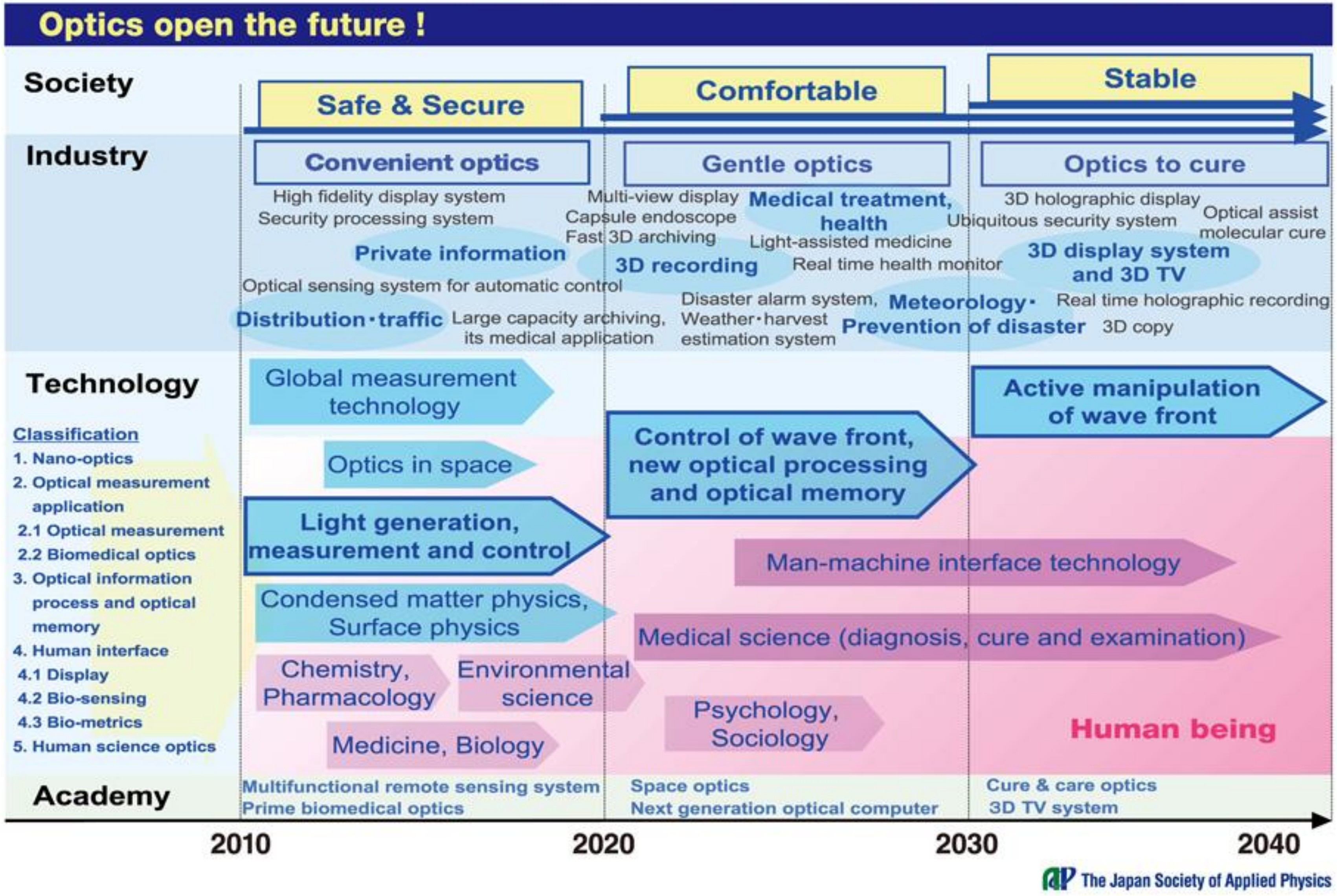
Optics



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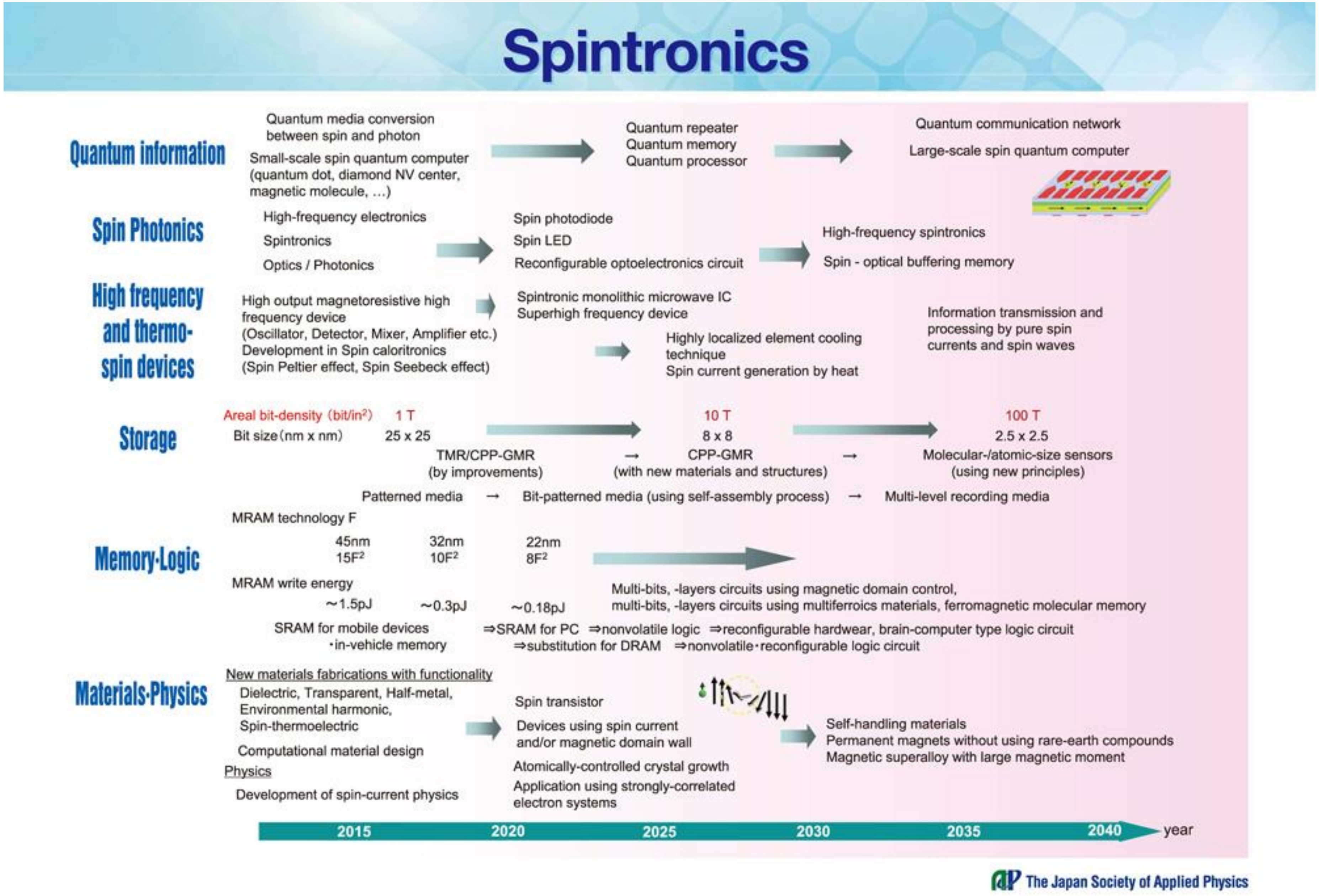

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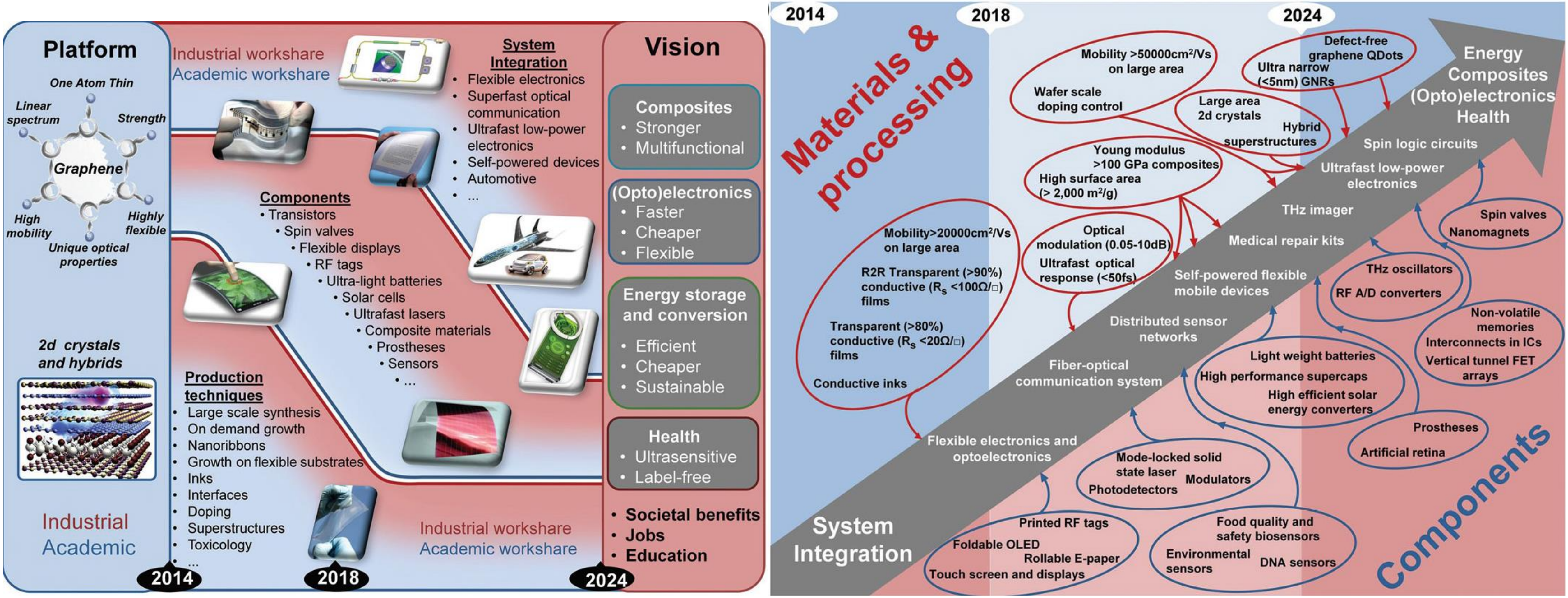
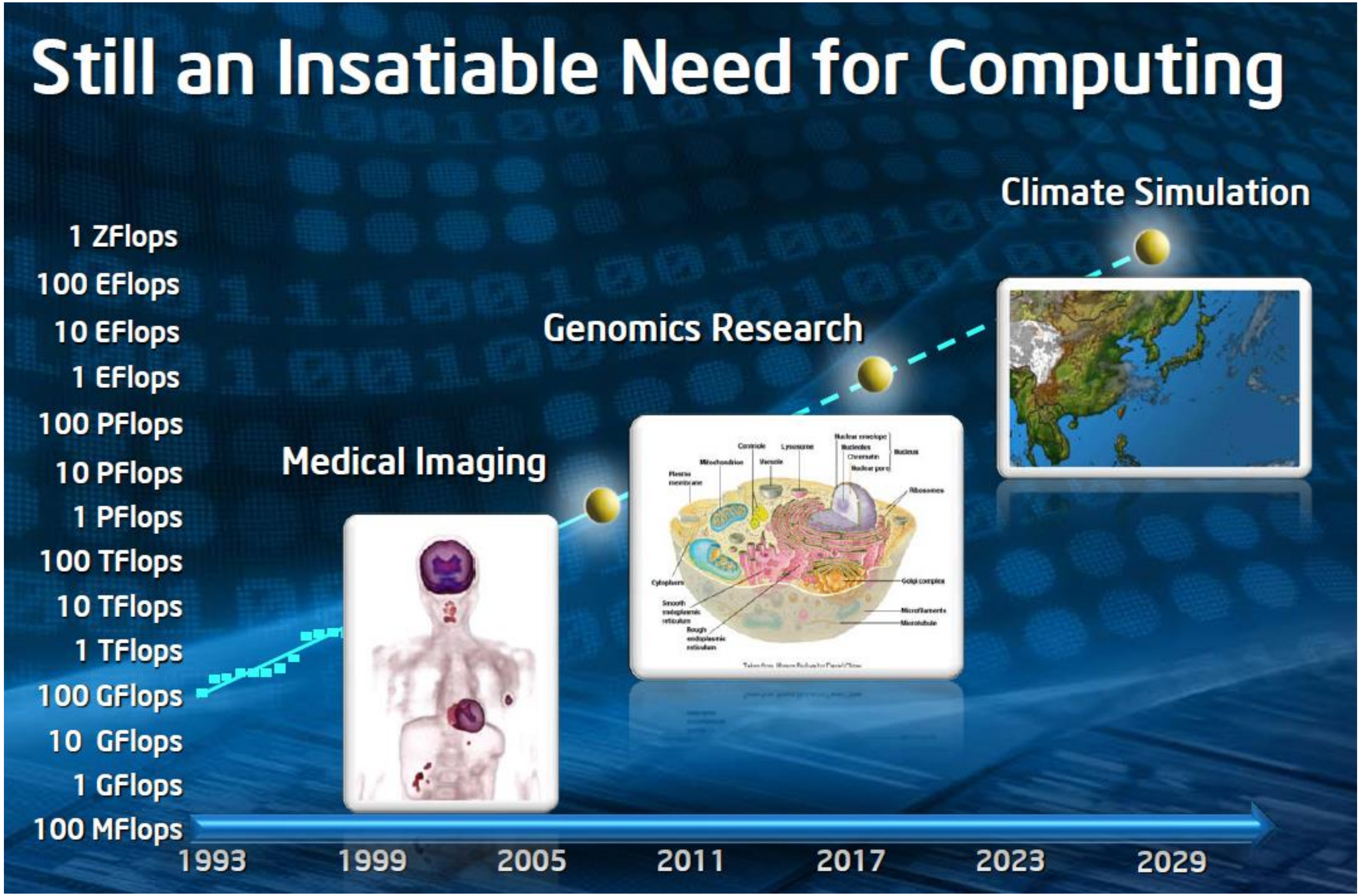
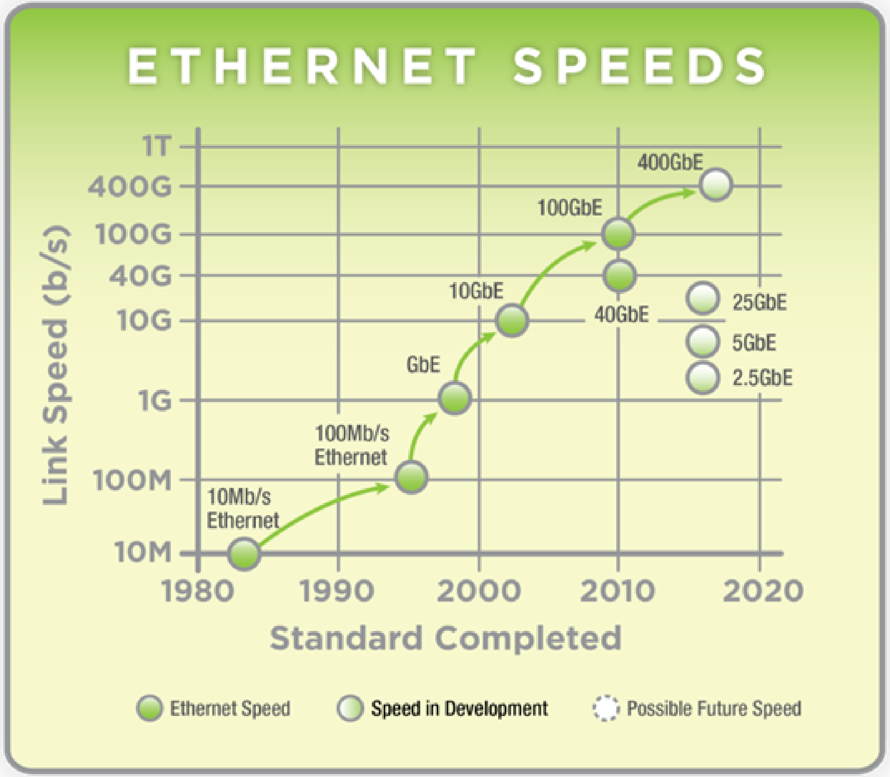


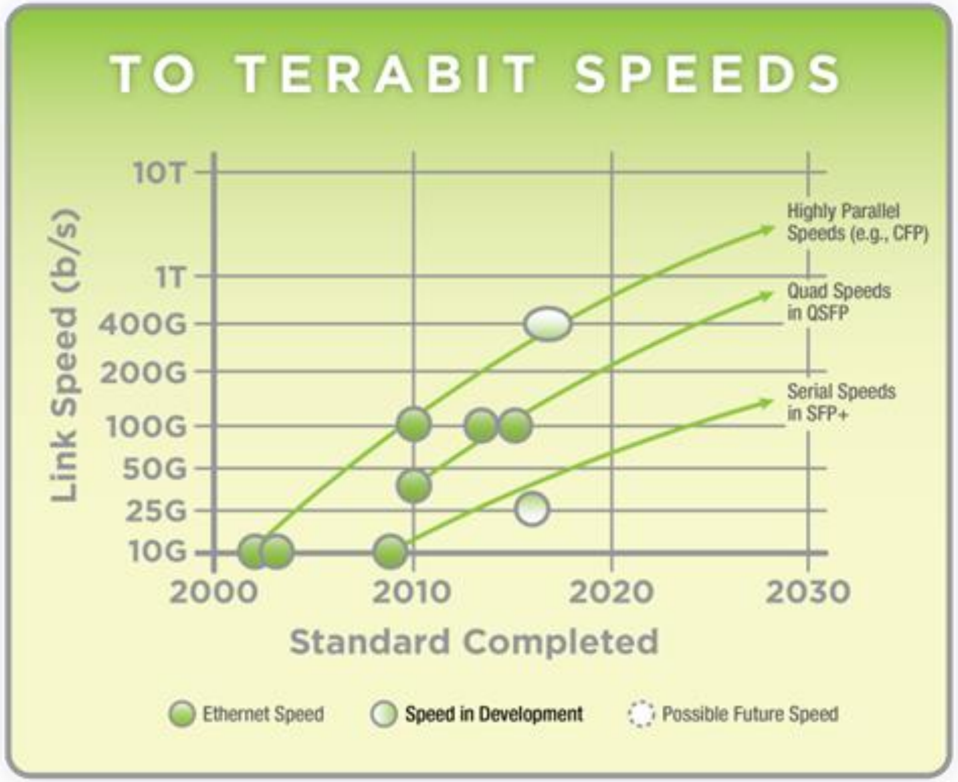
European Technology Roadmap for Graphene

(Ref: Andrea C. Ferrari et. al, Nanoscale, 2015, 7, 4598-4810)



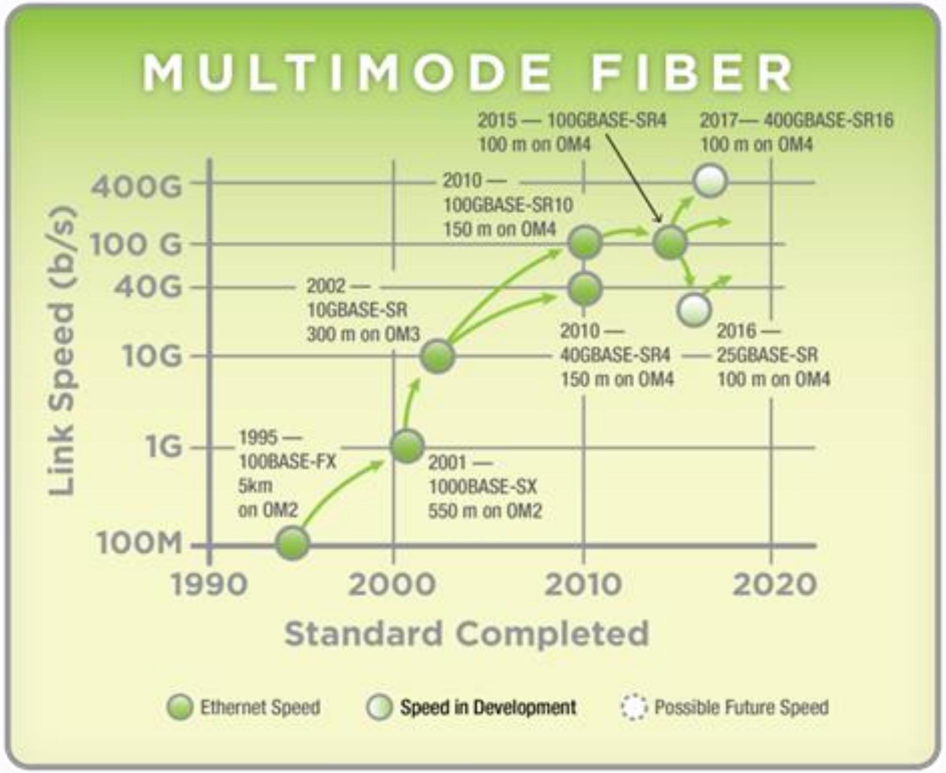
(Ref: http://www.top500.org/)

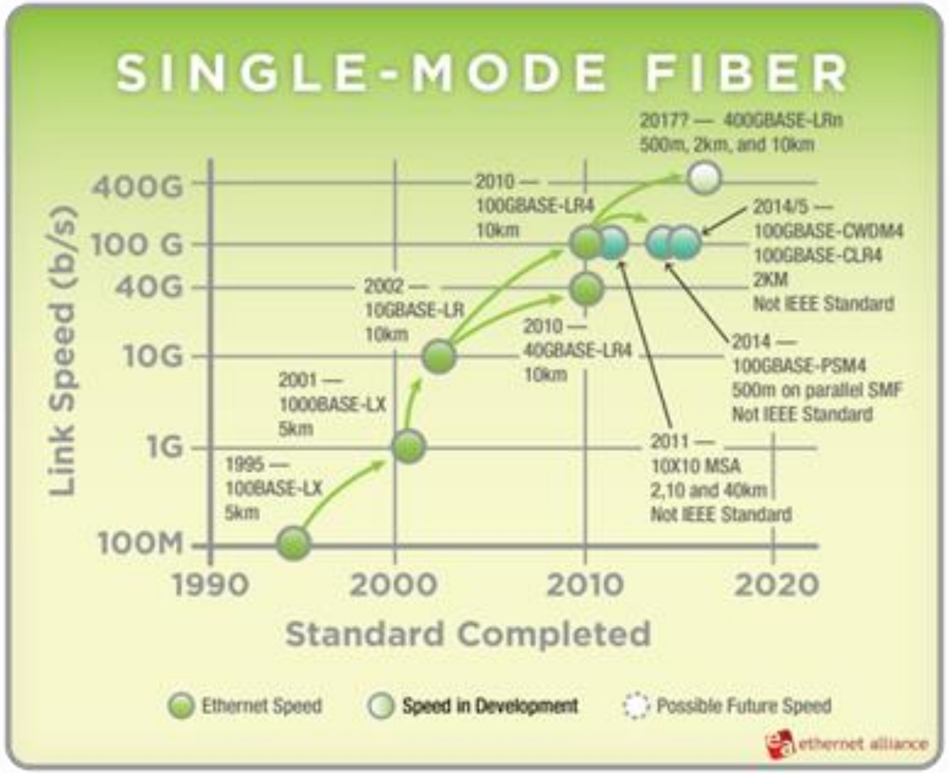




The 2015 Ethernet Roadmap

(Ref: The Ethernet Alliance, http://www.ethernetalliance.org/roadmap/)





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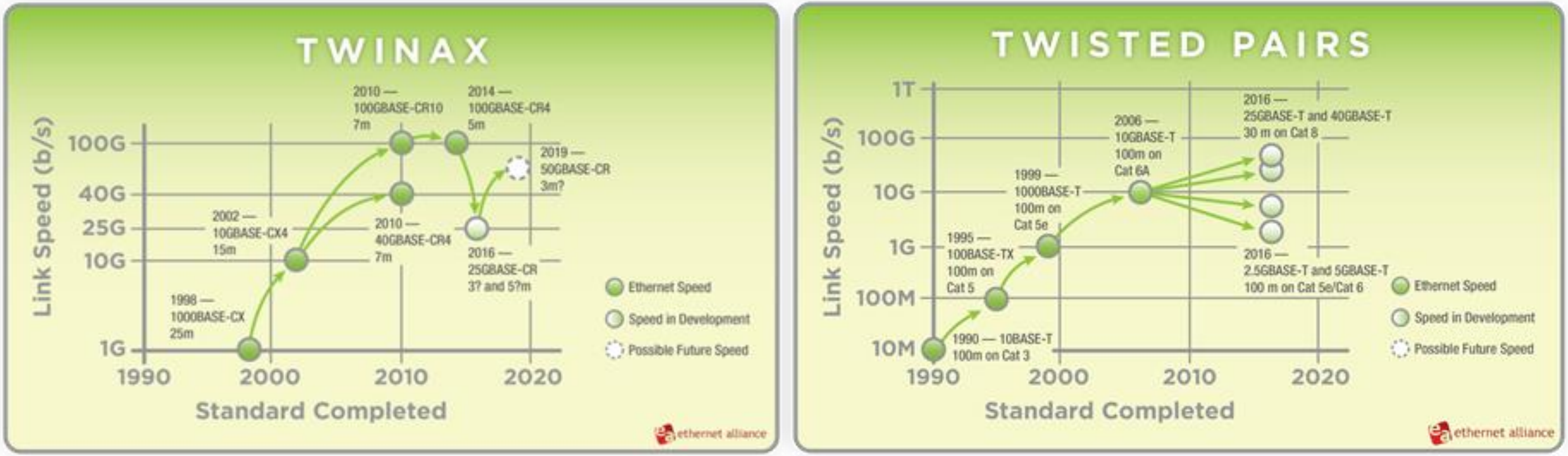
(Ref: The Ethernet Alliance, http://www.ethernetalliance.org/roadmap/)



The 2015 Ethernet Roadmap

(Ref: The Ethernet Alliance, http://www.ethernetalliance.org/roadmap/)

	Petascale system (2012)	Exascale / data center (2020)	Petascale / departmental (2020)	Terascale / embedded (2020)
Number of nodes	[3-8] x10^3	[50-200] x10^3 (20x)	[50-100]	1
Computation (Flop/s & Instructions)	10^15	10^18 (1000x)	10^15	10^12
Memory Capacity (B)	[1-2] x10^14	> 10 ^17 (1000x)	> 10^14	> 10^11
Global Memory bandwidth (B/s)	[2-5] x10^14	> 10^17 (1000x)	> 10^14	> 10^11
Interconnect bisection bandwidth (B/s)	[5-10] x10^13	~10^16 (1000x)	~10^13	N/A
Storage Capacity (B)	[1-10] x10^15	>10^18 (1000x)	> 10^15	> 10^12
Storage bandwidth (B/s)	[10-500] x10^9	> 10 x10^12 (1000x)	> 10 x10^9	> 10^6
IO operations/s	100 x10^3	> 100 x10^6 (1000x)	> 100 x10^3	> 100
Power Consumption (W)	[.5-1.] x10^6	< 20 x10^6 (20x)	< 20 x10^3	< 20

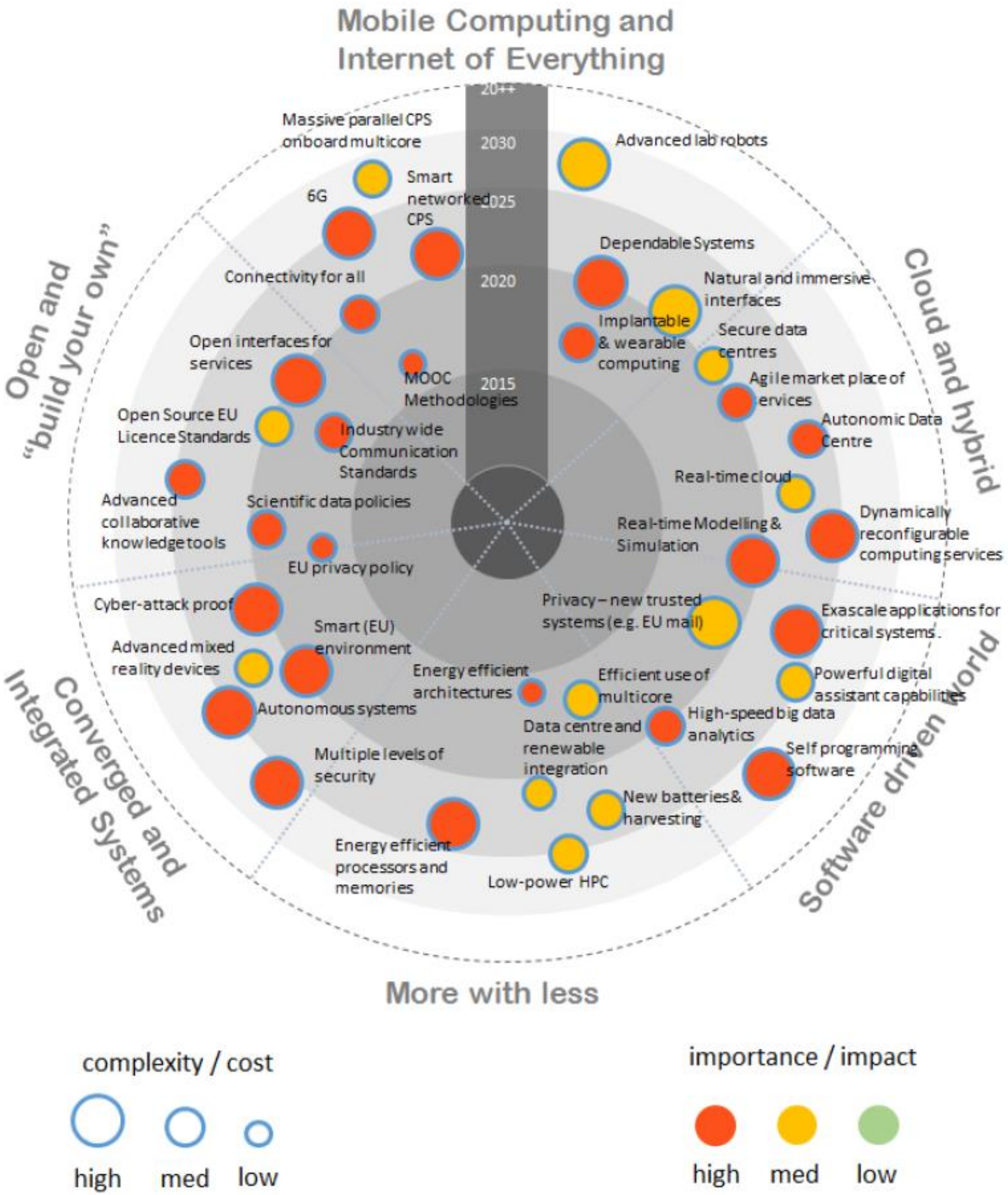
HPC Expected system characteristic 2020

(Ref: The European Technology Platform for High Performance Computing
http://www.etp4hpc.eu/publications/key-documents/)

	Traditional technologies			Emerging technologies			
Memory type	DRAM	SRAM	NAND	FeRAM	STT-MRAM	PCRAM	ReRAM
Physical effect at work	Silicon	Silicon	Tunnel effect	Ferroelectrics	advanced Spintronics	Phase-Change	Redox / Memristor
Technology status	Mature			product	products being introduced	1st Generation	Research
Read time (ns)	<1	<0.3	<50	<45	<20	<60	<50
Write erase time(ns)	<0.5	<0.3	10^6	10	10	60	<250
Retention time (years)	N/A	N/A	>10	>10	>10	>10	>10
Write endurance (nb of cycles)	10^16	10^16	10^5	10^14	10^16	10^9	10^15
Density (Gbit/cm2)	6.67	0.17	2.47	0.14	1	1.48	250
Technology potential scalability	Major technological barriers			Limited	Promising	Promising	Promising
Exascale applicability	No recognised alternative	Potential to scale suitably?	Tech barriers and endurance, may be overtaken by other NV devices	Unlikely	Promising, potential successor for DRAM	Very Promising	Unclear, potential as compatible SoC device

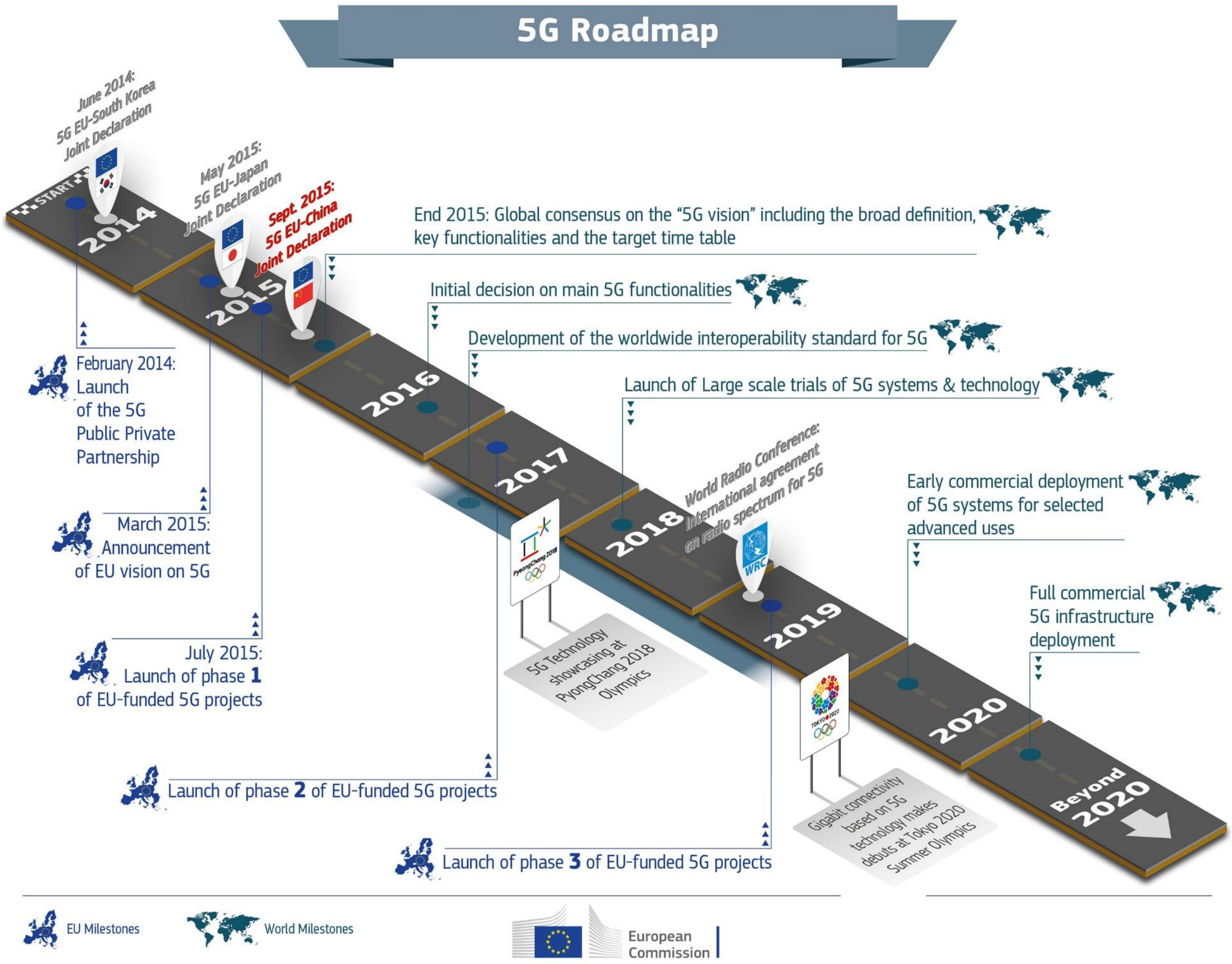
Expected memory characteristics ranges in 2020

(Ref: The European Technology Platform for High Performance Computing
http://www.etp4hpc.eu/publications/key-documents/)



Next Generation Computing Roadmap

(Ref: Study carried out for the European Commission by eutema GmbH (Austria) in co – operation with Optimat, EPCC and 451 Research, 2014, https://ec.europa.eu/digital-agenda/en/news/next-generation-computing-roadmap)



(Ref: European Commission

https://ec.europa.eu/digital-agenda/en/5G-international-cooperation)