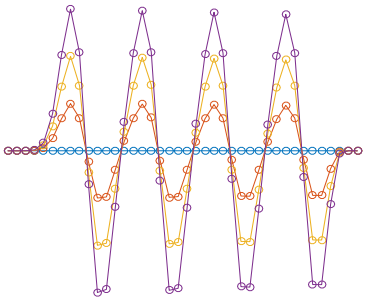
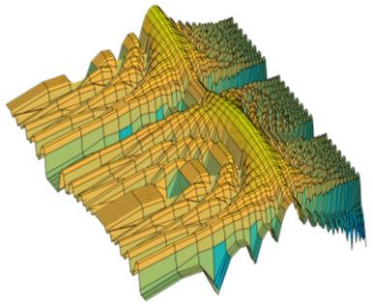
Digital Signal Processing Techniques to Monitor Bunch-by-bunch Beam Positions in the LHC for Machine Protection Purposes

Jan Pospisil, O. Bjorkqvist, A. Boccardi, M. Wendt

BE-BI-QP, CERN

8. 12. 2017



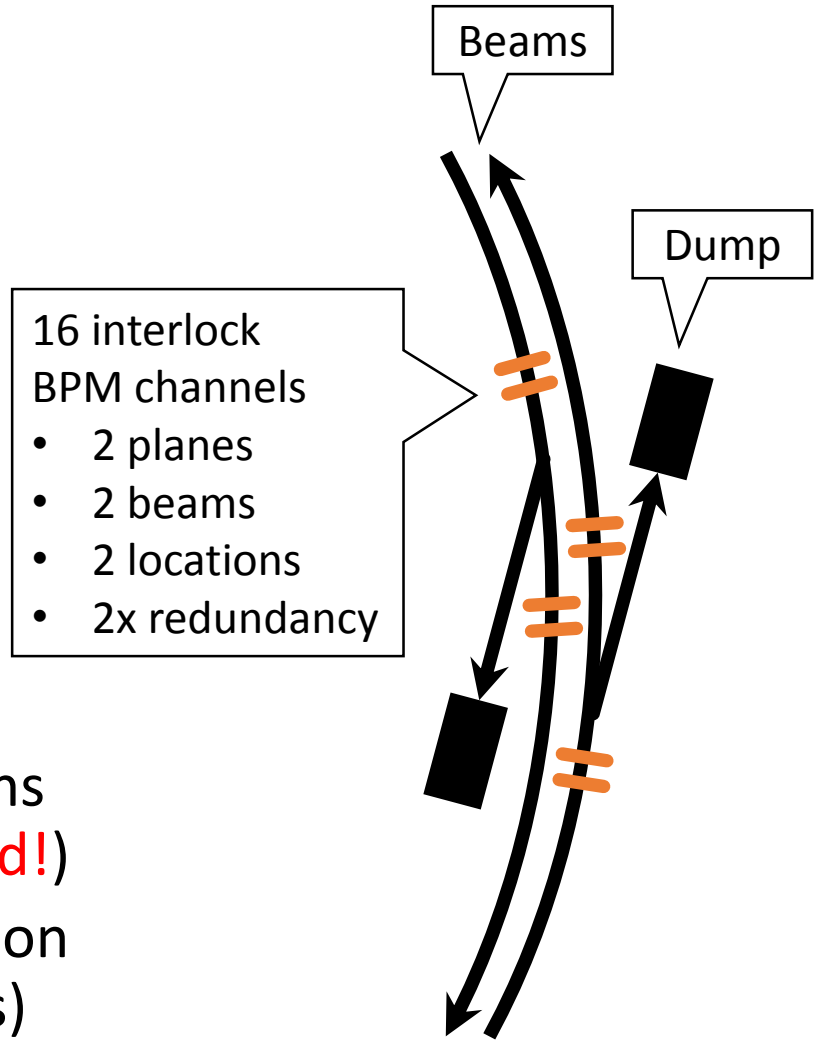


Outline

- Introduction
- Chosen Approach
- Performance Estimation
- Prototype Performance

Introduction

- LHC interlock BPM system
  - Protects beam dump, by continuously monitoring the beam position
  - Real time, bunch-by-bunch, failsafe system
- Limitations of present system
  - Bunch spacing needs to be > 25 ns (20-5 ns doublets are not covered!)
  - Sometimes unstable beam position (due to aging, temperature drifts)
  - Beam position offset at low bunch intensity
    - May cause an unnecessary beam abort



System Requirements

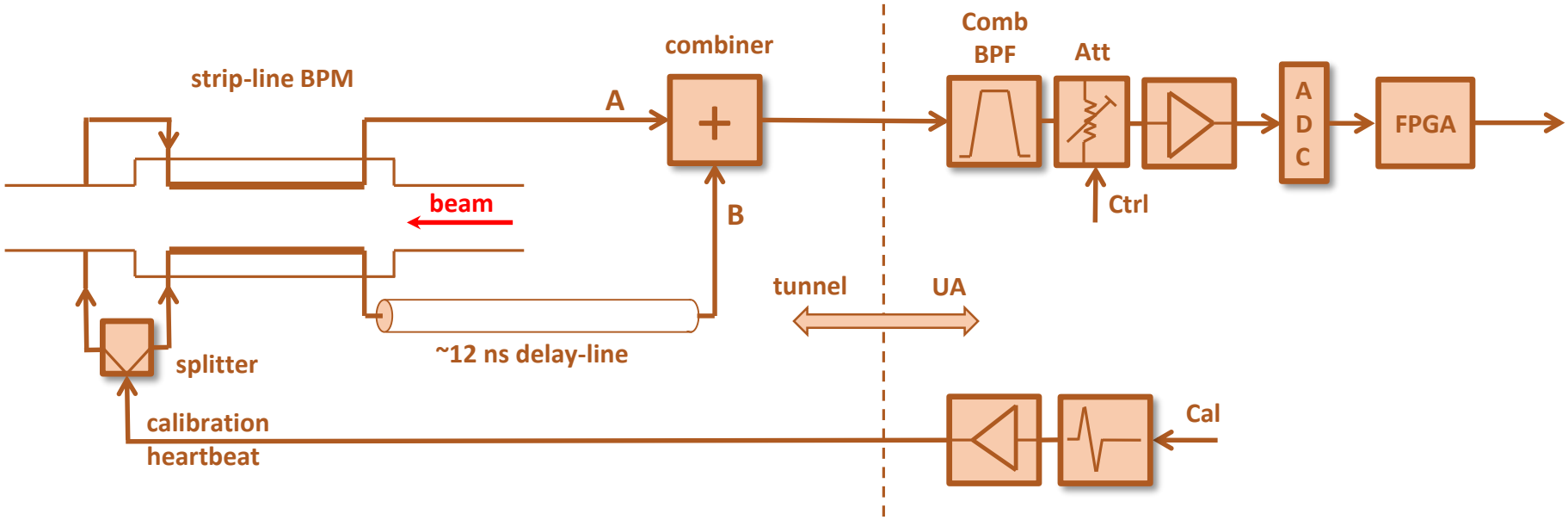
Single bunch:
- Protons
  1.5×10^{9} – 3×10^{11} cpb
- Ions
  1×10^{9} – 5×10^{10} cpb

- Bunch-by-bunch measurement
- Cover bunch intensity range throughout a LHC fill
  - Single fill without gain switching: 1×10^{10} – 2×10^{11} cpb
- Position
  - Beam-abort threshold: ~3 mm
  - Position range to be covered: ±7.5 mm
- Resolution for a given intensity range setting: <100 µm

Chosen Approach

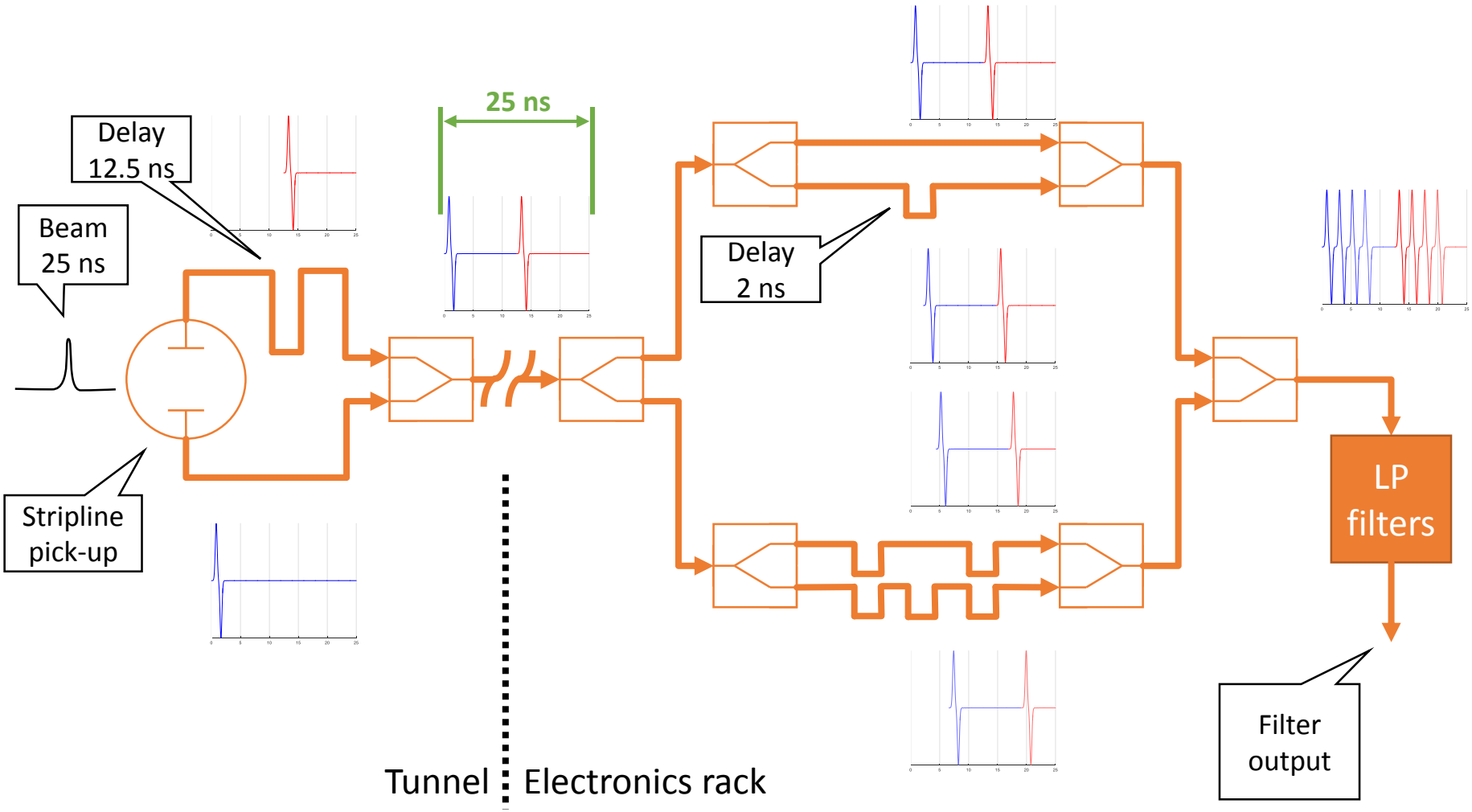
Chosen Approach – Overview

- Single processing chain for both electrodes
  - Minimize drifts and aging problems

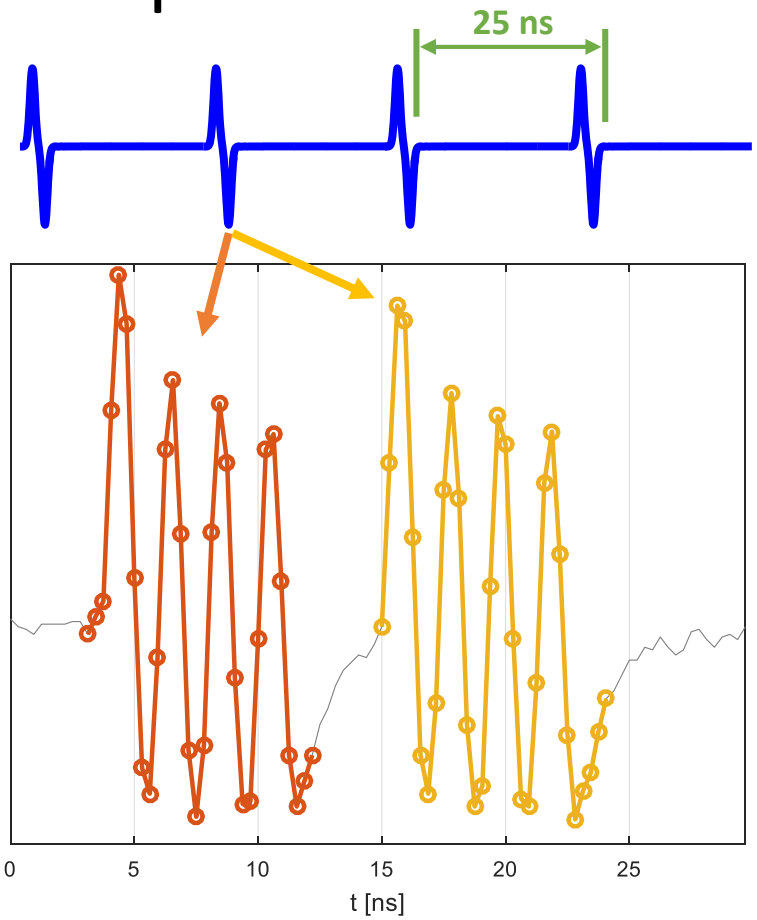


- Direct signal digitization by an ADC
  - Prototype with Texas Instruments ADC12J4000
    12 bits, 3.2 GSa/s, ~ 8.7 ENOB

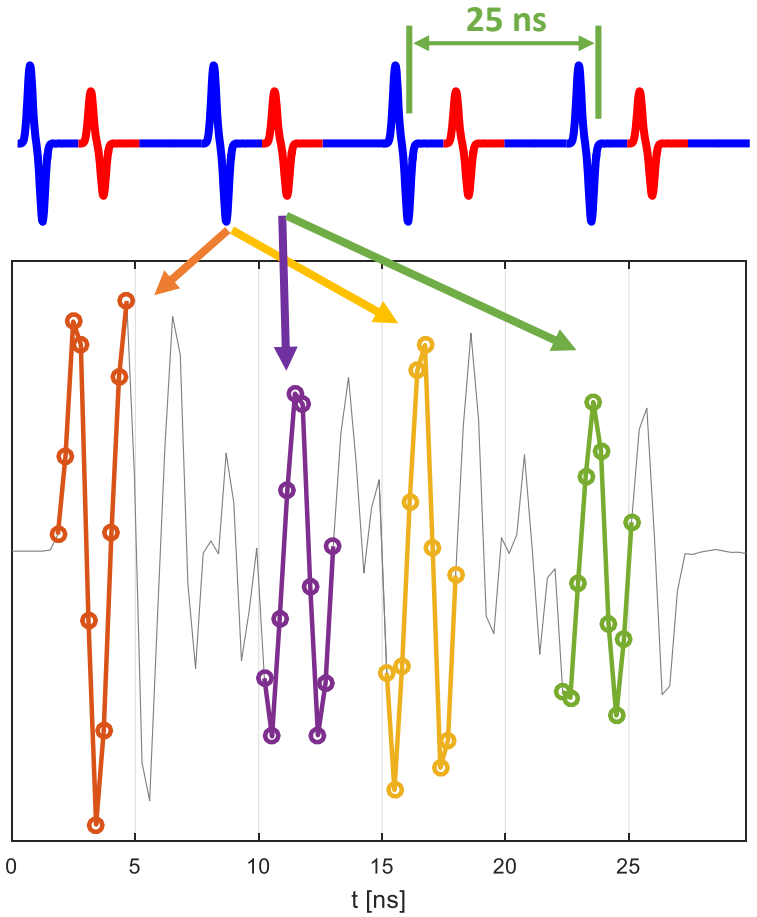
Band-pass Comb Filter



Expected ADC data



Single bunch (measured)



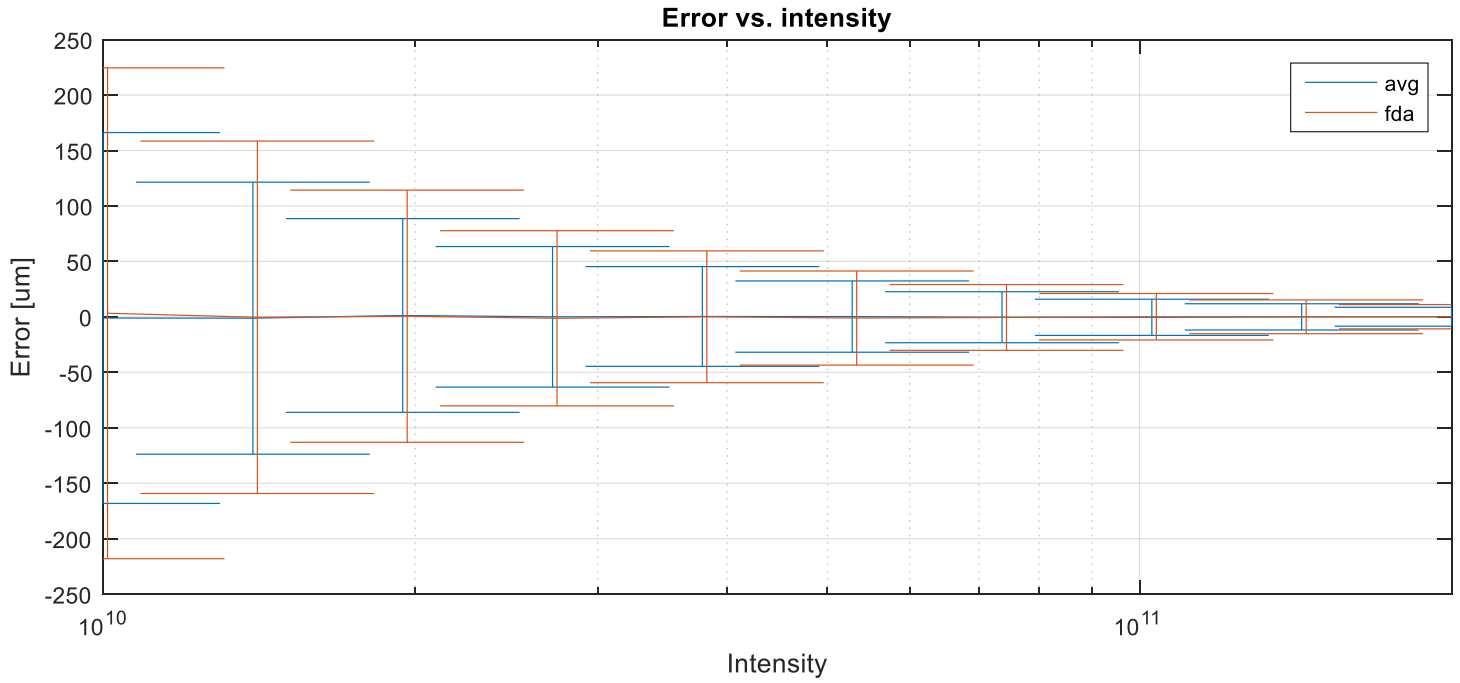
Doublet bunch (simulated)

Performance Estimation

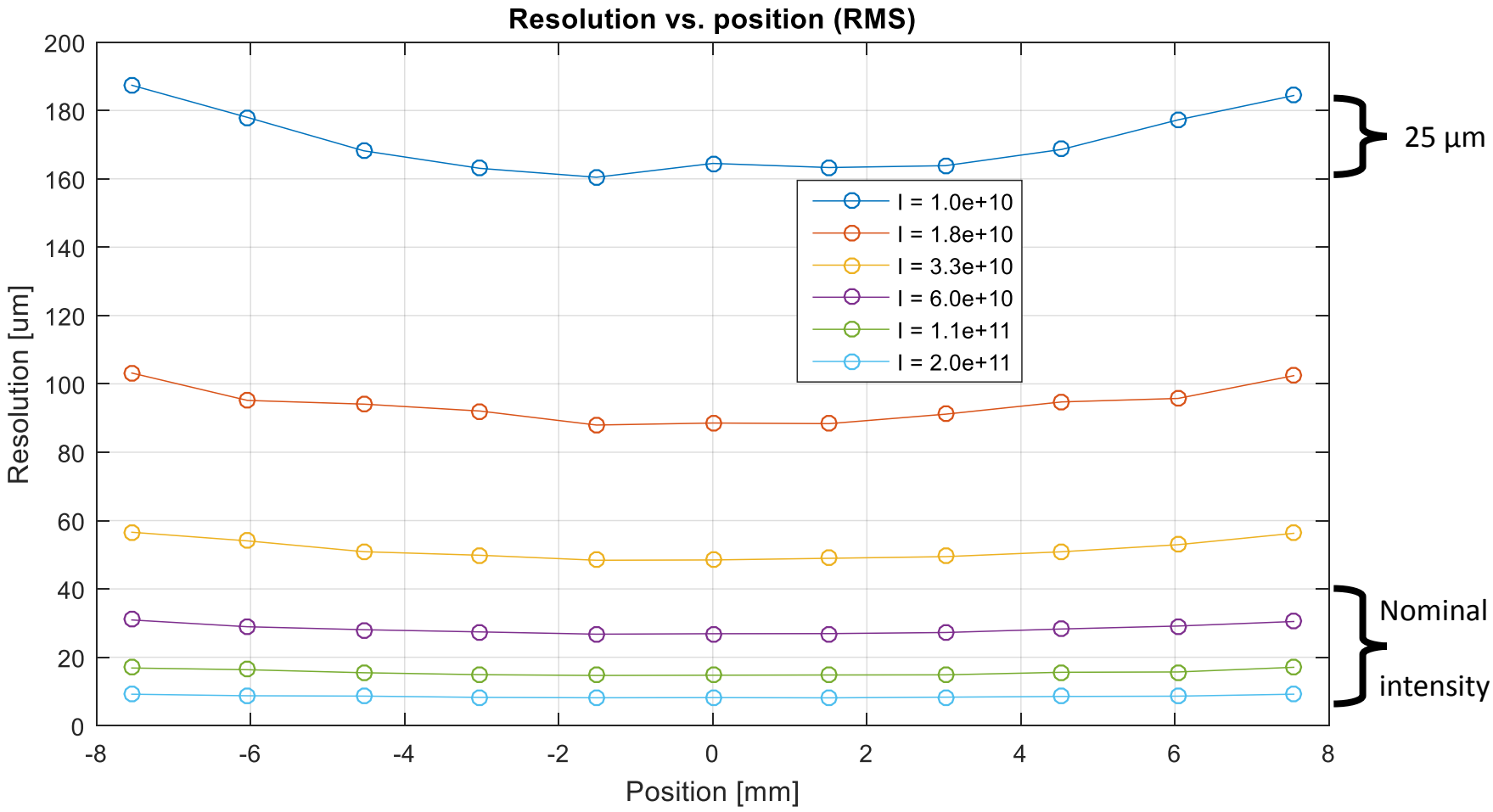
Simulation Results (1)

- Sensitivity to intensity
  - Resolution $< 100\ \mu m$ for $\mathrm{I} > 1.6\mathrm{e}10$ for AVG algorithm

Sim. parameters:
- 12 bits @ 3.2 GHz
- Random position
- Random time shift
- $\sigma_{noise} = 380\ \mu V$

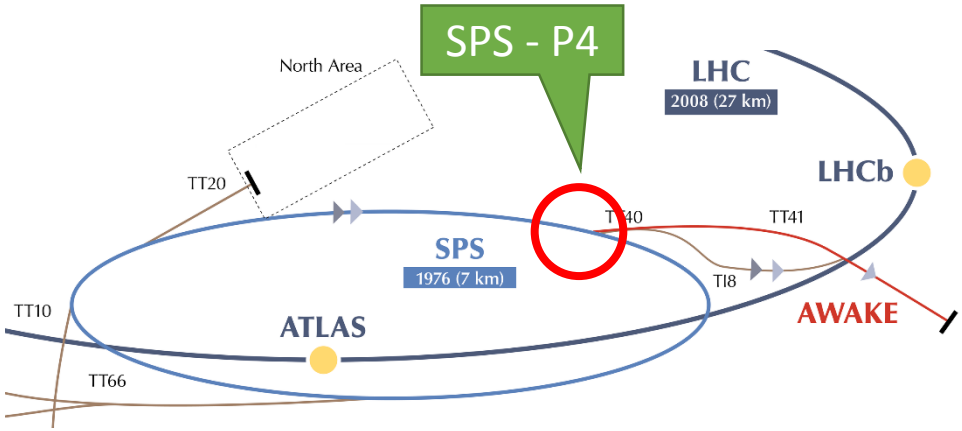


Simulation Results (2)



Prototype Performance

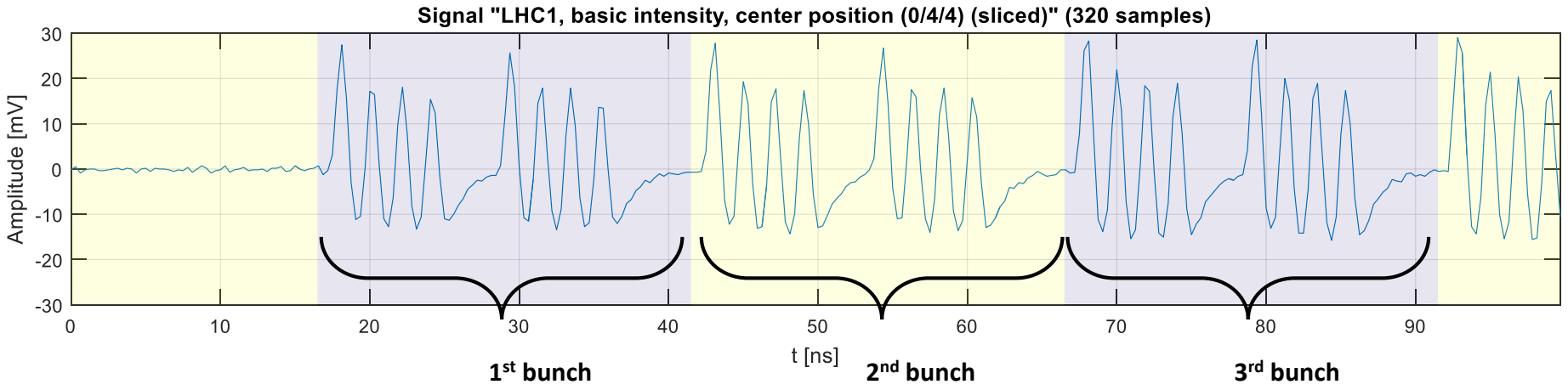
Test Setup



- Conditions
  - SPS point 4
  - Acquisition at flat-top
  - Two measurement campaigns
    - M1: One electrode split – emulated beam position
    - M2: Both electrodes – real beam position scan
- Hardware & Software
  - SPS button pick-up, vertical plane
  - Prototype of comb filter
  - Commercial ADC mezzanine (Vadatech FMC225)
  - CERN BE-BI VME carrier (VFC-HD)
  - Python script for read-out, MATLAB for analysis

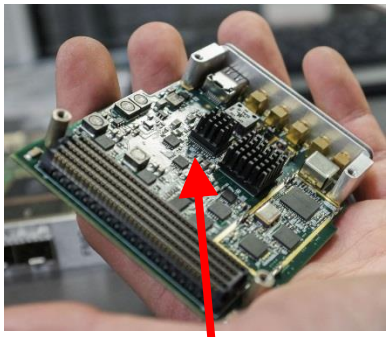
Measurement Details

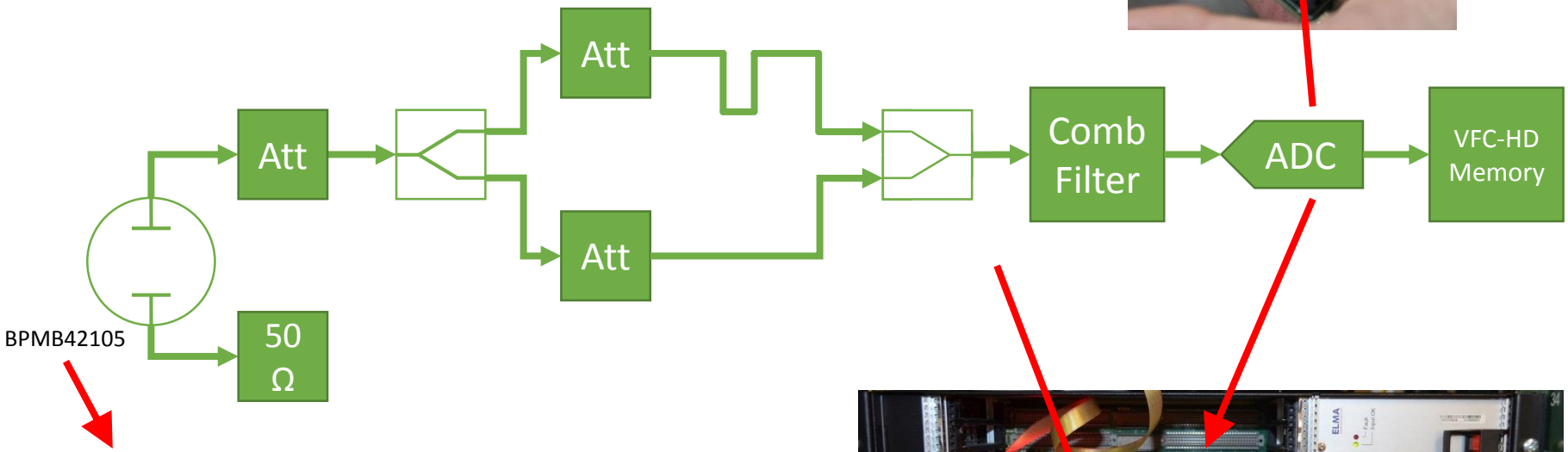
- Typical single-turn acquisition (first 100 ns):

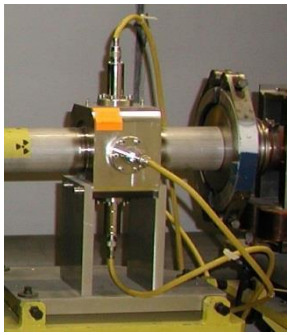


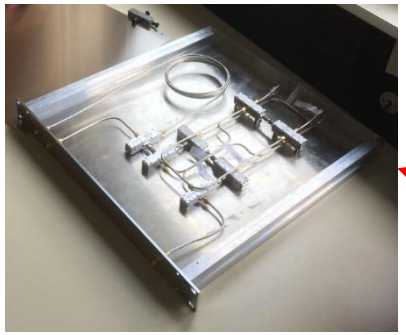
- Position calculated by RMS algorithm
- Position mean and std. dev. calculated in [mm] from >2000 turns.

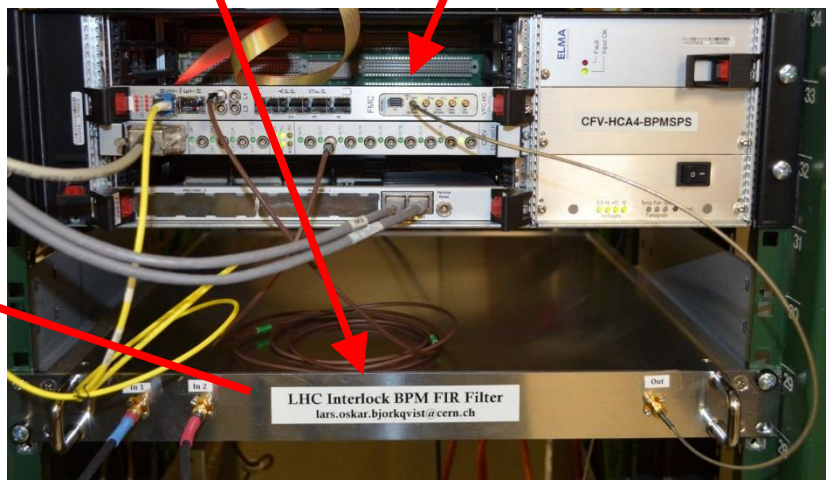
M1: Test Setup



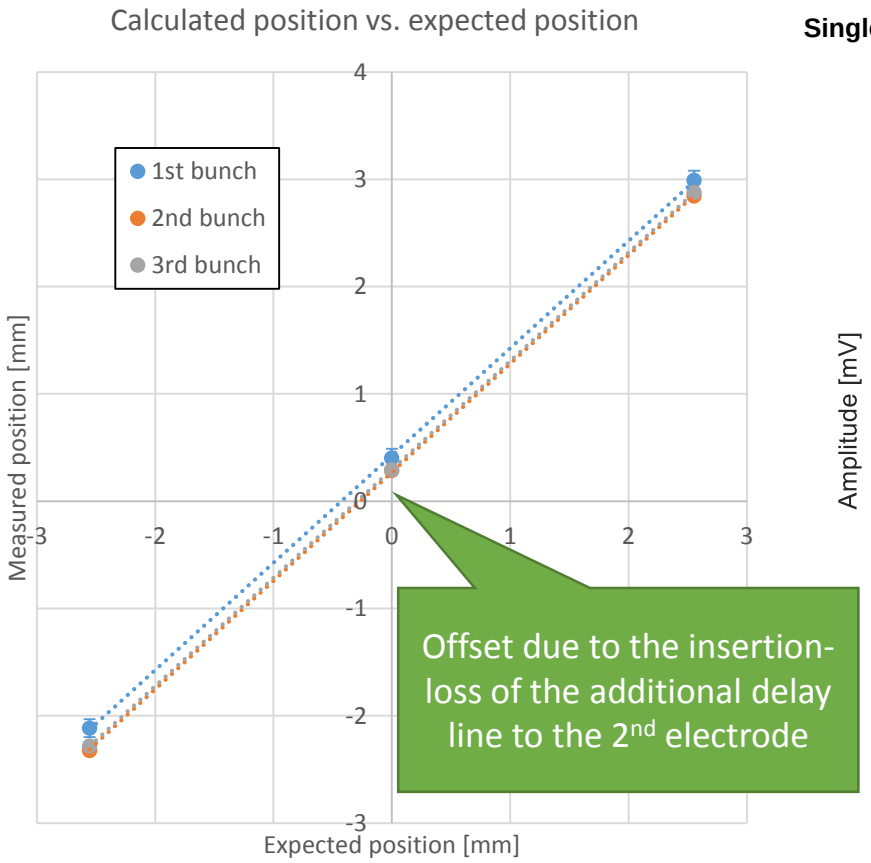




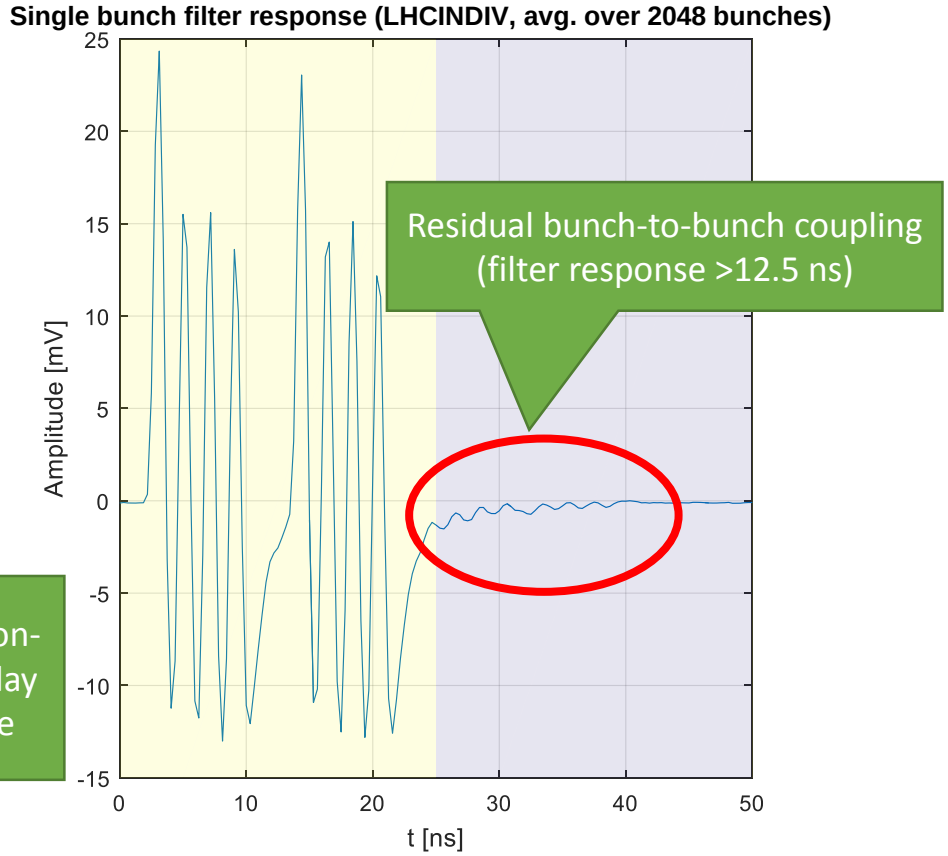




M1: Results

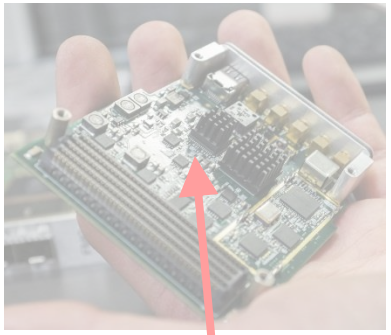


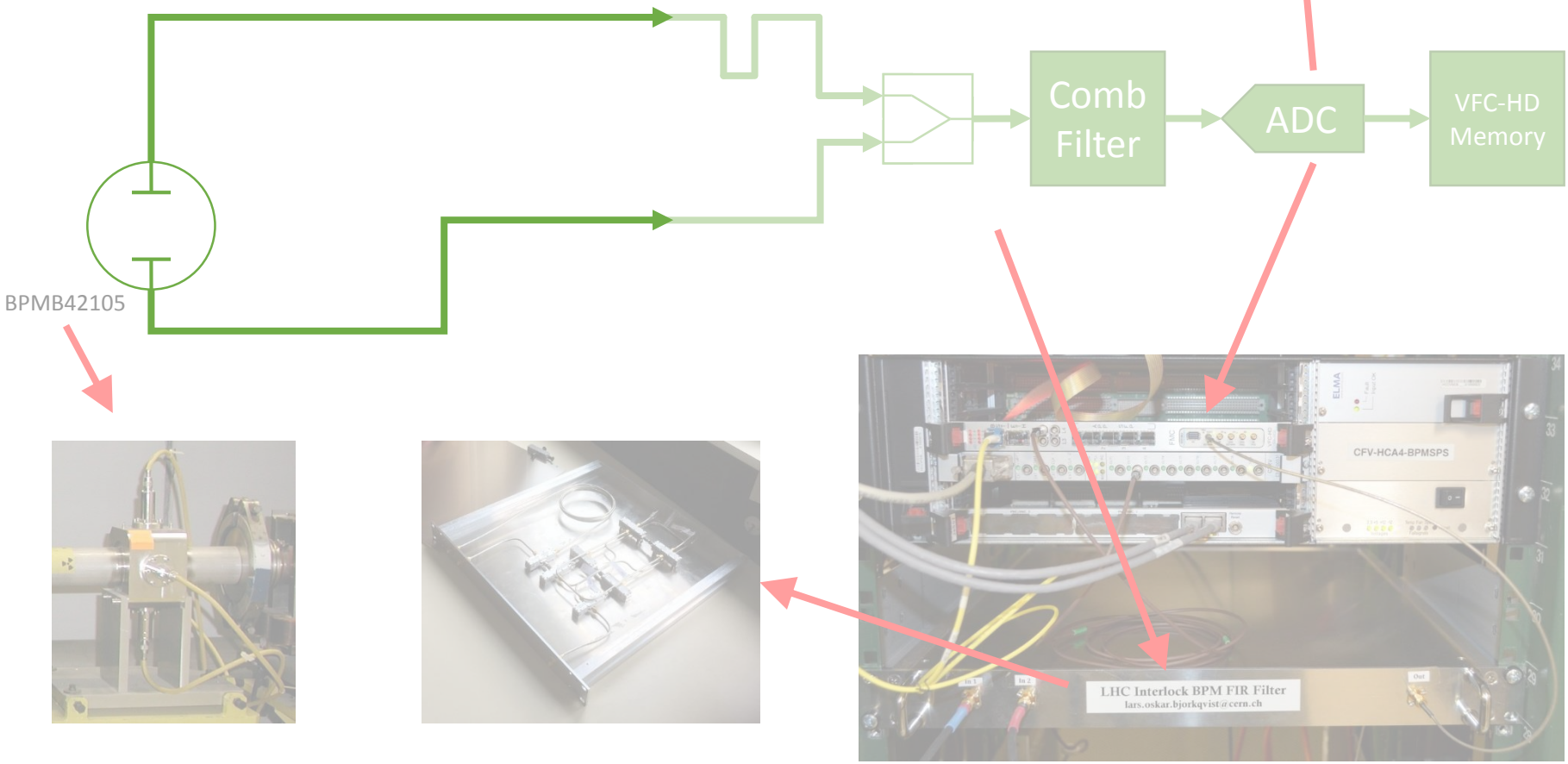
Offset due to the insertion-loss of the additional delay line to the 2nd electrode



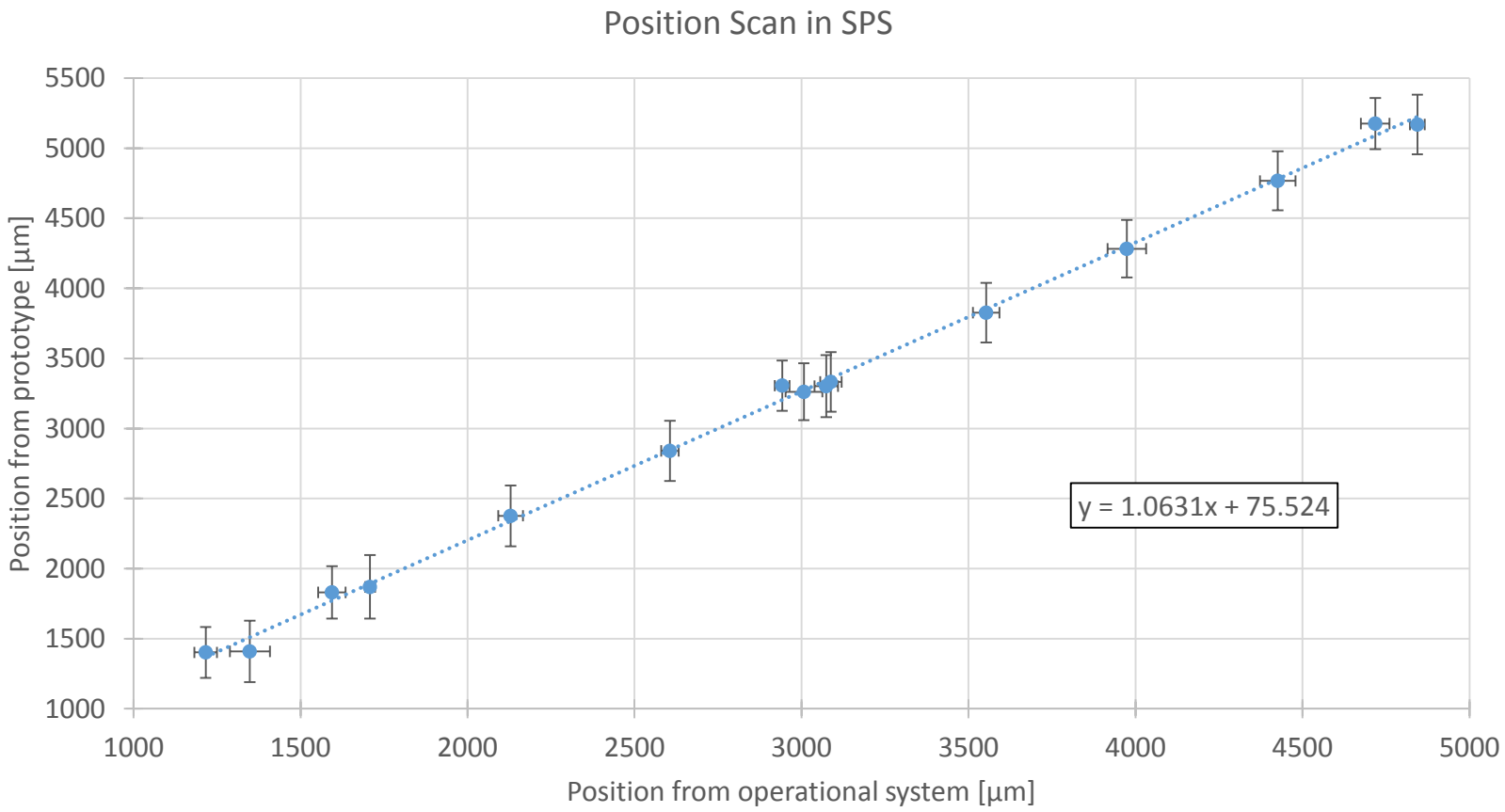
Residual bunch-to-bunch coupling (filter response >12.5 ns)

M2: Test Setup

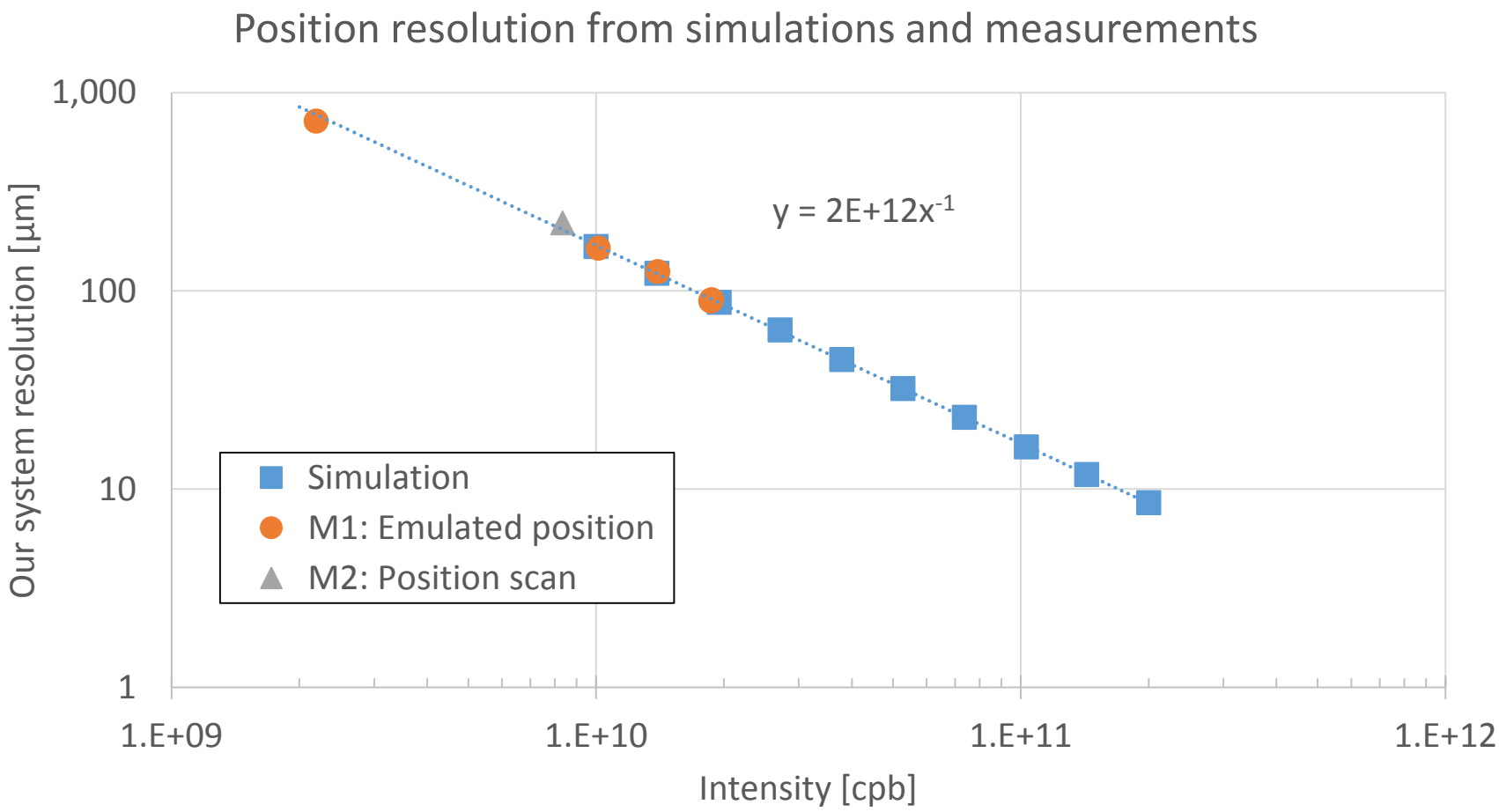




M2: Results


Position Scan in SPS
Position from prototype [µm]
Position from operational system [µm]
y = 1.0631x + 75.524
5500
5000
4500
4000
3500
3000
2500
2000
1500
1000
1000
1500
2000
2500
3000
3500
4000
4500
5000

Crosscheck With Simulation



Comb BP Filter: Proof of Concept

- Initial design for system evaluation:
  - Successful tests.
  - Beam measurements in the LHC and SPS.
- Improper to use this design for final system
  - Difficult to reproduce (hand made)
  - Possibly too low power handling capacity

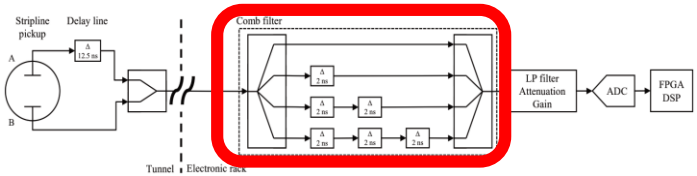


Fig 1. Interlock BPM system architecture.

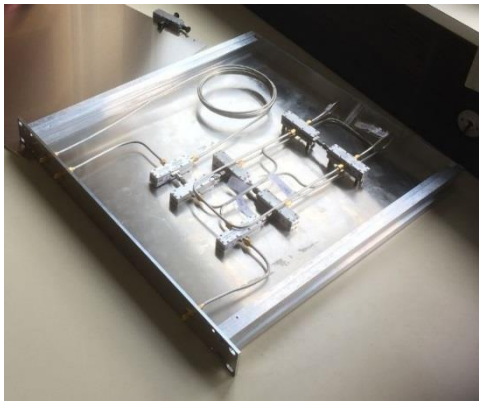


Fig 2. Proof of concept filter installed in rack box.

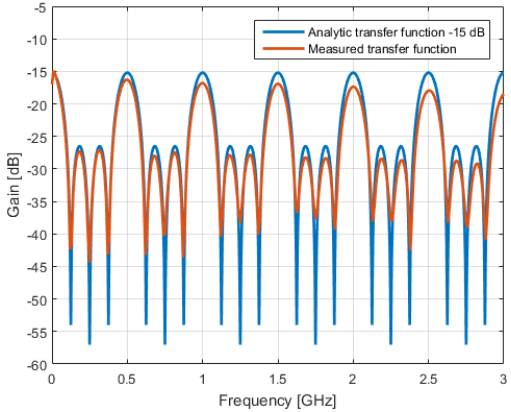


Fig 3. Filter frequency response.

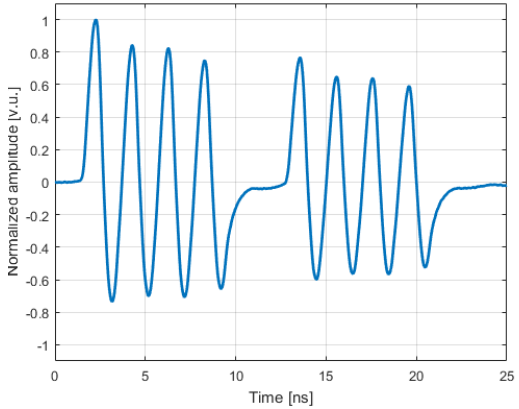


Fig 4. Beam measurement with filter.

Comb BP Filter: PCB Design

- Development of power dividers with proper power rating
- Development of full filter in PCB configuration
  - First prototype manufactured
  - Beam measurement show promising results
  - Improved impulse response without ringing!

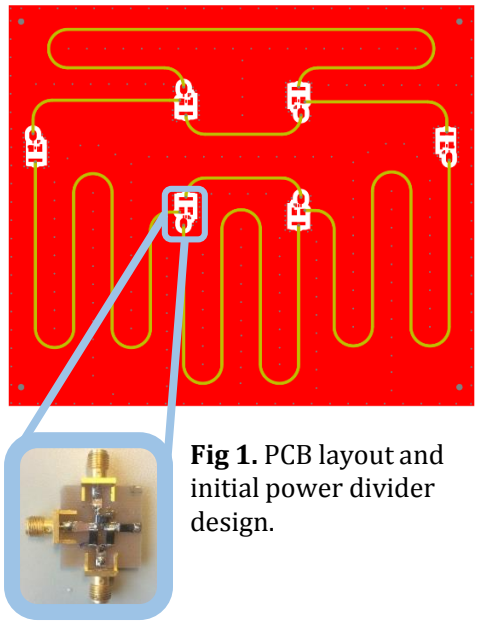


Fig 1. PCB layout and initial power divider design.

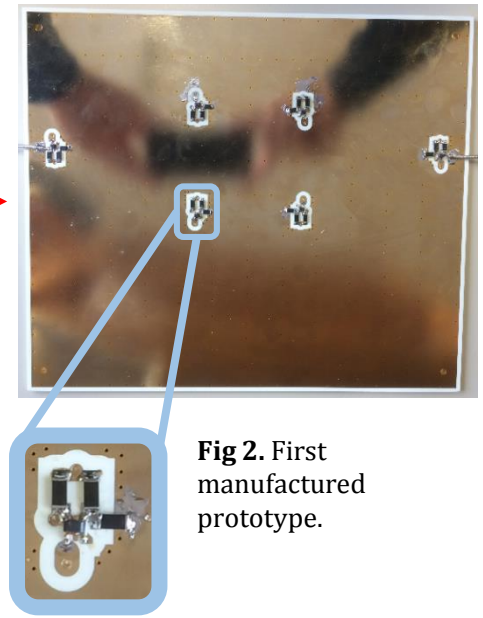


Fig 2. First manufactured prototype.

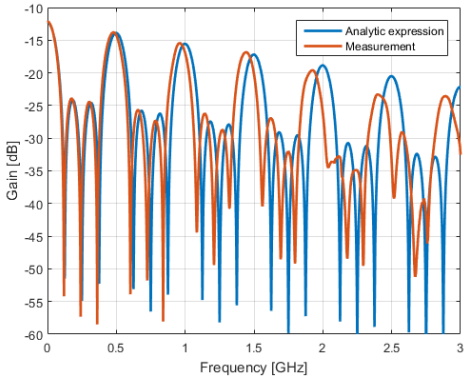


Fig 3. Frequency response of PCB filter.

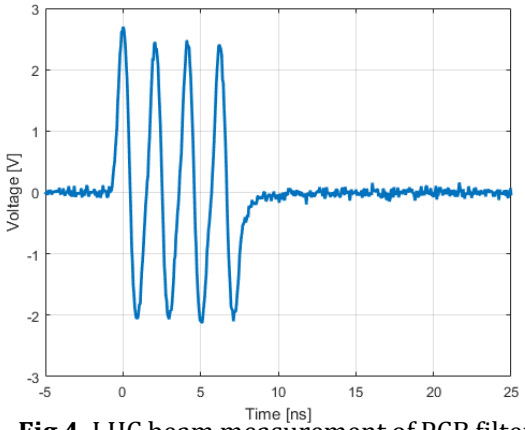


Fig 4. LHC beam measurement of PCB filter at 1.35e11 bunch intensity.

Summary of a new LHC interlock BPM system

- Single-channel scheme with direct digitization
- Bunch-by-bunch measurements
- Single-bunch, single-pass resolution
  - With 25 ns spaced bunches: 9 – 167 µm
  - With 5 ns spaced doublets: (to be measured)
    - Lower resolution expected, but still compatible with the interlock system requirements

Discussion

- Calibration / heartbeat signal
  - Is a centered beam calibration signal sufficient?
  - A calibration signal with beam offsets would require attenuators or/and switches plus extra cabling!
    - …and adds more complexity to the system.
- Prototype electronics test end of 2018
  - Where, how, goals?
- Old -> new electronics transition after LS2
  - How? Old/new systems in parallel? 50-50 split?
- Beam dump procedures (failure modes)
  - Position thresholds, bunch/ turn count windows
  - Fail-safe operation