Measurement of Single Event Upset Cross Section and Study of Noisy Pixels in ATLAS IBL

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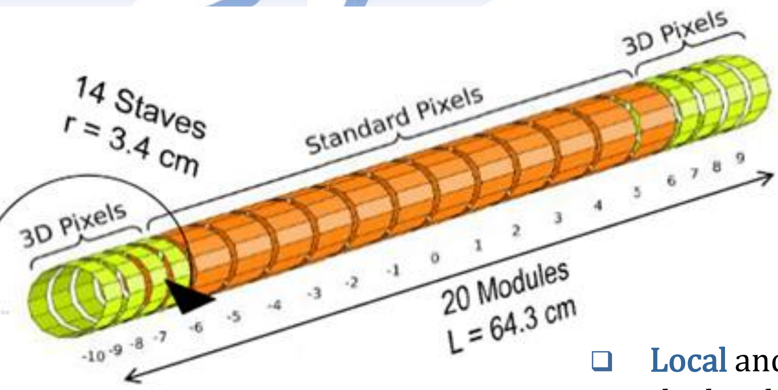
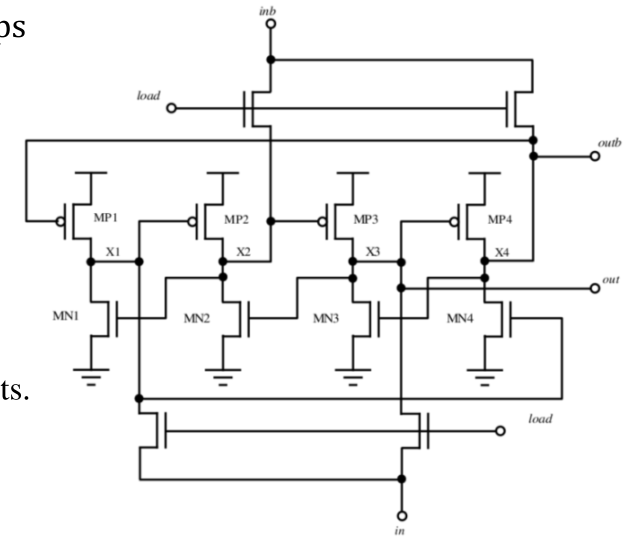
1. Introduction



The Insertable B Layer (IBL)

- The innermost layer of the ATLAS Pixel Detector at the LHC
- 14 staves placed around the beam pipe with a radius of 3.4 cm
- 2 sensor technologies[1]:
  - 12 modules in the central region: **planar sensor** (slim edge n-on-n, 200 μm) bump bonded to double-chip
  - 8 modules on the outside: **3D sensor** (with 2 electrodes per pixel, 230 μm) bump bonded to single-chip
- FE-I4 (2 cm × 1.8 cm) frontend chip in 130 nm CMOS, data rate 160 Mbps
  - 80×336 pixels - pixel size: 250×50 μm^2
- Local and global **memories** are implemented in FE-I4 to retain respectively the local-pixel and global-chip configurations.



Dual Interlocked CEll (**DICE**) latch

Single Event Upset (SEU) : change of state of memory bit caused by ionizing radiation

Efforts to increase SEU tolerance of FE-I4

Redundant storage nodes of DICE latches making SEU less likely (by ~1 order of magnitude from test beam studies)

DICE latch would be upset if 2 nodes storing the same logic state (X1-X3) or (X2-X4) change the state due to single particle impact effects.

Reduction of charge sharing between storage nodes (Smaller device size reduces the space between storage nodes)

Spatial separation of storage nodes

Isolated wells and guard rings, and cell interleaving

Single (Triple) **DICE** latches for memories of each pixel (global chip) configuration

2. SEU cross section

a) SEU cross section $\sigma = \frac{N_{\text{errors}}}{\Phi \cdot N_{\text{latches}}}$

- N_{errors}: the total number of errors obtained for the whole memory
- Φ: the total fluence achieved during the test
- N_{latches}: the number of the latches memories in the chip

Determined by beam testing in 2012: $\sigma = 1.1 \cdot 10^{-15}\text{cm}^2$, by disabling the enable bit of each pixel before the test beam [2]

b) Quiet-pixels-fraction

Quiet pixels : never fired in 20 pb^{-1} data (prob = 1.1× 10^{-20} for normal pixels)

* *Average occupancy of one pixel~46 in one of the most forward 3D module in 20 pb^{-1} data .*

* *Only clusters with length one along beam direction are used because the hit position is not stored for other cluster sizes.*

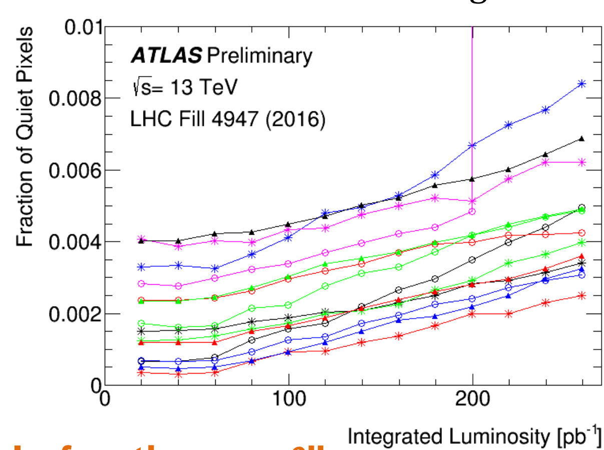
Caused by SEU effects with flipping the pixel enable bit from 1 to 0

Similar behavior of the 14 3D modules in the most forward IBL ring

- **More pixels go to quiet** along the data taking due to the **accumulation of ionizing radiation.**

Quiet-pixels-fraction = $p_0 + p_1 \cdot \mathcal{L}$

- p_0: Dead pixels in some modules
- p_1: $1\sim2 \cdot 10^{-5}$



c) Extraction of σ from "quiet-pixels-fraction vs $\mathcal{L}$"

Quiet-pixels-fraction is actually equal to $\frac{N_{\text{errors}}}{N_{\text{latches}}}$.

➔ $\sigma = \frac{p_1 \cdot \mathcal{L}}{\Phi}$ (Ideally $p_0 = 0$)

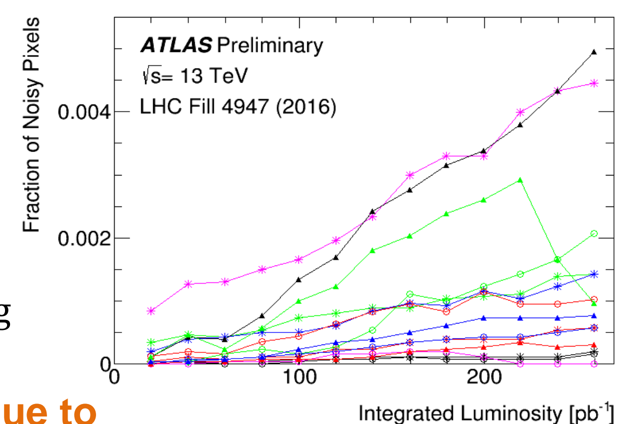
- 1 pb^{-1} data corresponds to a fluence of $\frac{5}{3} \cdot 10^{10} n_{eq}\text{cm}^{-2}$.
- **The SEU cross section is calculated to be $0.6\sim1.2 \cdot 10^{-15}\text{cm}^2$**
- This is at the same order of magnitude as the testbeam result.

3. Noisy pixels by SEU

a) Noisy-pixels fraction

Noisy pixel: fired >300 times in 20pb^{-1} data (prob.= 2.3 × 10^{-136} for normal pixels)

Different behavior of the 14 3D modules in the most forward IBL ring



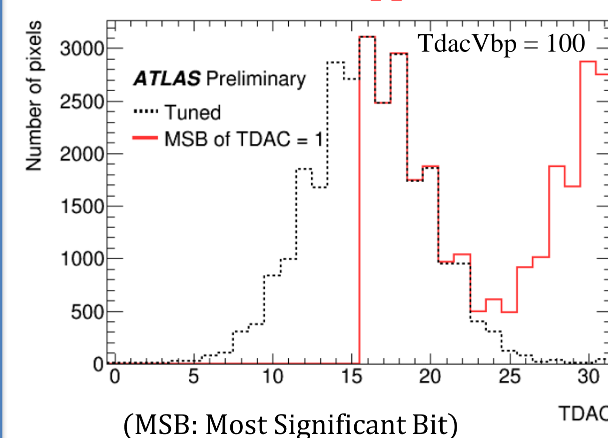
b) Production of noisy pixels is due to the threshold decrease caused by the bit flip of TDAC

- **Threshold in each pixel** is determined by
  f (VthinAlt_Coarse) + f (VthinAlt_Fine) + f(TDAC*TdacVbp)

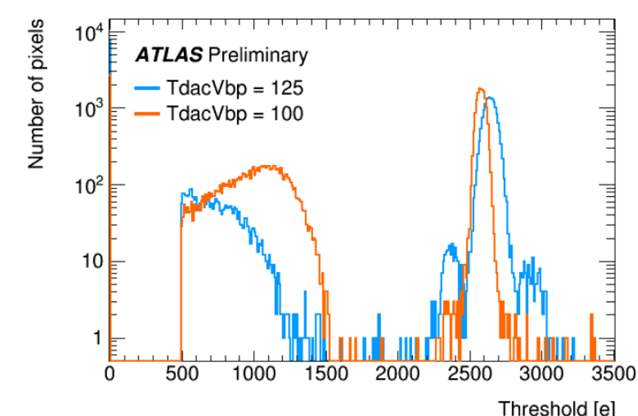
f (VthinAlt_Coarse) + f (VthinAlt_Fine)	TDAC	TdacVbp
two 8-bit global register for adjustment of global threshold	in-pixel threshold tuning 5-bit DAC	8-bit global register sets the step size of TDAC

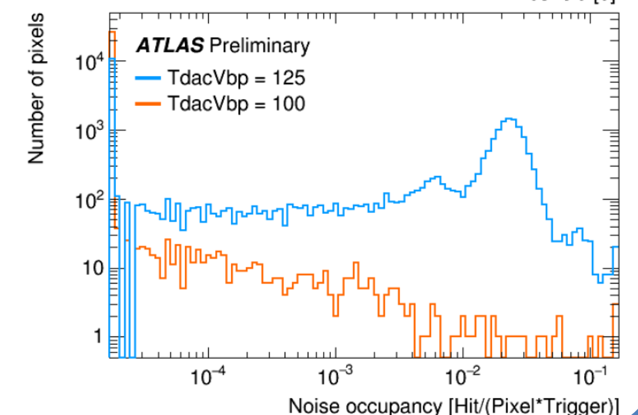
- Global registers are not easily flipped due to triple redundancy latches.

MSB of TDAC is flipped from 0 to 1 ➔ Lower threshold



(MSB: Most Significant Bit)





- The truncation at 500e is due to the lower limit of charge injection.
- The bias voltage of TdacVbp can be changed.
- **Smaller TdacVbp makes the pixels more robust against noise.**
  - **but some pixels cannot be tuned.**

4. Summary

- **The SEU effects flipping the enable bits of some pixels make them quiet.**
  The SEU cross section (flipping the enable bit of one pixel from 1→0) obtained by the study of "quiet-pixels-fraction vs $\mathcal{L}$" is at the same order of magnitude with the result of beam testing (0→1).
- **The lower threshold caused by the bit flip of TDAC makes pixels noisy.**

To recover the bits flipped by SEU → Automatic reconfiguration to each pixel will be carried out.

[1] ATLAS IBL Collaboration, ATLAS Insertable B-Layer Technical Design Report. CERN-LHCC-2010-0013.
[2] M. Menouni et al., SEU tolerant memory design for the ATLAS pixel readout chip, 2013 JINST 8 C02026.

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