The LHCb VELO Upgrade

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on behalf of the LHCb VELO group

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Overview

LHCb\textsuperscript{1} / Current VELO\textsuperscript{2} / VELO Upgrade

\textsuperscript{1} More details at J. Instrum. 3 (2008) S08005
\textsuperscript{2} More details at J. Instrum. 9 (2014) P09007

Operated 2011 - 2018
**LHCb / VELO**

**LHCb** is a single-arm forward spectrometer dedicated to the study of b- and c-physics.

**VErtex LOcator** is a silicon detector surrounding the collision region, providing excellent
- impact parameter resolution
- identification of secondary vertices
The current VELO microstrip detector

- 2 retractable detector halves at 5 (30) mm from beam when closed (open).
- 21 stations per half with an R and $\phi$ sensor.
- First active strip @ 8 mm from the beam.
- Operates in secondary vacuum.
- 300 $\mu$m Al foil separates detector from beam vacuum.
- CO$_2$ cooling system (operates @ -30°C, sensors @ -10°C).
LHCb Upgrade motivation

Precision of many physics measurements at LHCb will be statistically limited at end of Run II:

- Increase luminosity to boost statistics:
  \[ 4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1} \rightarrow 2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1} \]
  - 50 fb\(^{-1}\) expected after LS2

- Remove hardware trigger
  - 1 MHz \rightarrow 40 MHz readout rate
  - Data taking starting in 2021 (Run III)

many hadronic channels saturate, due to energy cuts in the trigger
VELO Upgrade

- To be operated @ **40 MHz** and **$2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$** and at **3.5 mm** from the beams
  - 2.8 Tb/s data rates
  - $8 \times 10^{15}$ 1 MeV $n_{eq} \text{ cm}^{-2}$ max fluence
  - Sensors to be kept < -20°C

- Improve detector performance
  - Track reconstruction
  - Resolution

- The plan:
  - **New pixel detector**
    - No ghost tracks
    - Faster reco algorithm
  - **New front-end electronics**
  - **Thinner RF-foil**
  - More efficient cooling interface
### VELO Upgrade in numbers

<table>
<thead>
<tr>
<th>Feature</th>
<th>VELO</th>
<th>Upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sensors</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R &amp; φ strips</td>
<td>0.22 m²</td>
<td></td>
</tr>
<tr>
<td>172,032 strips</td>
<td></td>
<td></td>
</tr>
<tr>
<td>electron collecting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>300 μm thick</td>
<td></td>
<td></td>
</tr>
<tr>
<td>40-100 μm pitch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41 M pixels</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pixels</td>
<td>0.12 m²</td>
<td></td>
</tr>
<tr>
<td>electron collecting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>200 μm thick</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55 μm pitch</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong># of modules</strong></td>
<td>42</td>
<td>52</td>
</tr>
<tr>
<td><strong>Max fluence</strong></td>
<td>$4.3 \times 10^{14}$ MeV n_{eq} cm^{-2}</td>
<td>$8 \times 10^{15}$ 1 MeV n_{eq} cm^{-2}</td>
</tr>
<tr>
<td><strong>HV tolerance</strong></td>
<td>500 V</td>
<td>1000 V</td>
</tr>
<tr>
<td><strong>ASIC readout rate</strong></td>
<td>1 MHz</td>
<td>40 MHz</td>
</tr>
<tr>
<td><strong>Total data rate</strong></td>
<td>analog (eq. to 150 Gb/s)</td>
<td>2.8 Tb/s</td>
</tr>
<tr>
<td><strong>Total Power consumption</strong></td>
<td>1 kW</td>
<td>1.6 kW (30 W/module)</td>
</tr>
</tbody>
</table>
Micro-channel cooling interface

- 500 µm thick silicon substrate with integrated micro channels.
- Same CTE as sensors + low material budget
- High thermal efficiency
- Routing of channels customisable
  - 120 × 200 µm micro-channels (19×)
  - 60 × 60 µm high impedance restrictions
  - Cooling power ~50 W
- Pressure: 14 bar @ -30 °C, 60 bar @ 22 °C

8” wafers containing 2 cooling interfaces, 4 soldering samples and several high pressure test samples.
Micro-channel cooling interface

1. connector pre-tinning
2. silicon pre-tinning
3. alignment
4. soldering

- high quality soldering is essential
  - leak tightness
  - planarity
  - minimum voids in the solder layer
  - no flux
  - high pressure qualification: 186 bar

- metallization with Ti+Ni+Au

For more details see this talk.
Aluminium foil

- accommodate modules (~1 m long)
- separate primary/secondary vacua
- shield against RF pick-up from the LHC beams
- light (300 μm → 250 μm)
- withstand ΔP = 10 mbar
- corrugated
- thermally stable
- vacuum tight
- rad-hard

Al mould 1 mm smaller than box
Mill inside of box
Mill outside of box
Half box prototype
ASIC derived from TimePix3 (VeloPix)
- 130 nm CMOS technology (TSMC)
- 256 x 256 pixels, 55 x 55 μm pixel size

Sensor is bump-bonded to 3 VeloPix ASICs
- Hamamatsu n-on-p 200 μm thickness
- Elongated pixels (137.5 μm) in the region between ASICs
- 450 μm wide guard ring
- DRIE-etched round corners (foil clearance)

Triggerless, binary readout (data-driven readout)
- Up to 800 Mhits/s/ASIC
- Highly non-uniform irradiation

For more info, see here.
Sensors qualification

- Sensors irradiated \((2-8 \times 10^{15} \text{ MeV } n_{eq} \text{ cm}^{-2})\) in 5 different facilities with neutrons (uniform) and protons (non-uniform).
- Rigorous series of testbeams to qualify the sensors, using TimePix3 telescope at SPS.
- Velo Sensors must collect at least 6000 e-/MIP @ 99% efficiency.

- Results after full fluence irradiation.
- Collected charge reaches 6000 e- target with bias voltage < 1000V.

- Results after full fluence irradiation.
- Efficiencies reach 99% at 1000V, also in the corners.
- Production choice: 39 \(\mu\)m implants.
First VELO module prototype

June 2018
The new VELO will have to cope with higher radiation and data rates.
- New module design based on pixels sensors mounted on a Si micro-channel substrate.
- Aluminium RF-foil prototypes progressing well.
- Sensor tiles irradiated and extensively characterised in test-beams.
- First Module prototypes in June 2018.

VELO fully mounted expected in September 2019.
- Install during LHC Long Shutdown 2 and take data in Run III
Backup slides
LHCb detector
**Alignment**

- VELO halves centred around beam at each fill, when beams declared stable.
  - Beam position determined from vertex reconstruction with tracks in right or left half.
  - Misalignment from distance between the two reconstructed vertices.
  - Fully automated procedure (~210 s).
  - Stable within ±5 μm (x).

![Graph showing variation in alignment number for LHCb VELO](graph.png)

- Empty markers = no update
- 17/04/2018 - 29/05/2018
Micro-channel cooling technology

Deep Reactive Ion Etching

Hydrophilic bonding

Silicon oxides

Au - 500 [nm]

Ni - 350 [nm]

Ti - 200 [nm]

DRIE etching of channels

Si cover bonding

Thinning

Plasma etching of fluidic inlets

Metallization for soldering connectors

500 μm

240 μm

120 μm

140 μm
None of the LHCb samples with nominal channel width broke. Max testing pressure: 450 bar.
Intra-pixel efficiency on neutron-irradiated sensors:
- Decreases in the corners at low bias.
- Scales with implant width.
- For normal incidence tracks.
- Efficiency reaches 99% at 1000 V.

Conditions:
- bias voltage: 300 V
- irradiation: $8 \times 10^{15}$ 1 MeV $n_{eq}$ cm$^{-2}$
- sensor thickness: 200 μm
VeloPix & DAQ

- Derived from Timepix3 ASIC.
- Based on 130 nm CMOS technology (TSMC).
- Data-driven readout.
- 2×4 pixels grouped to SuperPixel.
- Timepix3 is general purpose.
- VeloPix is optimized for speed: VELO will produce 3 Tbit/s.
- Radiation hardness and SEU robustness.
- Binary hit information.

- Data gathered in SuperPixels:
  - shared BCID and address
  - 30% data reduction
- SP data propagated downwards:
  - arbiter decides who can send.
  - time continuity lost.

- Back end electronics must cope with a huge amount of data:
  - TELL40 (upgrade of TELL1, current DAQ board) receives and builds events using FPGAs.
  - All the information is assembled and passed on to computing farm, stripping down redundant data.
  - Further processing and full reconstruction in the trigger farm.
Full 3D design

Beam vacuum

Isolation vacuum

Vacuum feedthrough board

Modules