环形正负电子对撞机
Circular Electron Positron Collider

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Development of the Silicon Tracker for CEPC

Yunpeng Lu

On behalf of the study group

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COEX, SEOUL

XXXIX INTERNATIONAL CONFERENCE ON HIGH ENERGY PHYSICS

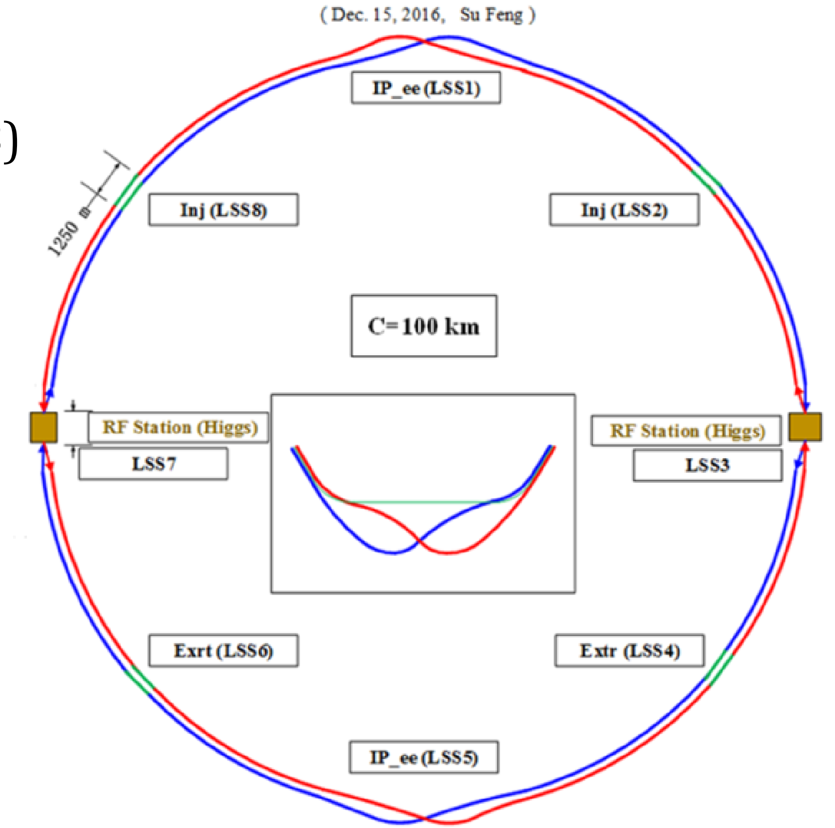
Outline:

- *Baseline design*
- *Pixel sensor specifications*
- *R&D activities*
- *Future plan*
- *Summary*

CEPC and Its Beam Timing

- Circular Electron-Positron Collider (90, 160, 250 GeV)
  - Higgs factory (10^6 Higgs)
  - Z & W factory (10^{10} Z^0)
- Baseline design in CDR(to be released in 2018)
- Bunch spacing 680 ns (25 ns @ Z-pole)
  - Continuous colliding mode
  - Power pulsing not applicable
  - New constraint for the detector development:

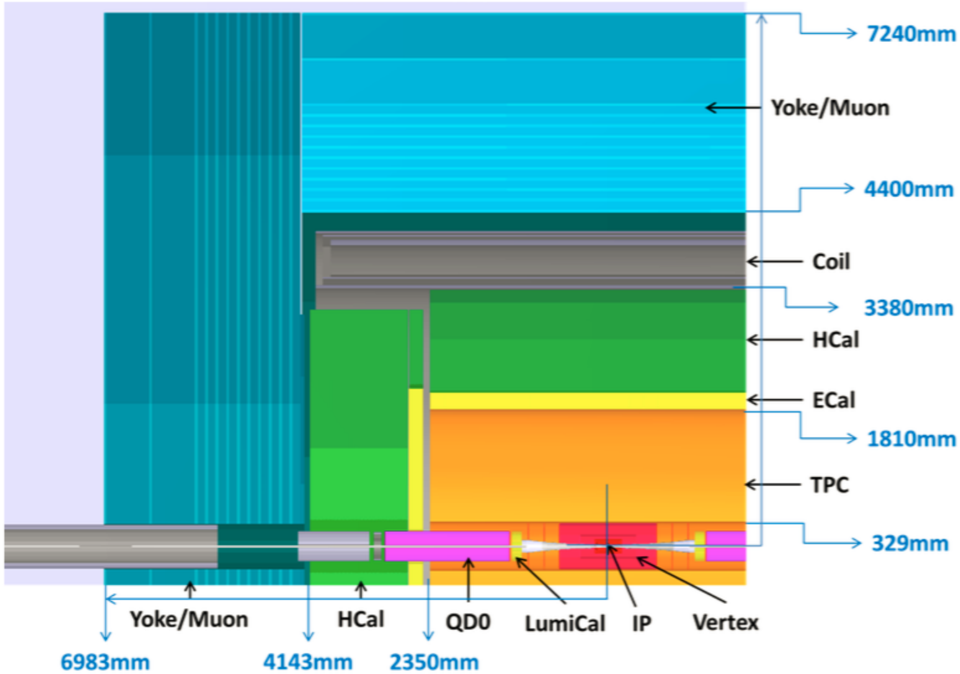
  Very low power consumption

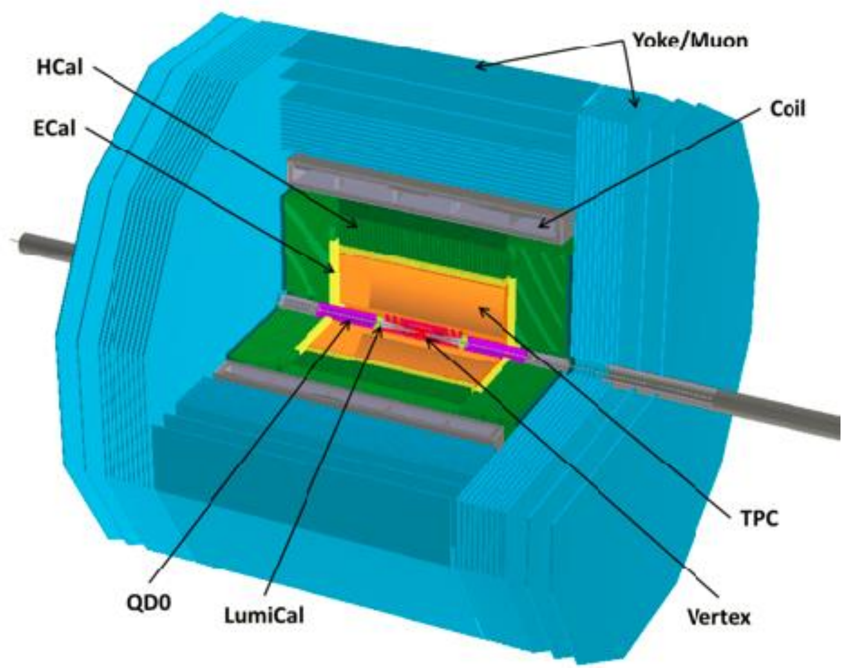


Fully Partial Double Ring - 100Km*

*** CEPC Accelerator CDR and R&D towards TDR, J. Gao, Accelerator session on Sat. morning**

Detector Concept





Particle Flow Oriented Detector for CEPC*

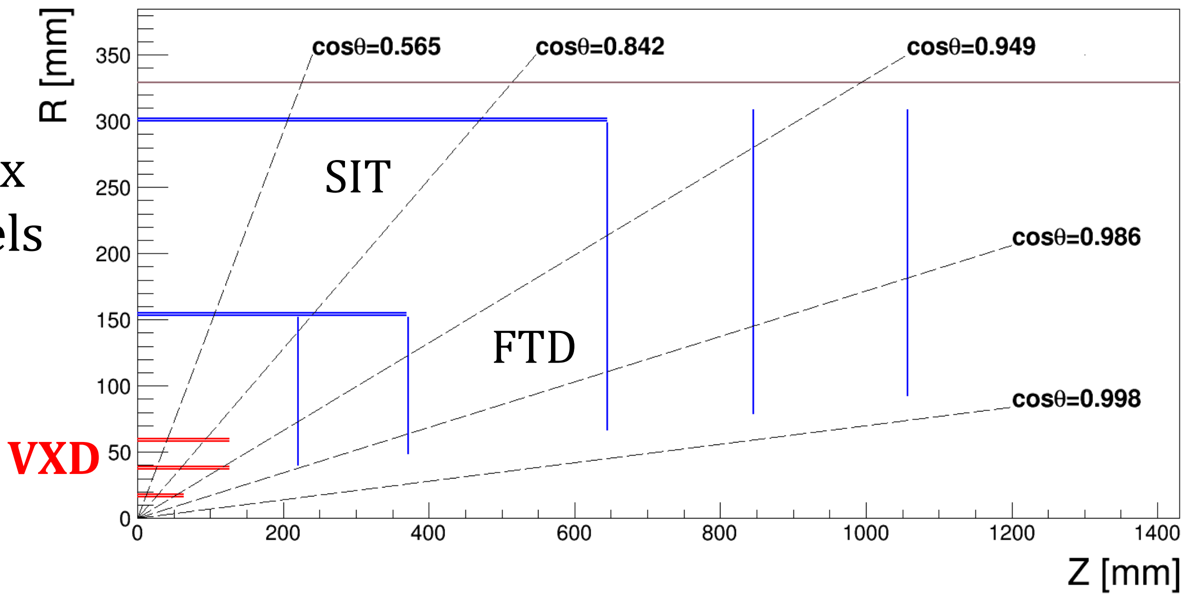
- Two detector concepts
- One is ILD-like, which is optimized for
  - 3 Tesla magnet
  - L* = 2.2 m

*** Physics performance of the Particle Flow Oriented detector at the CEPC, Manqi Ruan, Poster**

Baseline Silicon Tracker Layout

VXD:

- Same layout as the ILD vertex
- 3 layers of double-sided pixels
- σ_{SP}=2.8μm, inner most layer
- Polar angle θ~15 degrees



- Silicon Internal Tracker (**SIT**) – 2 inner layers Si strip detectors
- Forward Tracking Detector (**FTD**) – **5 disks** (2 with pixels and 3 with Si strip sensor) on each side, comparing 7 disks on ILD, due to **smaller L***
- Silicon External Tracker (**SET**) – 1 outer layer Si strip detector
- End-cap Tracking Detector (**ETD**) – 1 end-cap Si strip detector on each side

Silicon Tracker Requirements

B=3T

- momentum resolution
- impact parameter resolution

Efficient tagging of heavy quarks

$$\sigma_{1/p_T} = 2\times10^{-5} \oplus 1\times10^{-3}/(p_T \sin\theta)$$

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex specifications:

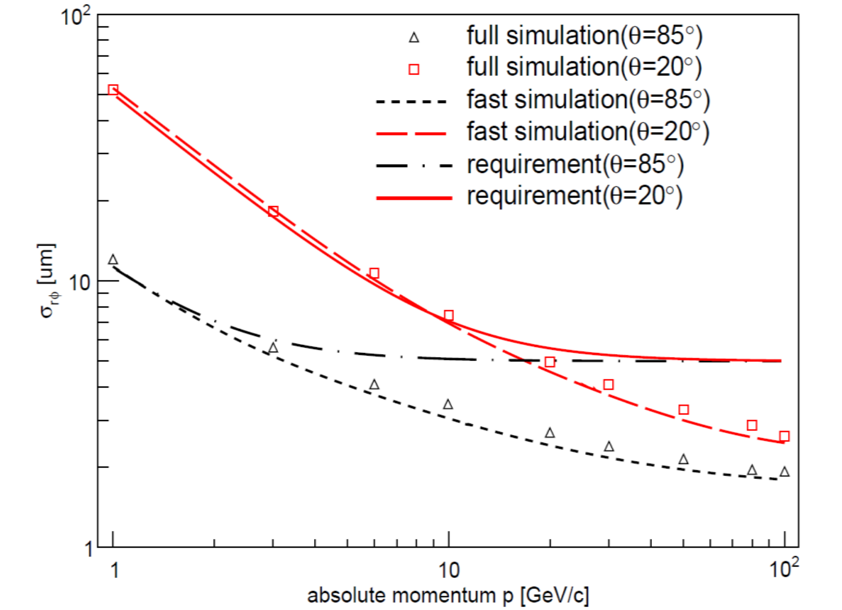
- σ_{SP} near the IP: *≤3 μm*
- material budget: *≤ 0.15%X_0/layer*
- pixel occupancy: *≤ 1 %*
- radiation tolerance: Ionising dose *≤1 Mrad/ year*
  Non-ionising fluences *≤10^{12} n_{eq}/ (cm^2 year)*
- first layer located at a radius: *~1.6 cm*

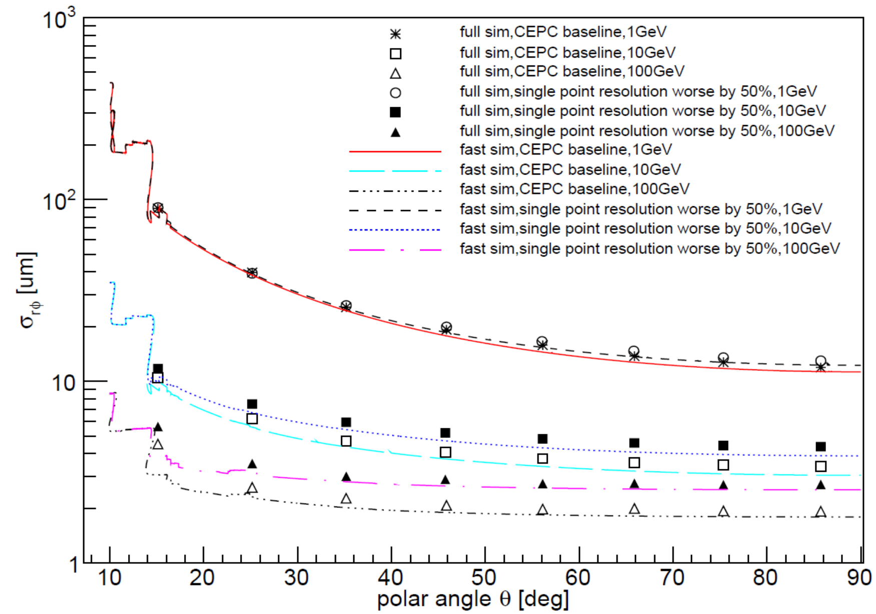
Tracking specifications:

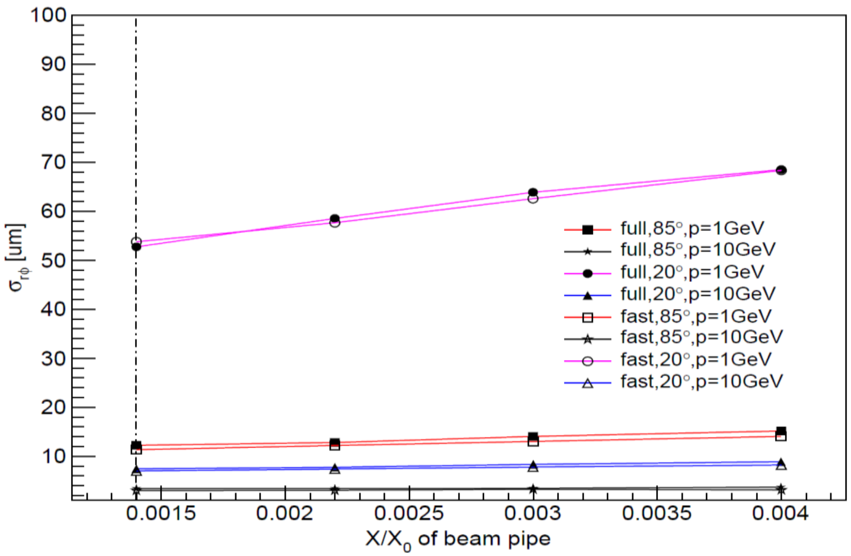
- σ_{SP} : *≤ 7 μm* → small pitch (50 μm)
- material budget: *≤ 0.65%X_0/layer*

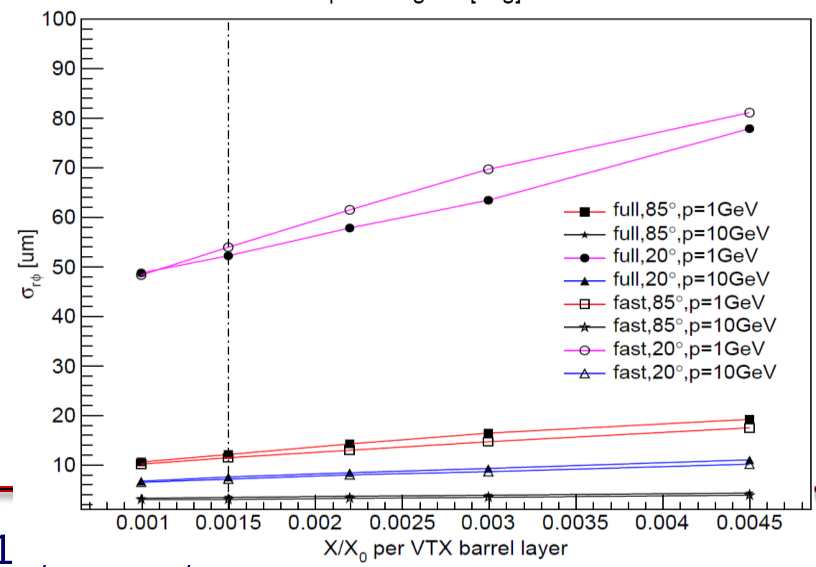
Performance Studies – IP Resolution

Z.Wu, C.Fu, et al (IHEP), CDR draft









Pixel Sensor Specifications

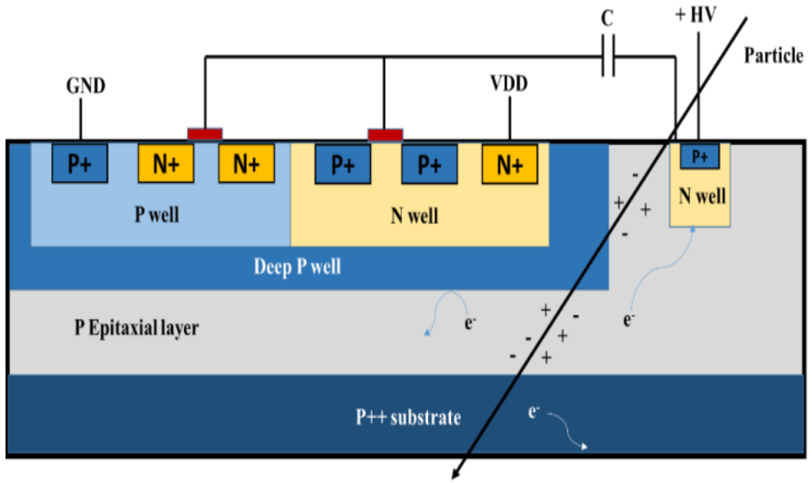
- **Current R&D focused on the pixel sensor for the Vertex**
- To achieve S.P. resolution
  - Digital pixel with in-pixel discriminator ~ 16um
  - Analog pixel ~ 20um (heavily rely on power pulsing as in the ILC)
- To lower the material budget
  - Sensor thickness ~ 50um
  - Heat load < 50 mW/cm^2 constrained by air cooling
- To tackle beam-related background
  - 20us/frame?
  - 1Mrad/year & 2$\times$10^{12}neq/ (cm^2·year)?

Physics driven requirements	**Running constraints**	**Sensor specifications**
$\sigma_{s.p.}$ 2.8um ---->		Small pixel 16um
Material budget 0.15% X_0/layer ---->		Thinning 50um
(Material budget) ---->	Air cooling ---->	low power 50mW/cm^2
r of Inner most layer 16mm ---->	beam-related background ---->	fast readout 20us?
(r of Inner most layer) ---->	radiation damage ---->	radiation tolerance *≤1 Mrad/ year ?* *≤2×10^{12}n$_{eq}$/ (cm^2 year) ?*

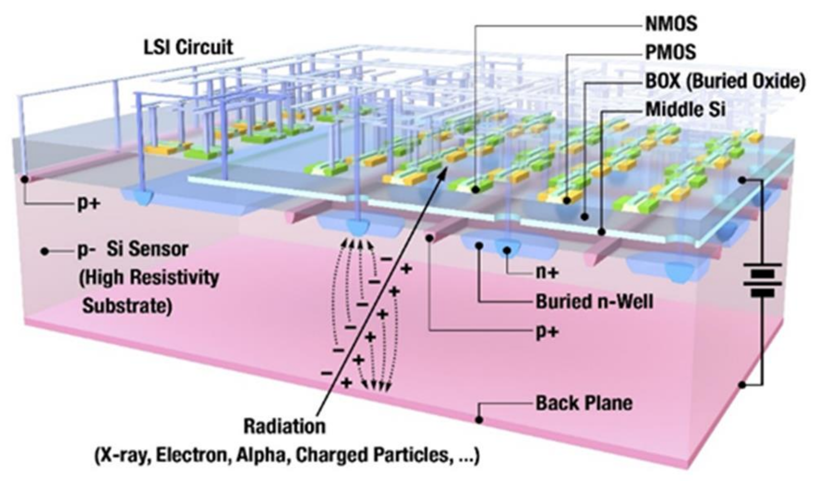
R&D Activities

- Two monolithic pixel technologies

- CMOS pixel sensor (CPS)
  - *TowerJazz CIS 0.18 μm process*
  - *Quadruple well process*
  - *Thick (~20 μm) epitaxial layer*
  - *with high resistivity (≥1 kΩ•cm)*



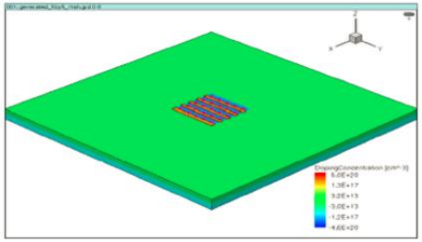
- SOI pixel sensor
  - *LAPIS 0.2 μm process*
  - High resistive substrate (≥1 kΩ•cm)
  - Double SOI layers available
  - Thinning and backside process



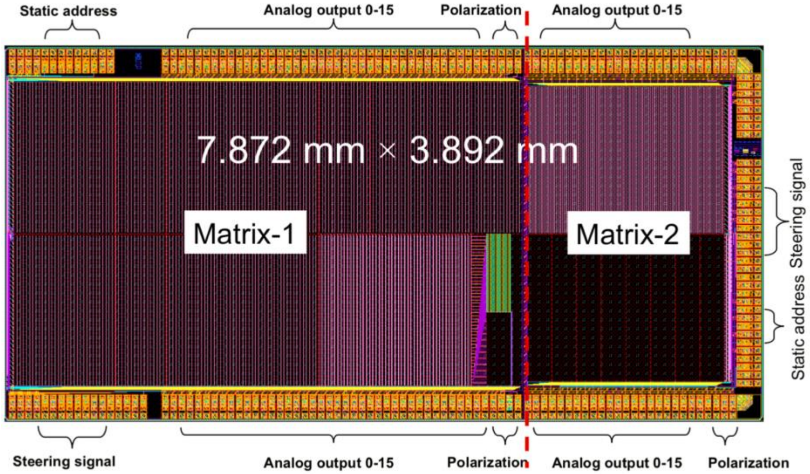
R&D Activities - CMOS Pixel Sensor

Y.Zhang, et al, NIMA 831(2016)99-104

- **Sensor design & TCAD simulation**
  - Different sensor diode geometries, epitaxial-layer properties and radiation damage



- **JadePix1, first submission in Nov. 2015**
  - Exploratory prototype, analog pixel, rolling shutter readout mode
  - Sensor optimization and radiation tolerance study
  - sensing node AC-coupled to increase biased voltage



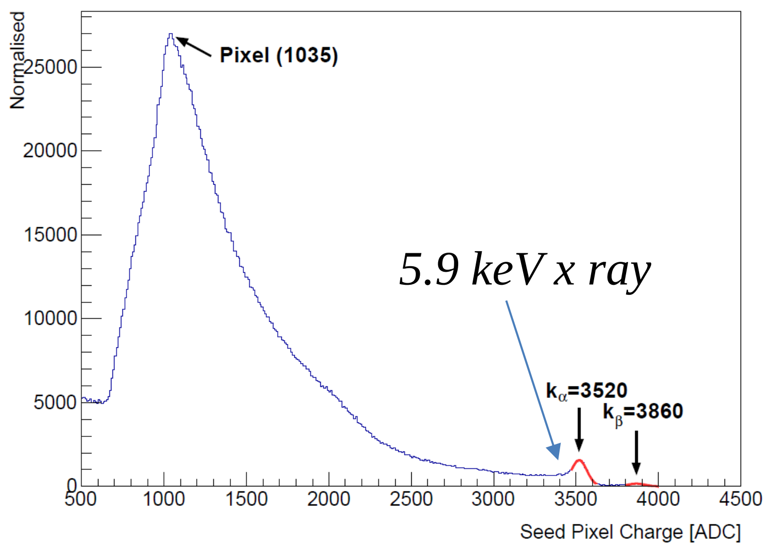
- **Sensor characterization ongoing**
  - Noise level
  - Gain calibration with ^{55}Fe
  - Charge collection efficiency with ^{90}Sr
  - Irradiation with Neutron
  - Test beam in Aug. 2018

X. Shi, CEPC Workshop Rome May 24-26 2018

^{55}Fe Source Calibration

Test results from ***JadePix1****: diode + SF structure*

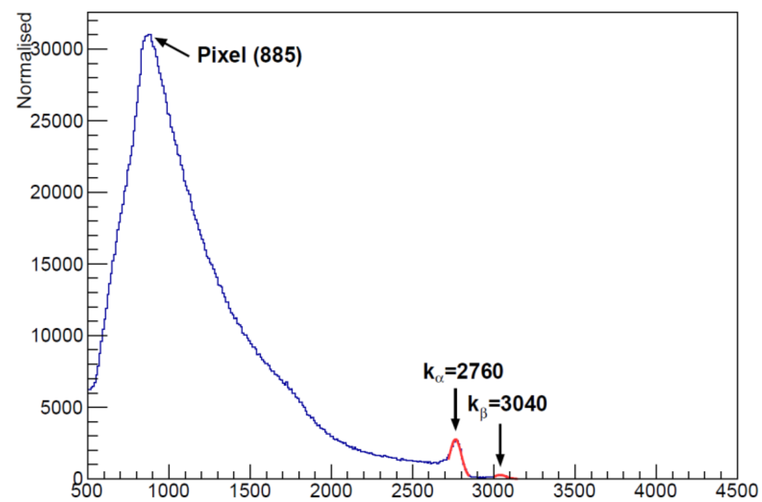
4 um^2 diode, V_{diode} ~1 V



$CVF \approx 32\ \mu V/e^-$

Equivalent $C_{in} \approx 5\ fF$

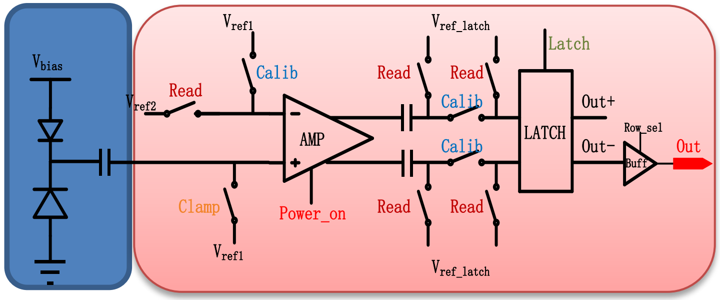
8 um^2 diode, V_{diode} ~1 V



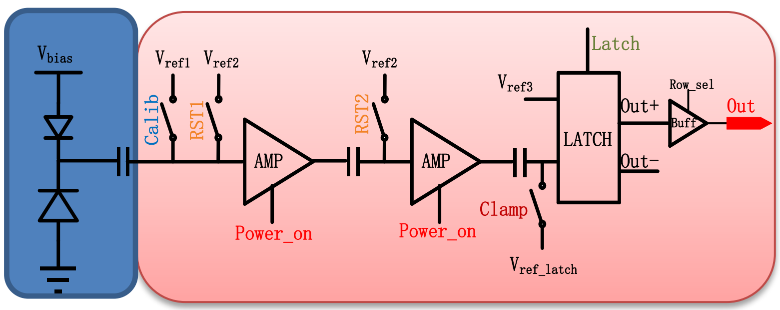
$CVF \approx 26\ \mu V/e^-$

Equivalent $C_{in} \approx 6.15\ fF$

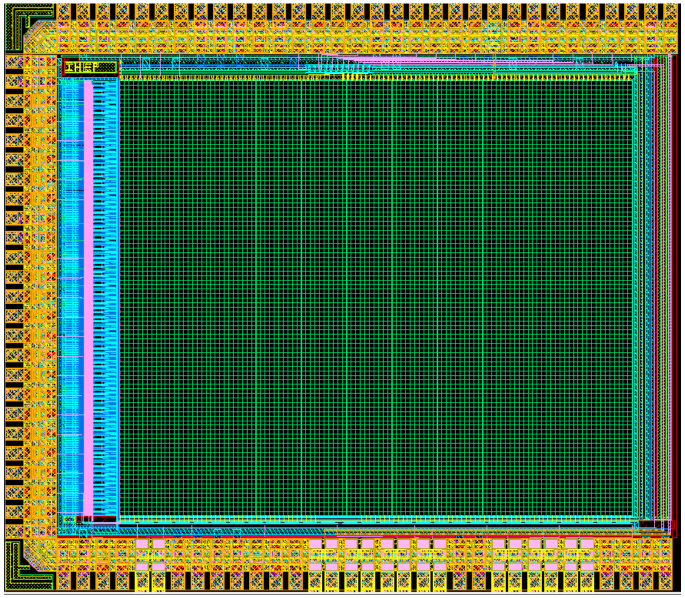
JadePix2 design: Rolling-shutter Mode



Version 1: differential amplifier + latch



Version 2: two stage CS amplifiers + latch



JadePix2 Layout

Submitted in 2017.

Two different pixel versions:

- Amplifier + Discriminator
- Pixel size: 22μm×22μm
- Positively biased sensing diode;
- Offset cancellation technique;

Chip features:

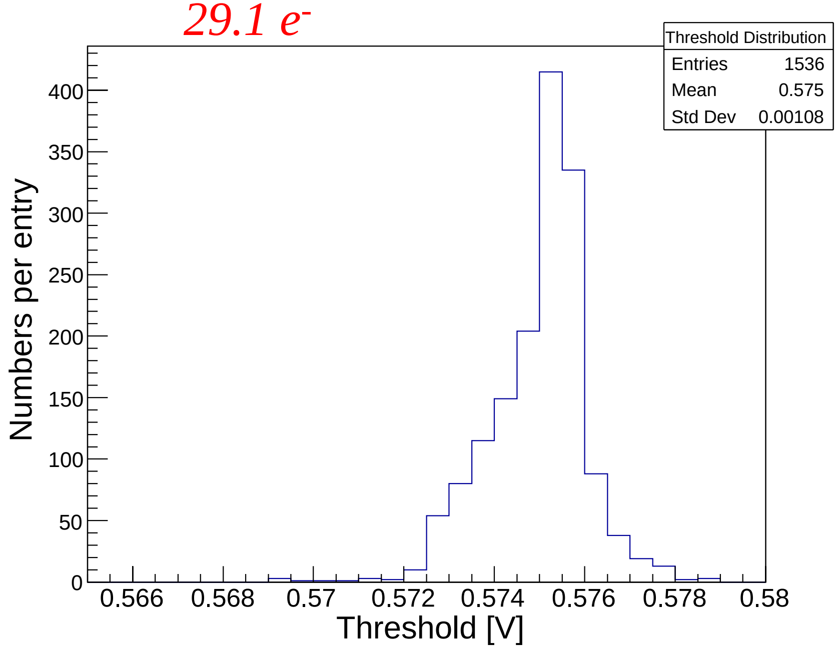
- 3×3.3 mm^2
- 96×112 pixels with 8 sub-matrix
- Processing speed: 11.2μs/frame with 100 ns/row
- Output data speed: 160 MHz
- Power: 3.7μA/pixel (14.4 mW/cm^2 @pixel matrix)

Y. ZHOU, HSTD11, OKINAWA Dec. 10-15 2017

Noise Measurement of JadePix2

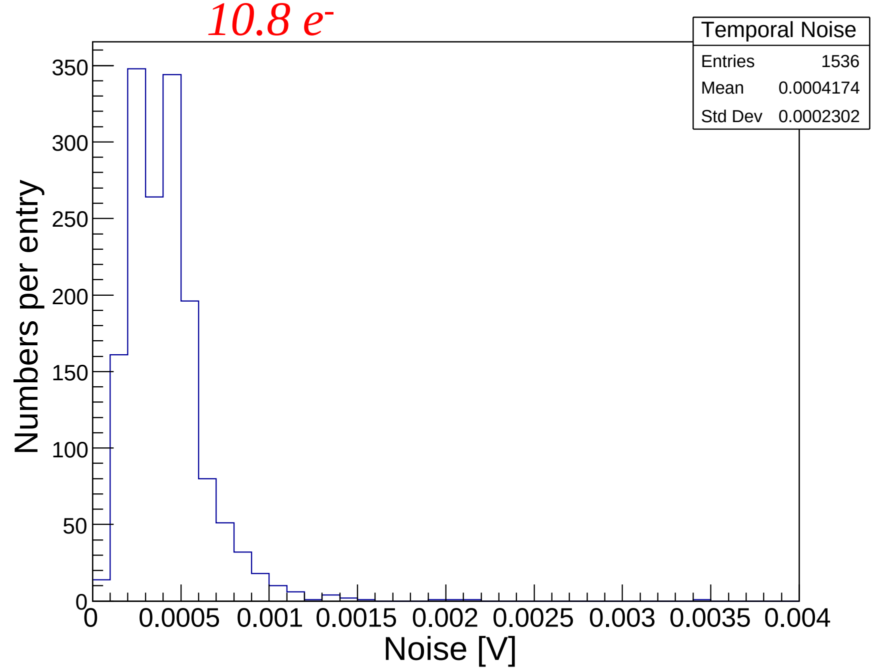
FPN: 1.08mV @input node

29.1 e^-



TN: 0.4mV @input node

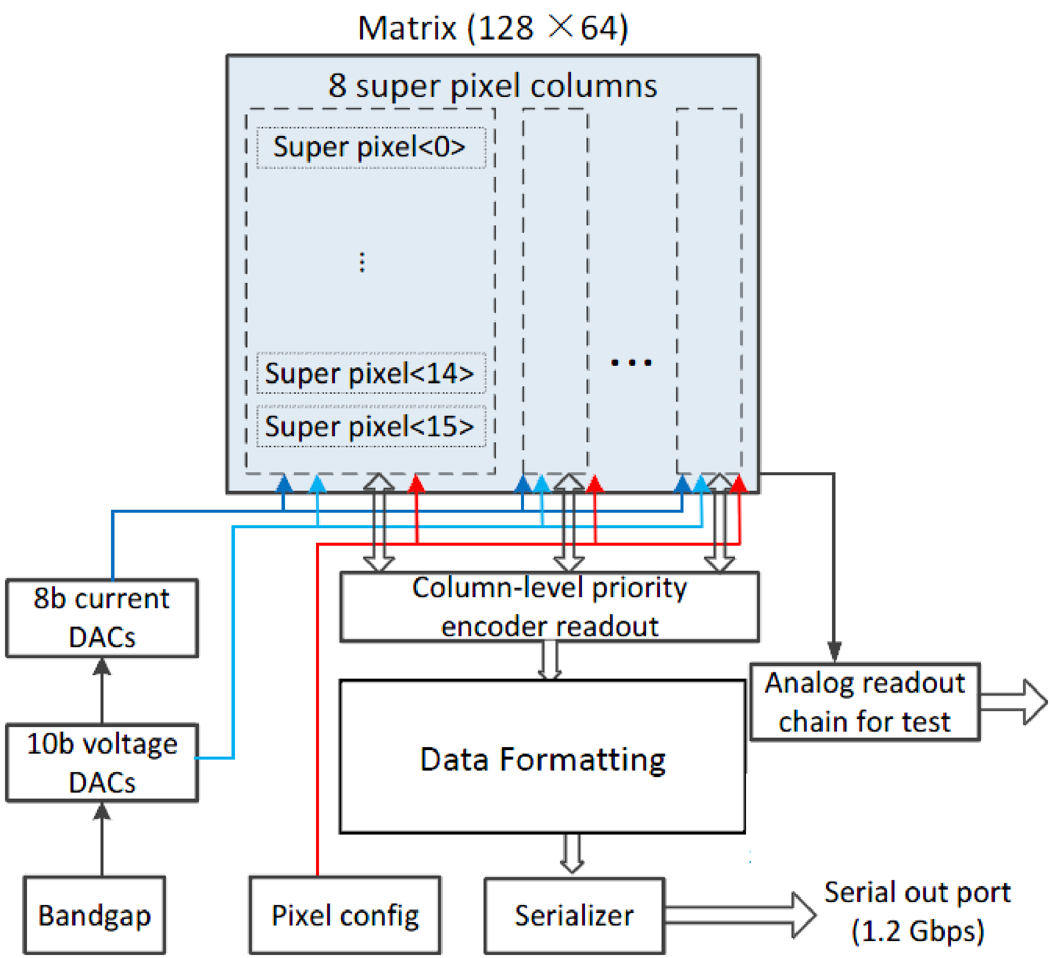
10.8 e^-



Total noise $= \sqrt{29.1^2 + 10.8^2} =$ *31 e^-*

Converted by simulation results, not calibrated yet

MIC4 Design: Asynchronous Mode

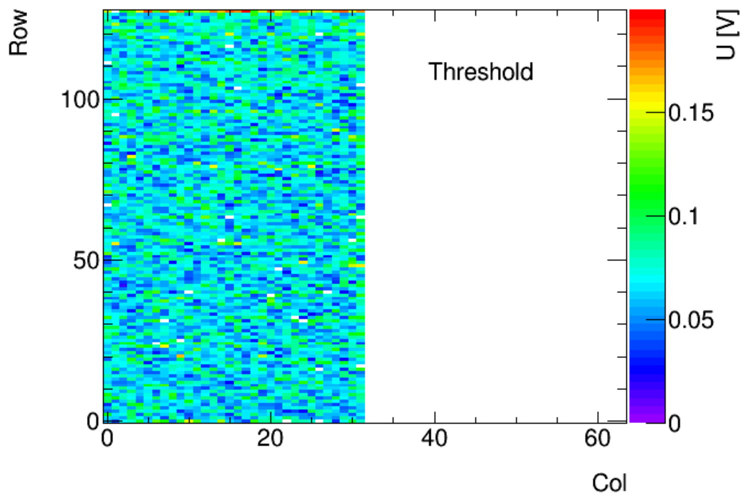


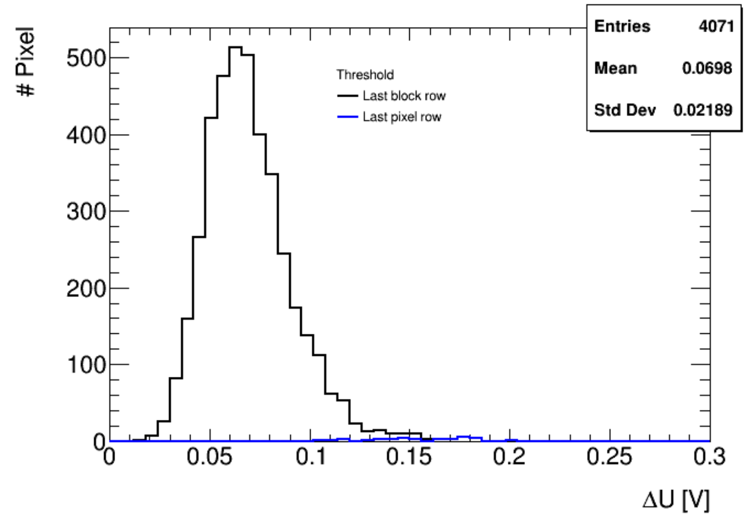
MIC4 over all block diagram

- Based on the ALPIDE design
  - Super pixel introduced
- Submitted in 2017
- TowerJazz180 nm CIS process
- Pixel size: 25 um x 25 um
- Matrix: 128 rows x 64 columns
- Zero suppression readout

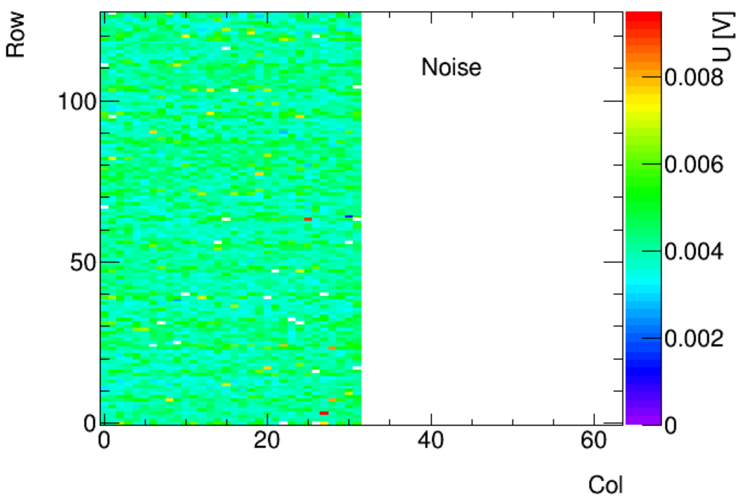
P. YANG, CEPC Workshop WUHAN Apr. 19-21 2017

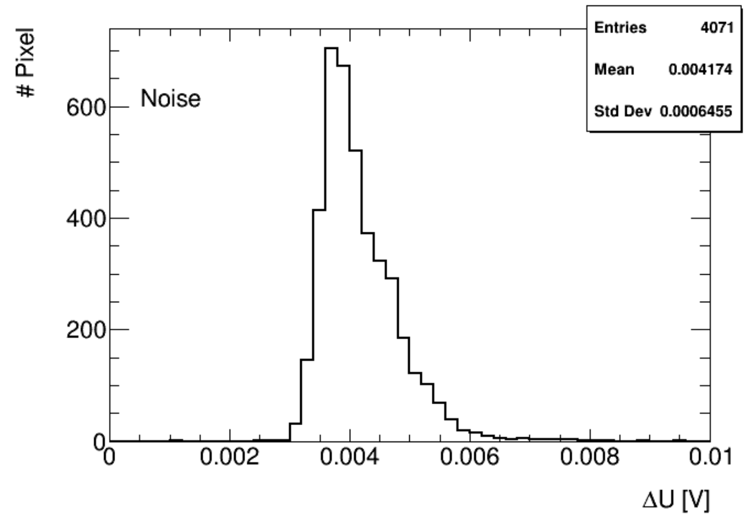
Threshold and Noise distribution in MIC4





- Mean threshold around 99 e^-

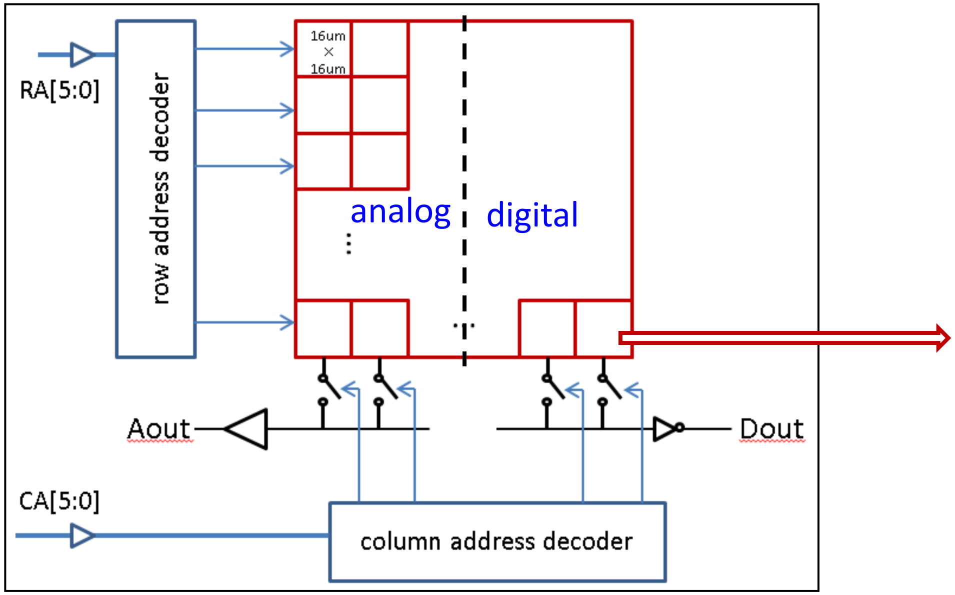




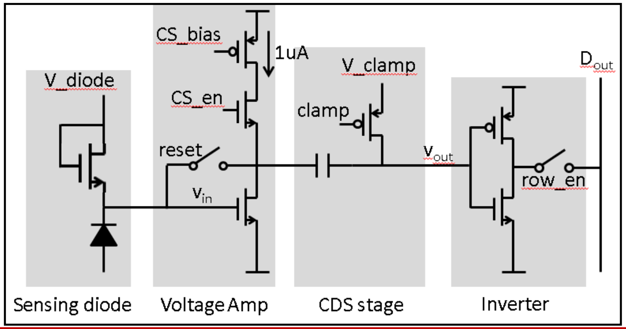
- Mean FPN ~ 31 e-, TN around 6 e-

R&D Activities - SOI Pixel Sensor

- **First submission (CPV1) in June 2015**
  - 16*16 μm with in-pixel-discriminator
  - Double-SOI process for shielding and radiation enhancement
- **Second submission (CPV2) in June 2016**
  - In-pixel CDS stage inserted
  - To improve RTC and FPN noise
  - Thinned down to 75 μm



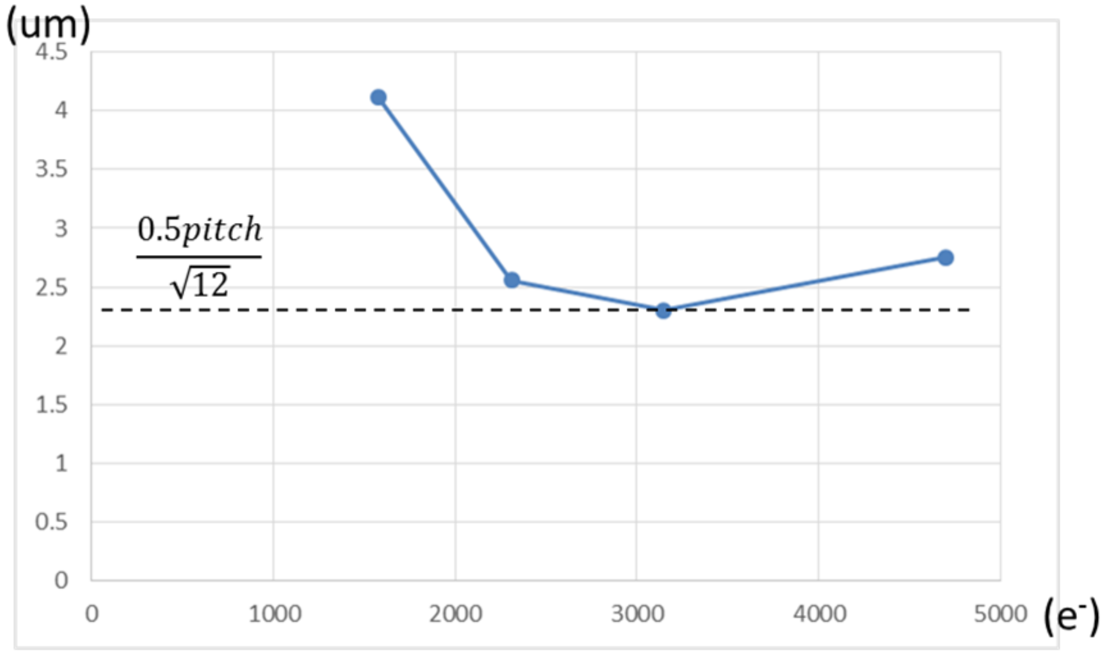
- Sensing diode, 2um
- HV protection, diode-connected NMOS
- Voltage amplifier, DC Gain ~ 10
- Reset & Clamp
- Inverter as discriminator
- Layout, 16 um pitch



Yunpeng Lu, et al, A prototype SOI pixel sensor for CEPC vertex, FEE2018, May 2018

Spatial Resolution

- 1064nm laser beam
  - Focused beam waist ~ 3.4 um
  - Intensity adjustable
- Spatial resolution versus signal charge
  - Obtained the best resolution of 2.3um at around 3000e$^-$ signal charge
  - Consistent with the simulation



S.P. resolutin as a function of signal charge

Future Plan on R&D

- Laboratory and test-beam characterizations
- Coordination of sensor design team for next submission
- Novel readout scheme
- Large area pixel array design
- Radiation hardness
- Time stamp @ Z-pole?
- Small (16μm × 16μm) pixel, targeting on 3μm single point resolution
  - To explore SOI 3D connection technology by designing the in-pixel digital logic in a separated tier
  - Or to look for any new process

Summary and Outlook

- R&D focused on the inner layer of the Vertex
- CPS & SOI prototype design submitted
  - *in-pixel electronics, small pixel size*
  - *new asynchronous readout architecture*
- Preliminary test results is encouraging
  - 2.3um resolution achieved on 16 um small pitch with in-pixel discriminator
- Engineering run submission is planned in 2019-2020

Acknowledgements

This work is partially supported by

- The National Nature Science Foundation of China, Grant 11575220 & 11505207 & 11605071 & 11605217, and
- The National Key Program for S&T Research and Development, Grant 2016YFA0400400

Thank you for your attention!

CEPC CDR Parameters

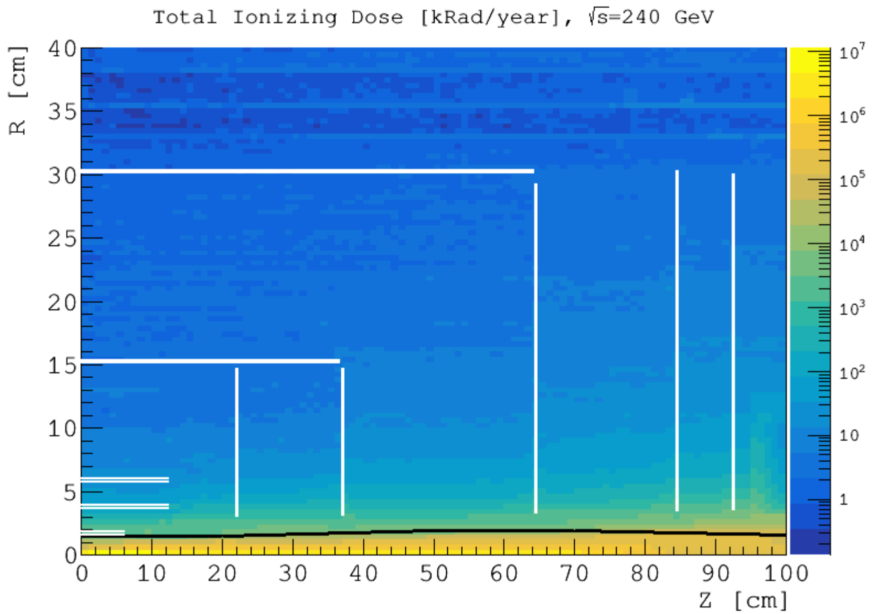
D. Wang

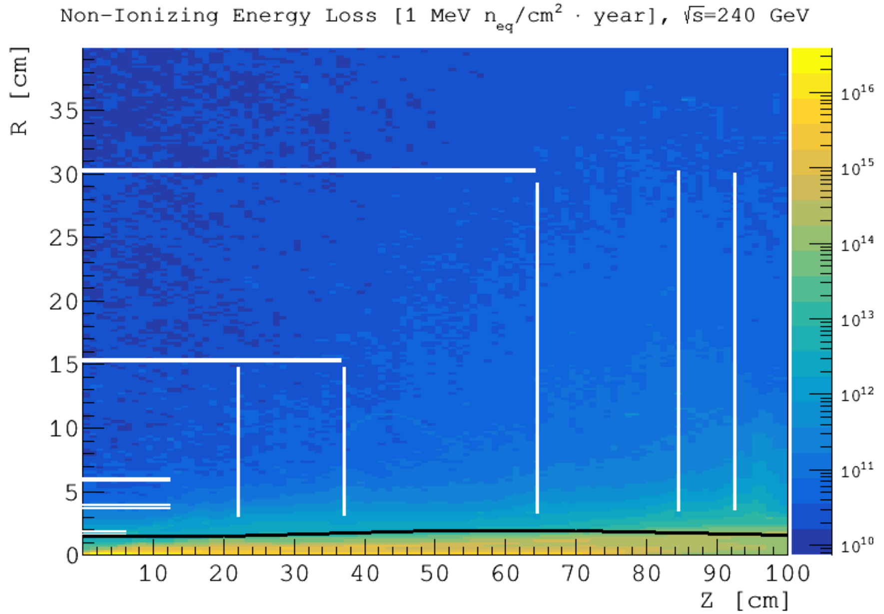
	Higgs	*W*	*Z (3T)*	*Z (2T)*
Number of IPs	2			
Beam energy (GeV)	120	80	45.5	
Circumference (km)	100			
Synchrotron radiation loss/turn (GeV)	1.73	0.34	0.036	
Crossing angle at IP (mrad)	16.5×2			
Piwinski angle	2.58	7.0	23.8	
Number of particles/bunch N_e (10^{10})	15.0	12.0	8.0	
Bunch number (bunch spacing)	242 (0.68μs)	1524 (0.21μs)	12000 (25ns+10%gap)	
Beam current (mA)	17.4	87.9	461.0	
Synchrotron radiation power /beam (MW)	30	30	16.5	
Bending radius (km)	10.7			
Momentum compact (10^{-5})	1.11			
β function at IP β_x^* / β_y^* (m)	0.36/0.0015	0.36/0.0015	0.2/0.0015	0.2/0.001
Emittance $\varepsilon_x/\varepsilon_y$ (nm)	1.21/0.0031	0.54/0.0016	0.18/0.004	0.18/0.0016
Beam size at IP σ_x/σ_y (μm)	20.9/0.068	13.9/0.049	6.0/0.078	6.0/0.04
Beam-beam parameters ξ_x/ξ_y	0.031/0.109	0.013/0.106	0.0041/0.056	0.0041/0.072
RF voltage V_{RF} (GV)	2.17	0.47	0.10	
RF frequency f_{RF} (MHz) (harmonic)	650 (216816)			
Natural bunch length σ_z (mm)	2.72	2.98	2.42	
Bunch length σ_z (mm)	3.26	5.9	8.5	
Betatron tune ν_x/ν_y	363.10 / 365.22			
Synchrotron tune ν_s	0.065	0.0395	0.028	
HOM power/cavity (2 cell) (kw)	0.54	0.75	1.94	
Natural energy spread (%)	0.1	0.066	0.038	
Energy acceptance requirement (%)	1.35	0.4	0.23	
Energy acceptance by RF (%)	2.06	1.47	1.7	
Photon number due to beamstrahlung	0.29	0.35	0.55	
Lifetime _simulation (min)	100			
Lifetime (hour)	0.67	1.4	4.0	2.1
F (hour glass)	0.89	0.94	0.99	
Luminosity/IP *L* ($10^{34}cm^{-2}s^{-1}$)	2.93	10.1	16.6	32.1

Radiation Background Levels

H. Zhu, CEPC Workshop Rome May 24-26 2018

- Using hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) to quantify the radiation background levels
- Adopted the calculation method used for the ATLAS background estimation (ATL-GEN-2005-001), safety factor of ×10 applied





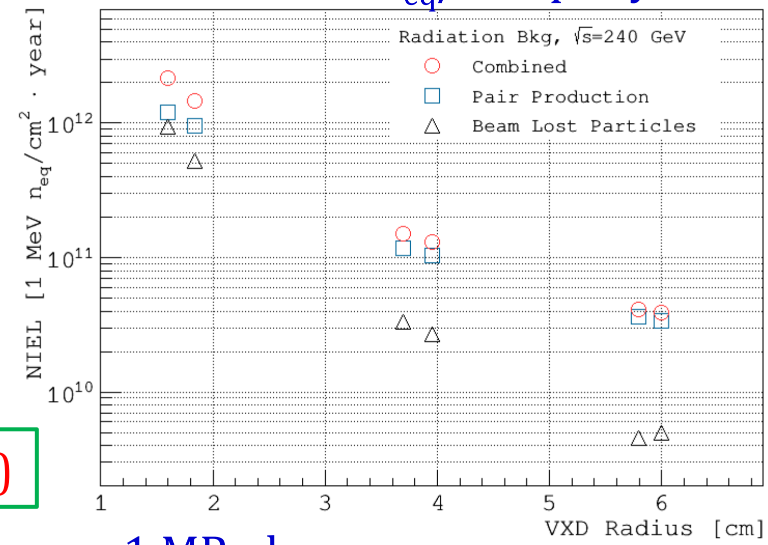
Combined Beam-Induced Backgrounds

H. Zhu, CEPC Workshop Rome May 24-26 2018

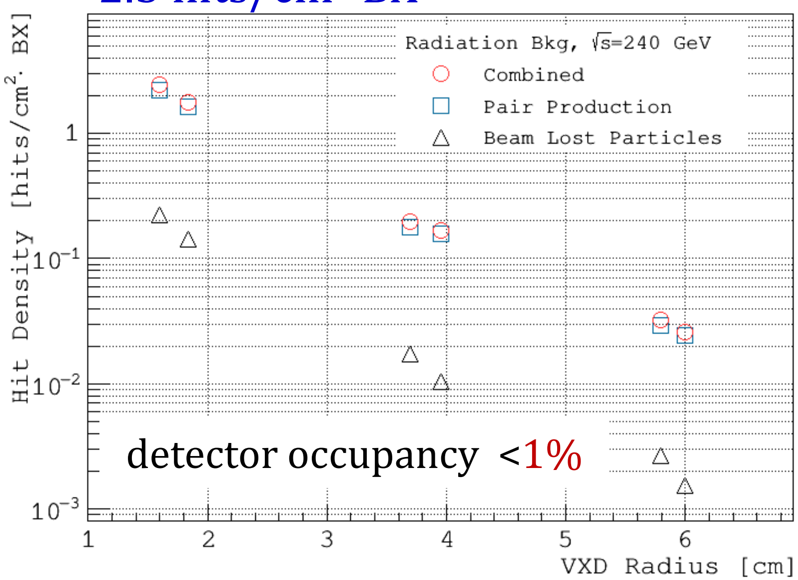
- Radiation backgrounds from pair production, radiative Bhabha scattering + beamstrahlung
- Most significant contributions from the pair production

(safety factor: 10)

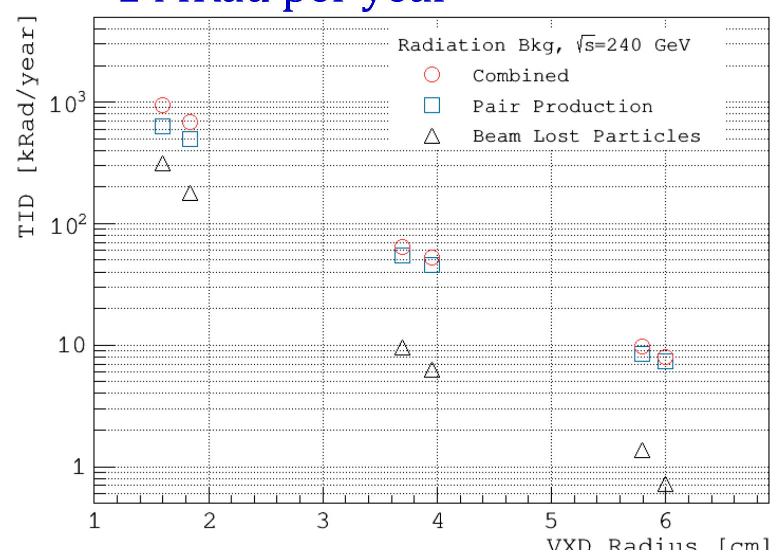
2×10^{12} 1MeV n_{eq}/cm^2 per year



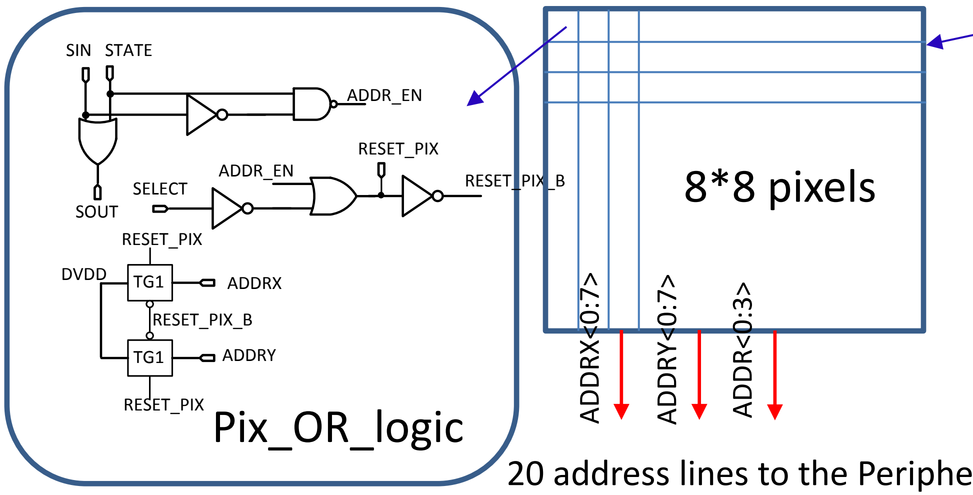
2.5 hits/cm^2 BX $^{-1}$

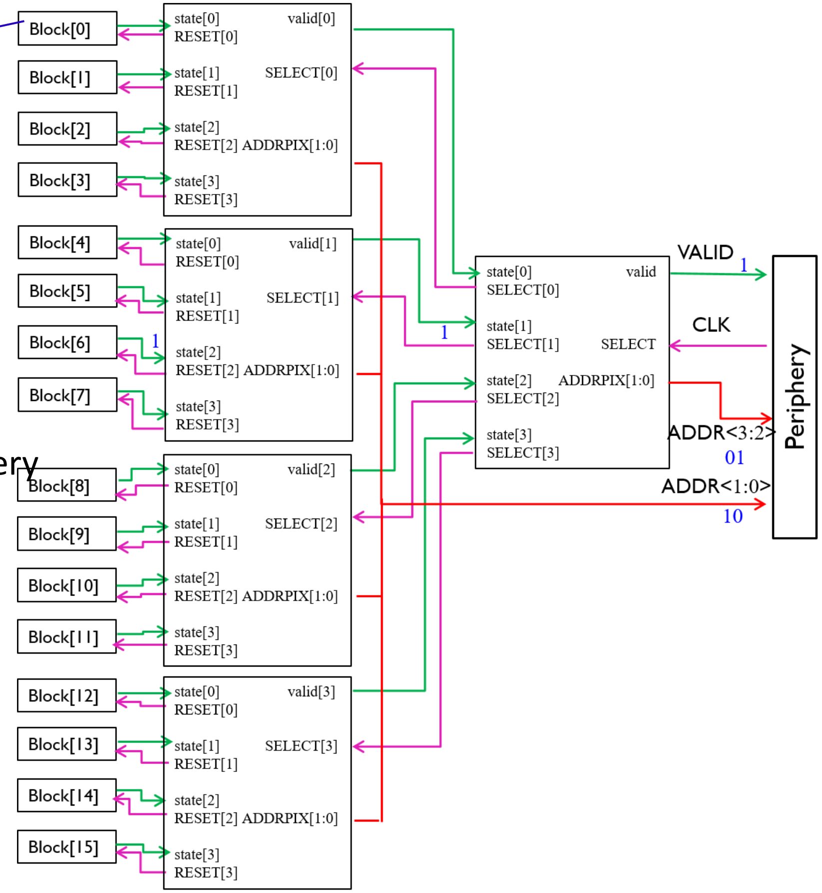


1 MRad per year



MIC4 Readout architecture

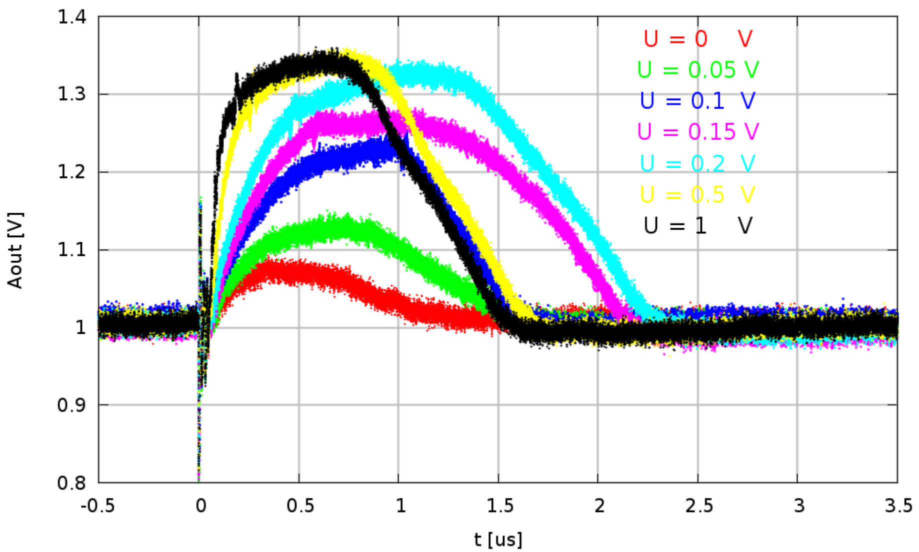


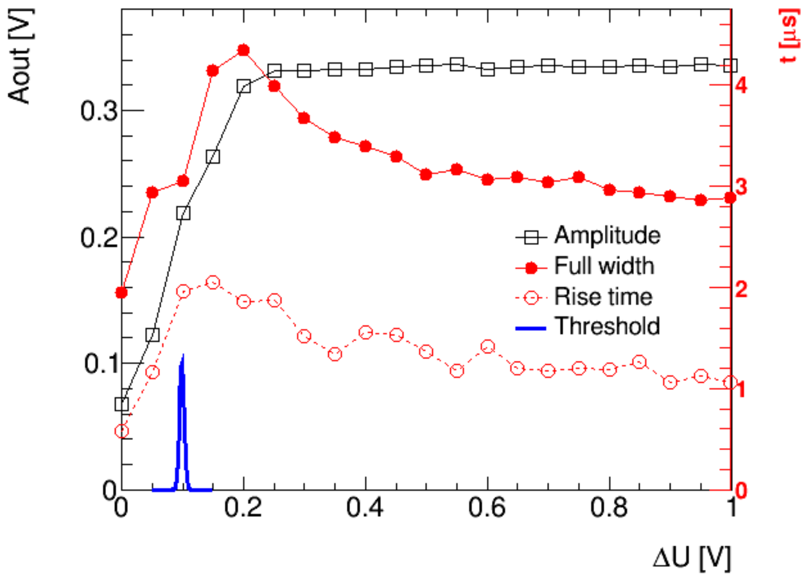


Matrix readout architecture:

- **AERD (Address-Encoder and Reset-Decoder)** many connection lines occupy larger area than the logic circuit itself
- **OR gate chain:** speed is limited with the number of the chain pixels
- **Combine these two solutions:** 64 pixels as a group using OR gate chain, groups using AERD structure to readout

Characterization of Analog Front-end in MIC4

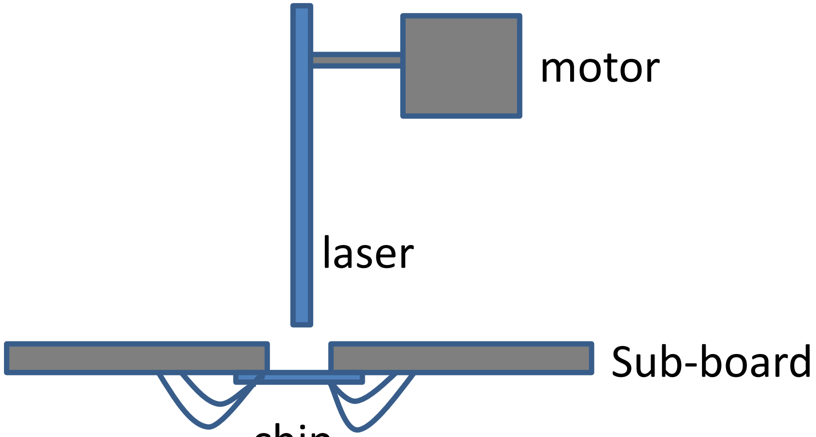




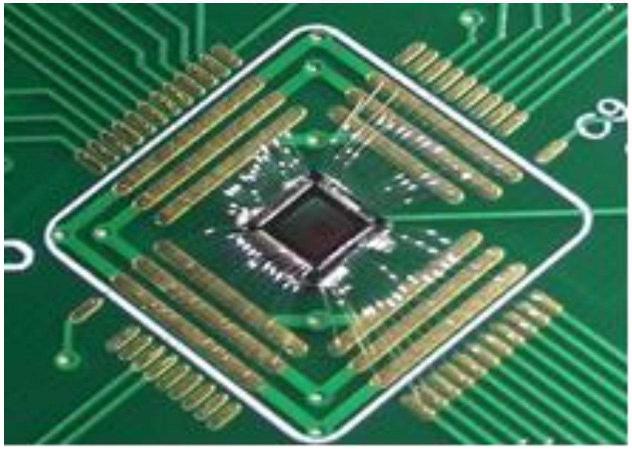
Analog output parameters as a function of the amount of injected charge.

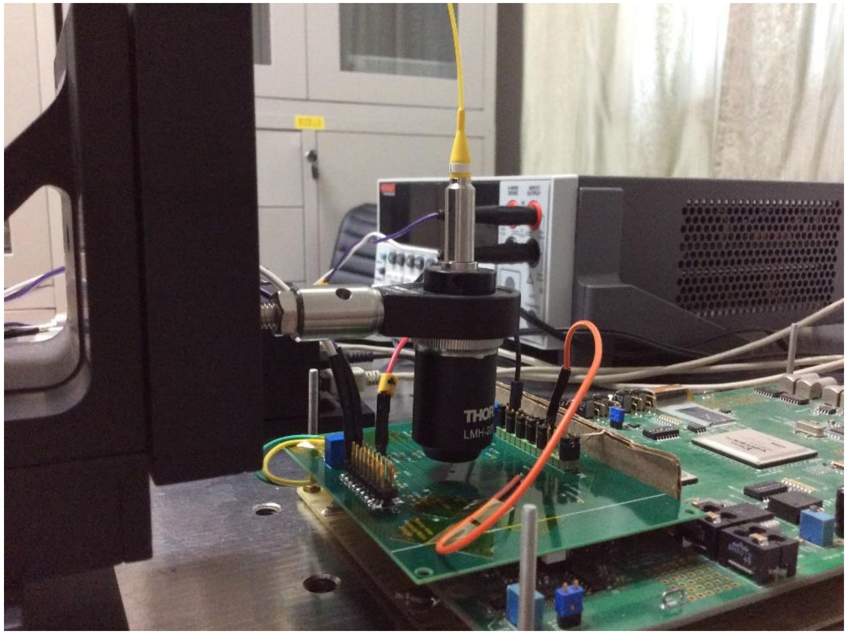
- The front-end response is non-linear which is as expected.
- Peaking time < 1 μs, duration < 3 μs, close to the simulation results.

Laser Test Setup



- 1064nm laser beam
  - Focused beam waist ~ 3.4 um
  - Energy adjustable ~ pJ/pulse
- 3-dimensional stepping motor
  - Minimum step size: 0.1um
- Thinning chip (75 um)
  - Backside illumination (no aluminum)

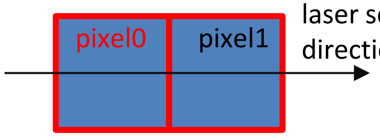


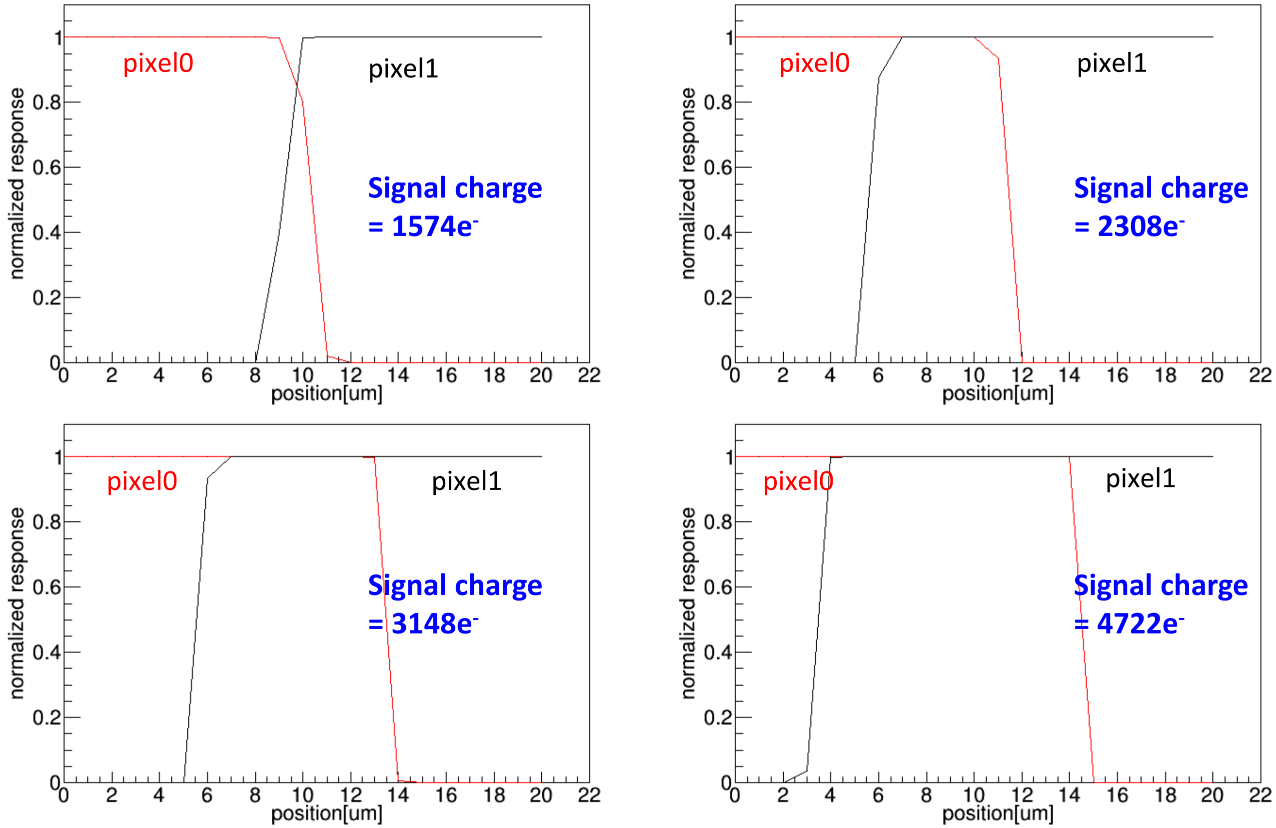


Laser position scan with different laser intensity

Scan two adjacent digital pixels

- –Step size of 1um
- –Threshold is fixed (minimum threshold without noise hit)





Normalized response
= hits / pulses