An updated design of the read out link and control board for the Phase-2 upgrade of the ATLAS Tile Calorimeter.

**Introduction.**

The High-Luminosity Large Hadron Collider (HL-LHC) will have an increased instantaneous luminosity of five to seven times the nominal design value. ATLAS (Figure 1d) Phase-II upgrade program for the Hadronic Tile Calorimeter (TileCal) (Figure 1c) [1] will compensate for the higher radiation levels and higher rates of pileup by fully replacing the present aged readout electronics. The new design will assure better timing and energy resolution and decreased sensitivity to out-of-time pileup by adopting a fully-digital trigger system that will provide full-granularity data to the off-detector system. To achieve continuous read-out of the entire TileCal within HL-LHC conditions, a radiation tolerant design of a read-out link and control board (Daughterboard) powered by multiGBPS optic transceivers will interface the on- and off-detector system. We present the updated design of the Daughterboard and preliminary results from the TID radiation tests performed.

**ATLAS Hadronic Tile Calorimeter (Figure 1).**

TileCal is a sampling calorimeter composed of plastic scintillator tiles as active material interleaved with steel plates as absorber. The detector is divided in four cylindrical barrels (Figure 1b) composed of 64 wedge-shaped modules each (Figure 1a). The scintillators in each module are grouped in pseudo-projective cells. Light from two sides of a cell is collected by wavelength shifting fibers and read out by two photomultiplier tubes (PMTs) (Figure 1a).

**Phase-II upgrade read-out system (Figure 2).**

The Phase II read-out system (Figure 2) will sample all the TileCal signals at 40 MHz. The system is modularized in Superdrawers (SDs), each divided in 4 Mindrawers (MDs) (Figure 2c).

- Each MD serves up to 12 channels, each consisting in a Front-End Board (FEB) that shapes and conditions two gains of the PMT signals before they are digitized in a Mainboard (MB) (Figure 2a). A Daughterboard (DB) provides LHC synchronized timing, control and configuration to the front-end, and continuous readout of the Mainboard (MB) channels to the off-detector system.
- A Tile Preprocessor receives and stores two gains of PMT data in pipelines until a trigger decision event is received and in parallel provides reconstructed data to the trigger, all at 40 MHz (Figure 2b).
- Upon the reception of a trigger signal, the data is read out by the FELIX system (Figure 2b).

**DB Revision 5 design (Figures 3 and 4).**

The DB Revision 5 design main features are:

- Double Redundant design that allows nomally running with either one or two working links.
- Migration from Kintex-7 (GTYS transceivers) to Kintex Ultrascale+ (GTYS transceivers) to improve radiation tolerance[3] and the Kintex-7 XADC.
- New digital unique ID serial chip and xADC panel for extra sensor monitoring.
- Double Readout link with 4x QSFP+ to 4x SFP+ servicing.
- Backward compatible with legacy HV-OPTO, FMC and Cs interface options[2].
- New digital unique ID serial chip and xADC panel for extra sensor monitoring.
- Migration from 2x QSFP to 4x SFP+ servicing:
  - Recovering 2x 160 MHz LHC synchronized clocks to drive both FPGAs transceivers.
  - Recovering 6x 40 MHz TTC phase configurable clocks, 2 for driving the FPGAs relevant logic and 4 for driving the digitizing blocks on each Mindrayer quadrant.
  - Propagating configuration and control commands to both FPGAs through the EPorts via a configuration bus.
  - Propagating remote FPGA resets and remote configuration of FPGAs and PROMs though the EPorts by means of controlling both FPGAs JTAG chains (the TDO returning signal is transmitted from the opposite FPGA uplink).
- Two pairs of redundant readout uplinks from the FPGAs powered with TMR capable firmware providing continuous GBT CRC protected words with two gains of digitized data and SC information to the back-end via GTYS transceivers.

**TID tests.**

A DB with functional firmware connected to a TilePPr was exposed to a total of 20 kRad delivered by a 9 MeV electron beam (Figure 5) in six doses over ~ 1 hr (Figure 6a), following the ESCC-22900 standard[5]:

- Level E of TID (20kRad/200y) Standard Rate (Window 1): 365 Rad(Si) / min @ 9 MeV and 381 Rad(Si) / min @ 12 MeV.
- Between doses, the system was power cycled and FPGAs reconfigured from the PROMs.
- Monitored currents were constant over the full dose, apart from the GBTx which had a small but measurable current decrease over the 20 kRad exposure (Figure 6b).
- Temperature and current monitoring showed no evidence of latch-up (Figure 6c).
- Core FPGA voltages were extremely stable over entire irradiation period (Figure 6d).

No component failures:

- FPGAs, GBTx, PROMs,
- Two types of SFP+ tested:
  - CORETEK CT-000NPP-SB1L-D (baseline),
  - AVAGO AFBR-7095MZ.

**References.**


**Outlook.**

The DB revision 5 was designed to meet all the requirements for the Phase-II Upgrade. Currently, it is being integrated to the Mindrawers and firmware development and improvement is taking place. Good preliminary results on TID radiation tests were seen. However, they need to be adjusted to new ATLAS simulation values according to the ATLAS protocol and safety factors. Radiation tests for NIEL took place during May with pending analysis and SEU is planned for September 2018. Near future plans include integrating it in the beam campaign that will take place in October 2018.

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