Level-1 Calorimeter Trigger
from Virtex-7 to UltraScale+

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Mainz
Introduction to the Current System

• Trigger System for the ATLAS Experiment @ LHC
• Level-1 Topological Processor (L1Topo)
  → Hardware, Firmware & Performance

Future Upgrades of the Level-1 Calorimeter Trigger

• Quick Overview
• Jet Feature EXtractor (jFEX) & New L1Topo
  → Hardware, Firmware, FPGA Resource Usage & Test Results
Introduction
Introduction
Trigger System for the ATLAS Experiment @ LHC

Run-1 (2009 to 2013)

Level-1: FPGA based Hardware Trigger

↓ First Upgrade (2013 to 2015)

Run-2 (2015 to 2018)

With the Topological Processor (L1Topo) it became possible for the first time to transfer 4-vectors of all Trigger Objects (TOBs) for the full event to a single module and process them with FPGAs.
Technical Details of the L1Topo System @ Run-2:

• 2 ATCA boards
• 2 processor FPGAs (Xilinx Virtex-7) plus 1 FPGA (Xilinx Kintex-7) for control and readout to DAQ per module

Input:

• Trigger Objects (TOBs), e.g. Jets, myons, electrons, photons, taus

FPGA Processing:

• Angular distances, missing energy, transverse and invariant mass calculations etc.

Output:

• *Trigger data* is sent to the L1CTP
L1Topo Algorithms:

**Input**

- Trigger Objects (TOBs)

**Sort & Select**

- Reduction of input lists to ensure fast processing

**Topological Algorithms**

- Calculations of event topological variables

**Output**

- Results & Overflows

**Exotic Example: Late-Muon (Sort) Algorithm**

→ Meant for new heavy (long lived) particles decaying in muons

- event $N$
  - new heavy particle

- event $N+1$
  - delayed muon from event $N$

→ Most energetic delayed muon is used in topological cuts with jets / MET from earlier bunchtick
L1Topo Trigger Performance in Run-2: already presented by D. Zanzi

Significant reduction of background rates while keeping a good signal efficiency without raising $E_T$ thresholds

- **Rate reduction and trigger efficiency** are shown below for B-physics dimuon triggers
  - overall reduction of the rate by a factor of 4 (left plot)
  - only small efficiency losses of about 12% (right plot)

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TriggerOperationPublicResults
upgrades
Future Upgrades of the Level-1 Calorimeter Trigger
Quick Overview

Next Upgrade (2019 to 2020)

- **New readout** of the calorimeters
- **Increased granularity** becomes available for the hardware triggers
  → the entire trigger must be **rebuilt**

Run-3 (2021 to 2023)

**Level-1: FPGA based Hardware Trigger**

- **Muon Trigger**
- **Calorimeter Trigger**
  - **Feature Extractors**
  - Electron Feature Extractor (eFEX) → e/γ, τ
  - Jet Feature Extractor (jFEX) → Jets, τ, ΣE_T, E_T^{miss}
  - Global Feature Extractor (gFEX) → Large-R Jets

**CPUs**

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July 5, 2018
Technical Details of the jFEX System:

- 6 ATCA boards
- 4 processor FPGAs (Xilinx UltraScale+) plus extension mezzanine equipped with one FPGA (Xilinx Artix 7) for control
- 120 multi-gigabit transceivers (MGTs) per FPGA (up to 12.8 Gbps link speed)

New L1Topo based on jFEX:

- 3 ATCA boards (only 2 for Run-2)
- 2 processor FPGAs (Xilinx UltraScale+) per module
- 118 input (24 output) fibres per processor FPGA (up to 12.8 Gbps link speed)

→ First prototype expected soon
Jet Feature EXtractor (jFEX)
Firmware Algorithms – Block Diagram

Menu / Databases

Parameters

LAr

Tile

Noise Suppression

Pile-up Subtraction

LAr + Tile

LAr + Tile

LAr, Tile

Small-Area Jets

Large-Area Jets

jFEX Taus

Global Variables

TOB Generation & Sorting

Output: Trigger Objects (TOBs):
- $\eta$ and $\phi$ coordinates
- Transverse Energy
- ...

Input: Calorimeter Tower Energies:

Maximum processing time: 6 bunchticks ($= 150$ ns)

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July 5, 2018
jFEX & New L1Topo
FPGA Resource Utilization

- **jFEX Lookup table (LUT) resource usage:**
  - Central region
    - (different in the forward region)
    - Used: 18%
    - Available: 82%

- **L1Topo LUT resource usage:**
  - Run-2 system → Run-3 system (preliminary)
    - Current system (coarse granularity)
    - Used: 29%
    - Available: 71%
    - jFEX (fine granularity)
    - Used: 22%
    - Available: 78%

new (larger) FPGAs allow implementations of much more complex algorithms
Power Consumption:

- All multi-gigabit transceivers enabled
- 11.2 Gbps link speed
  - Link speed tests successfully done up to 12.8 Gbps

Thermal Measurement:

- All multi-gigabit transceivers enabled
  - no critical temperatures observed

### Power Consumption Table

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<th>Voltage Rail</th>
<th>Current (A)</th>
<th>Temp. (°C)</th>
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</table>

**Total (W)**

- 265.86

→ well within limits of ATCA standard (400 W)
Summary:

• **jFEX / upgraded L1Topo** are boards based on Xilinx **UltraScale+** FPGAs running at a link speed of **up to 12.8 Gbps**
  → has been shown to work reliably in prototype testing

• The **larger FPGAs** allow implementations of **much more complex algorithms**
  → improvements in performance have been shown in high-level simulations

Outlook:

• **Final production** in the second half of 2018
• **Integration tests** at the beginning of 2019
• **Installation** in autumn 2019
Thanks for your attention.