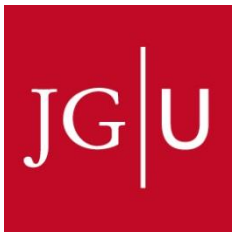
Level-1 Calorimeter Trigger

from Virtex-7 to UltraScale+



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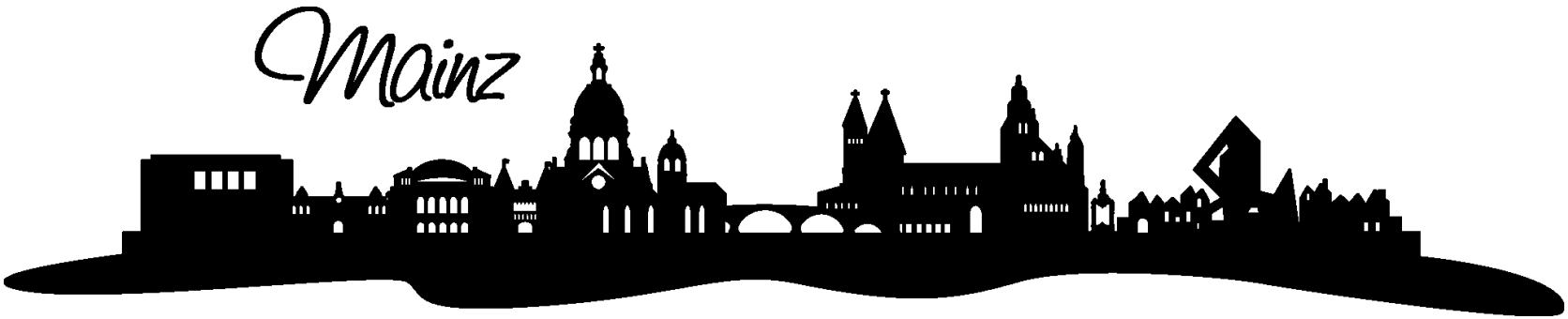


Outline

Introduction to the Current System

- Trigger System for the ATLAS Experiment @ LHC
- Level-1 Topological Processor (L1Topo)

  → Hardware, Firmware & Performance

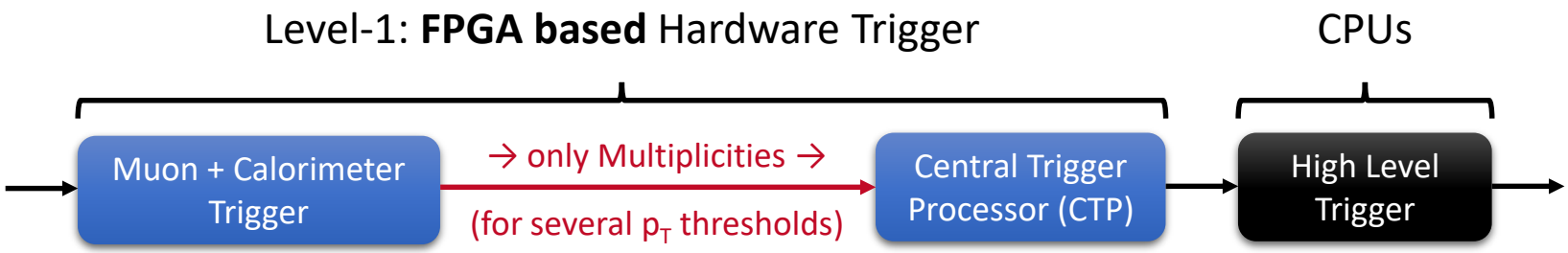
Future Upgrades of the Level-1 Calorimeter Trigger

- Quick Overview
- Jet Feature EXtractor (jFEX) & **New** L1Topo

  → Hardware, Firmware, FPGA Resource Usage & Test Results

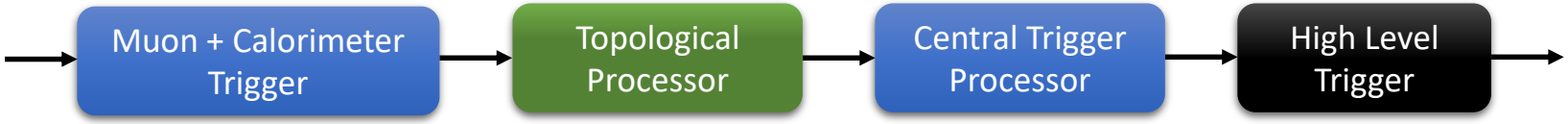
Introduction

Run-1 (2009 to 2013)



↓ First Upgrade (2013 to 2015)

Run-2 (2015 to 2018)



With the **Topological Processor (L1Topo)** it became possible for the first time to **transfer 4-vectors of all Trigger Objects (TOBs)** for the full event to a single module and process them with FPGAs.

Technical Details of the L1Topo System @ Run-2:

- 2 ATCA boards
- 2 processor FPGAs (Xilinx **Virtex-7**) plus 1 FPGA (Xilinix Kintex-7) for control and readout to DAQ per module

Input:

- Trigger Objects (TOBs), e.g. Jets, myons, electrons, photons, taus

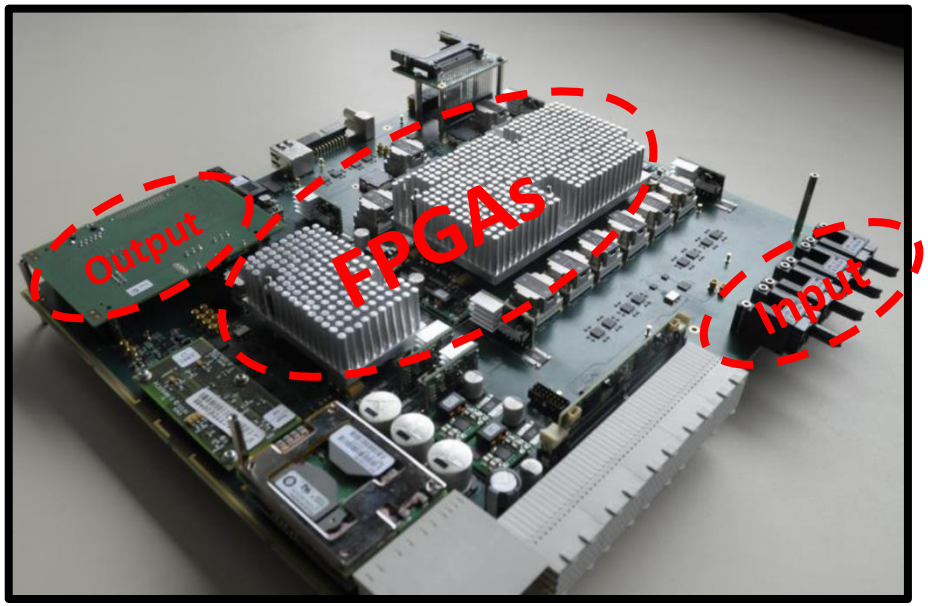
FPGA Processing:

- Angular distances, missing energy, transverse and invariant mass calculations etc.

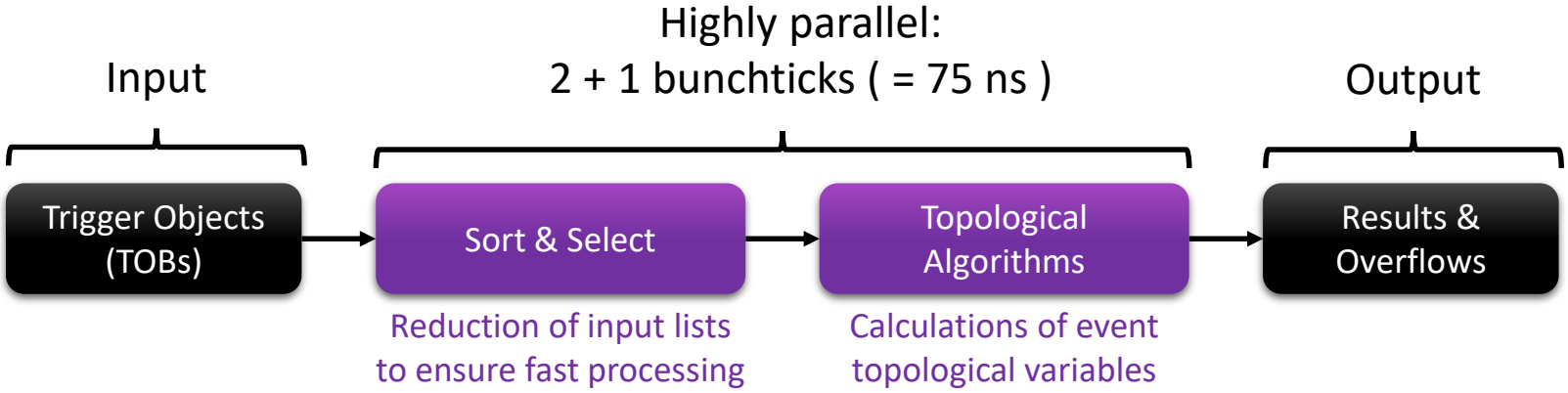
Output:

- *Trigger data* is sent to the L1CTP

↓ L1Topo module ↓

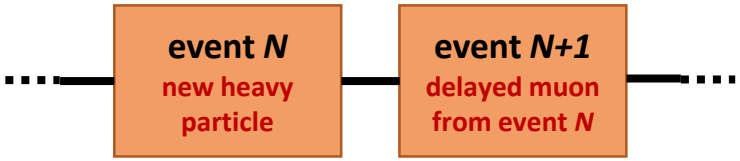


L1Topo Algorithms:

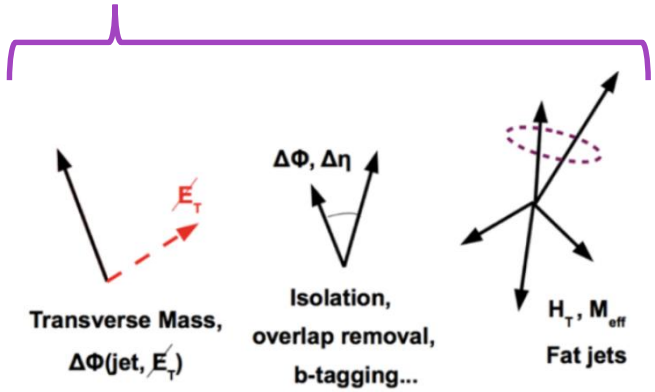


Exotic Example: Late-Muon (Sort) Algorithm

→ Meant for **new heavy** (long lived) particles decaying in muons



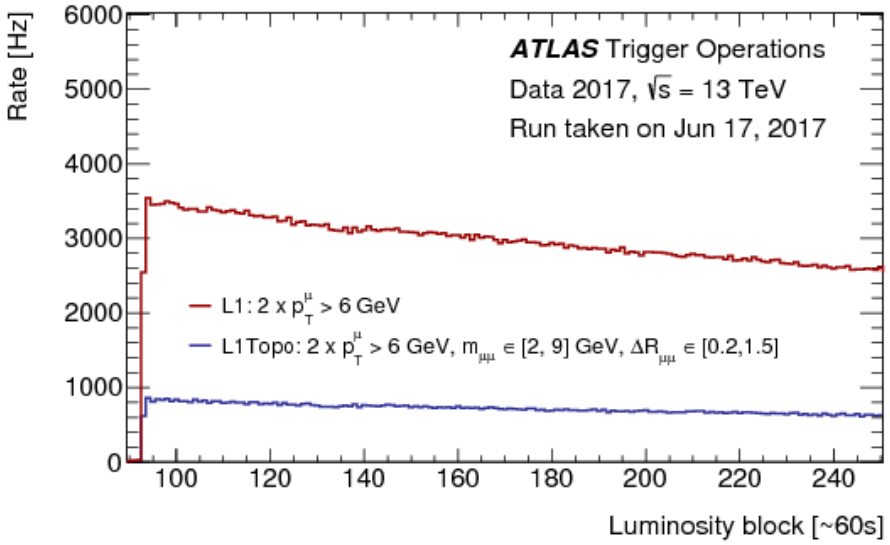
→ Most energetic **delayed** muon is used in topological cuts with jets / MET from **earlier** bunchtick

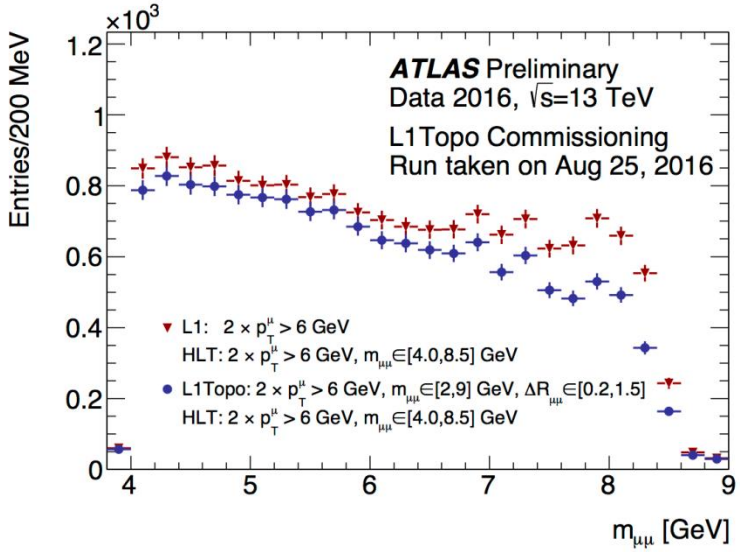


L1Topo Trigger Performance in Run-2: → already presented by D. Zanzi

Significant reduction of background rates while keeping a good signal efficiency without raising E_{T} thresholds

- **Rate reduction and trigger efficiency** are shown below for B-physics dimuon triggers
  - → overall reduction of the rate by a factor of 4 (**left plot**)
  - → only small efficiency losses of about 12% (**right plot**)





https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TriggerOperationPublicResults

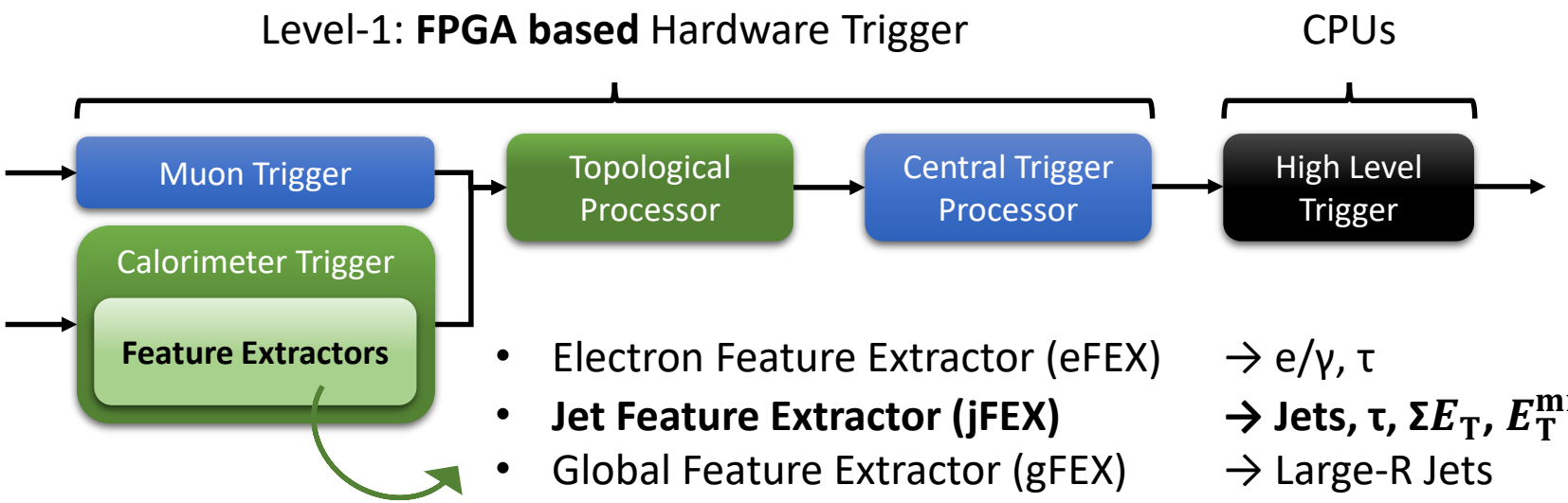
Upgrades

Future Upgrades of the Level-1 Calorimeter Trigger
Quick Overview

Next Upgrade (2019 to 2020)

- **New readout** of the calorimeters
- **Increased granularity** becomes available for the hardware triggers
  → the entire trigger must be **rebuilt**

Run-3 (2021 to 2023)



Future Upgrades of the Level-1 Calorimeter Trigger
Jet Feature EXtractor (jFEX) & New L1Topo

Technical Details of the jFEX System:

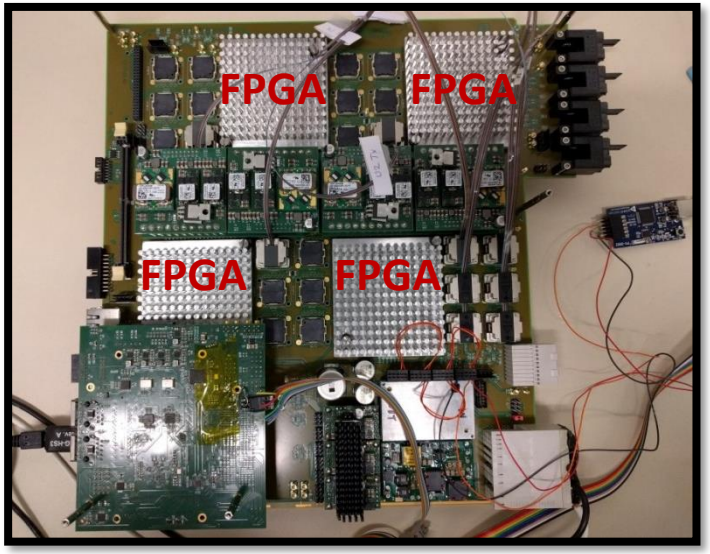
- 6 ATCA boards
- 4 processor FPGAs (Xilinx **UltraScale+**) plus extension mezzanine equipped with one FPGA (Xilinx Artix 7) for control
- 120 multi-gigabit transceivers (MGTs) per FPGA (up to 12.8 Gbps link speed)

New L1Topo based on jFEX:

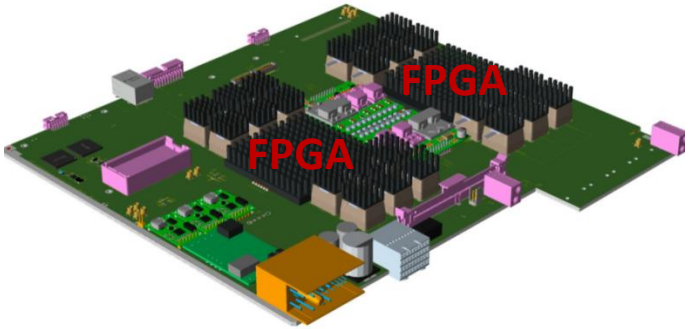
- 3 ATCA boards (only 2 for Run-2)
- 2 processor FPGAs (Xilinx **UltraScale+**) per module
- 118 input (24 output) fibres per processor FPGA (up to 12.8 Gbps link speed)

→ First prototype expected soon

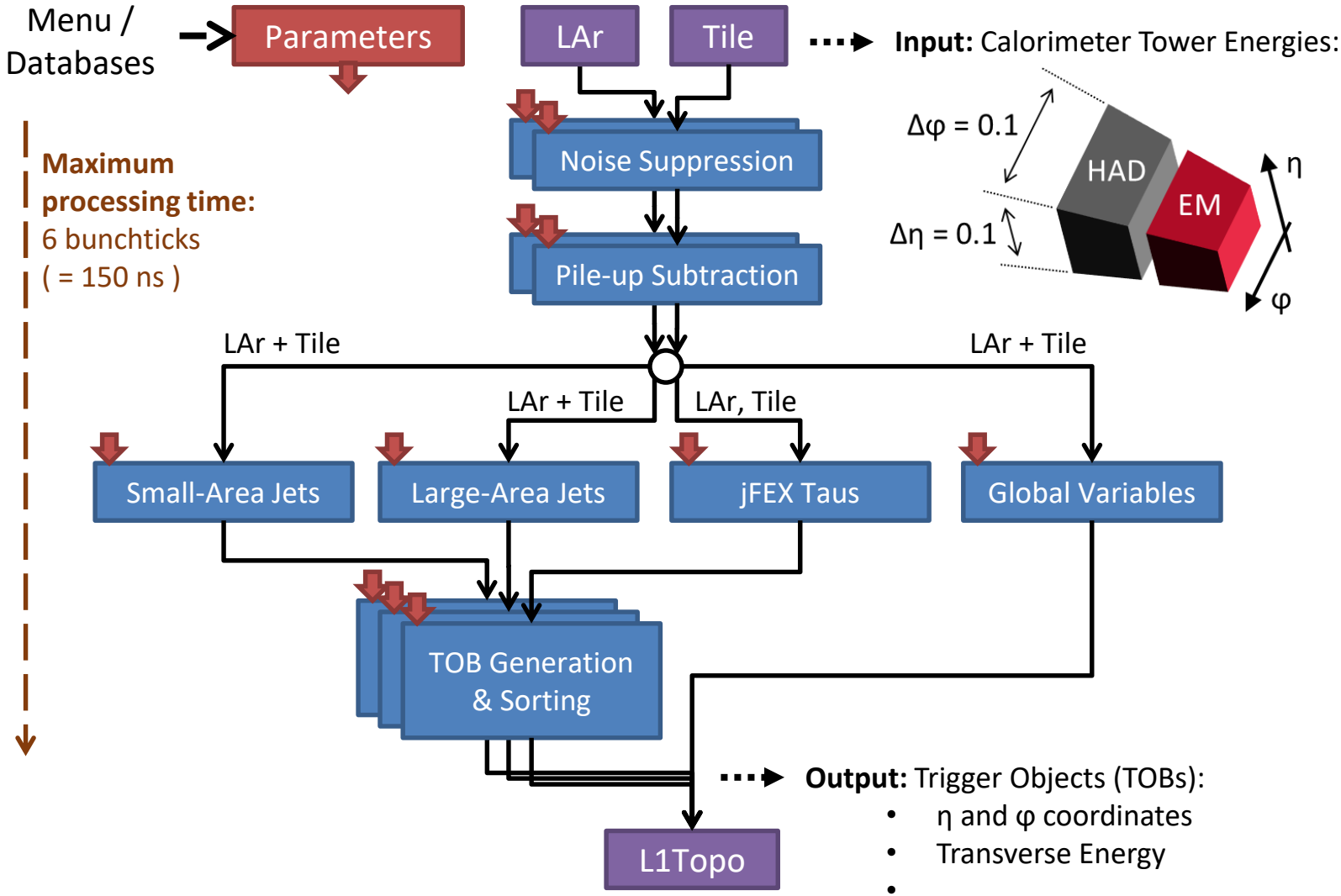
↓ jFEX final prototype ↓



↓ New L1Topo (3D computer generated) ↓



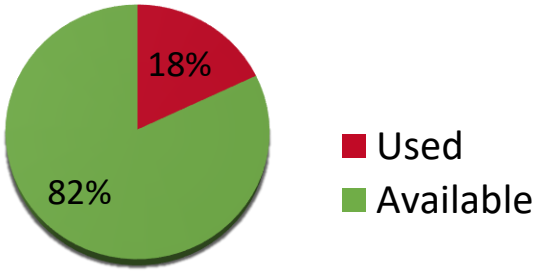
Jet Feature EXtractor (jFEX)
Firmware Algorithms – Block Diagram



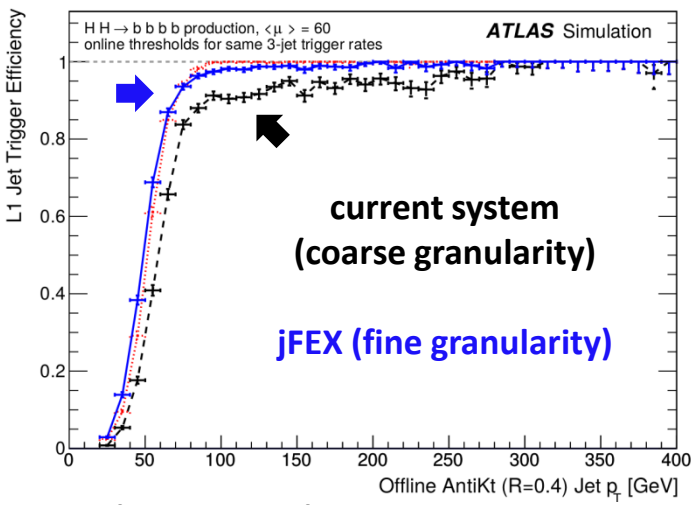
jFEX & New L1Topo
FPGA Resource Utilization

- **jFEX Lookup table (LUT)** resource usage:

Central region
(different in the forward region)



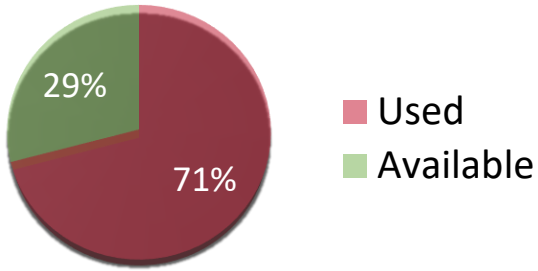
↓ jFEX Performance Studies ↓

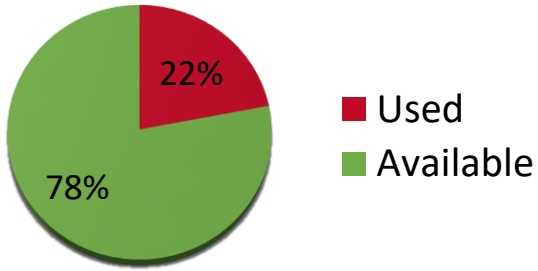


https://cds.cern.ch/record/2309479

- **L1Topo LUT** resource usage:

Run-2 system ——→ **Run-3 system (preliminary)**





➡ **new (larger) FPGAs allow implementations of much more complex algorithms**

jFEX Final Prototype
Hardware Test Results

Power Consumption:

- All multi-gigabit transceivers enabled
- 11.2 Gbps link speed
  - ↘ Link speed tests successfully done up to 12.8 Gbps

Supply	Voltage Rail	Current (A)	Temp. (°C)
Board Level Voltages	1V8	0.47	32.00
	2V5	14.55	–
	3V3	7.42	30.00
U1	$V_{CCINT\ (0.85V)}$	23.75	44.00
	$MGTYAV_{CC\ (0.9V)}$	10.95	46.00
	$MGTYAV_{TT\ (1.2V)}$	20.42	52.00
U2	$V_{CCINT\ (0.85V)}$	20.41	36.00
	$MGTYAV_{CC\ (0.9V)}$	10.75	39.00
	$MGTYAV_{TT\ (1.2V)}$	20.43	45.00
U3	$V_{CCINT\ (0.85V)}$	17.17	38.00
	$MGTYAV_{CC\ (0.9V)}$	10.45	43.00
	$MGTYAV_{TT\ (1.2V)}$	20.14	48.00
U4	$V_{CCINT\ (0.85V)}$	18.82	38.00
	$MGTYAV_{CC\ (0.9V)}$	10.73	39.00
	$MGTYAV_{TT\ (1.2V)}$	20.21	45.54
Total (W)			265.86

→ well within limits of ATCA standard (400 W)

Thermal Measurement:

- All multi-gigabit transceivers enabled

↘ no critical temperatures observed

Summary & Outlook

Summary:

- **jFEX / upgraded L1Topo** are boards based on Xilinx **UltraScale+** FPGAs running at a link speed of **up to 12.8 Gbps**
  → has been shown to work reliably in prototype testing
- The **larger FPGAs** allow implementations of **much more complex algorithms**
  → improvements in performance have been shown in high-level simulations

Outlook:

- **Final production** in the second half of 2018
- **Integration tests** at the beginning of 2019
- **Installation** in autumn 2019

Thanks
for your attention.