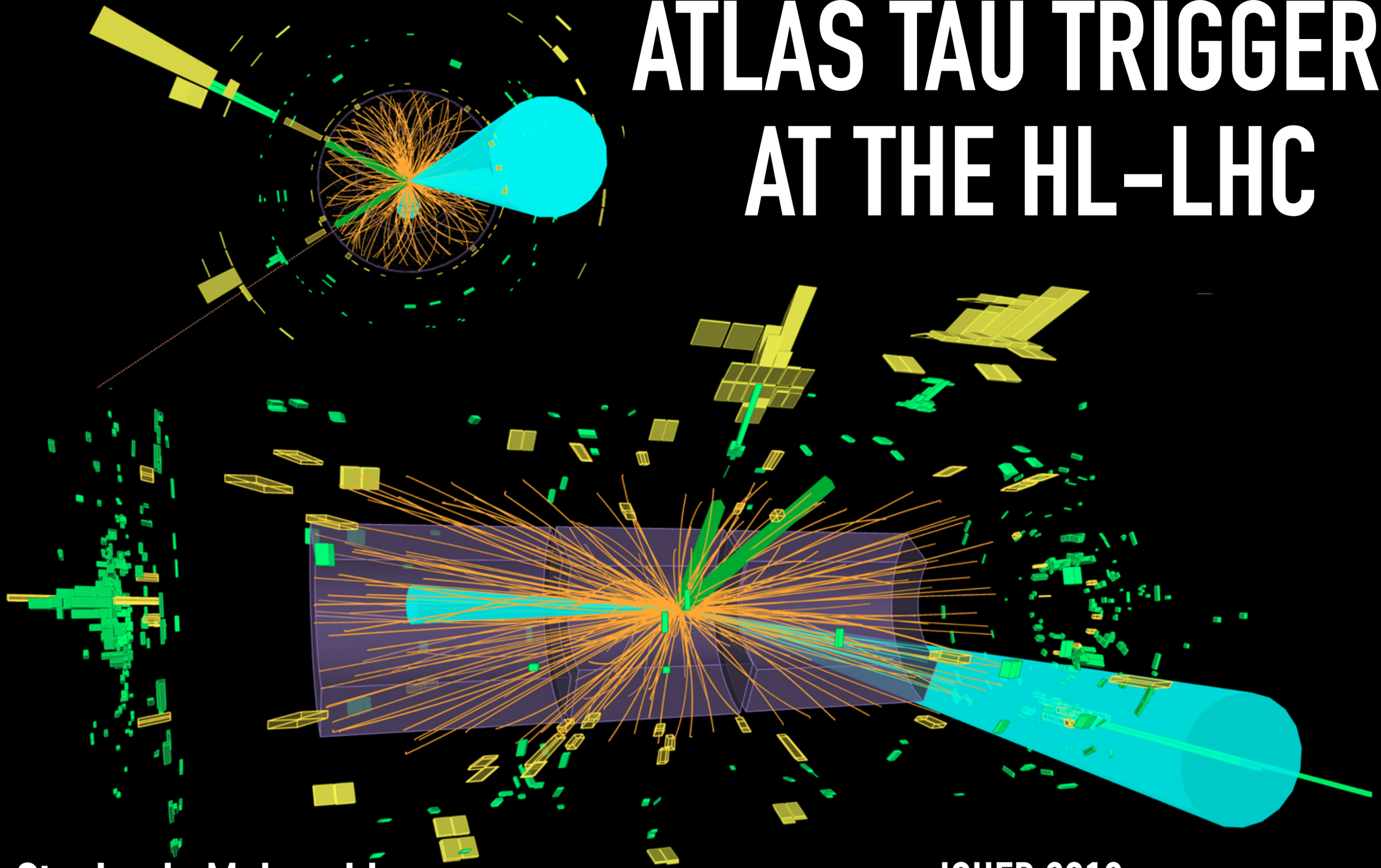
ATLAS TAU TRIGGERS AT THE HL-LHC

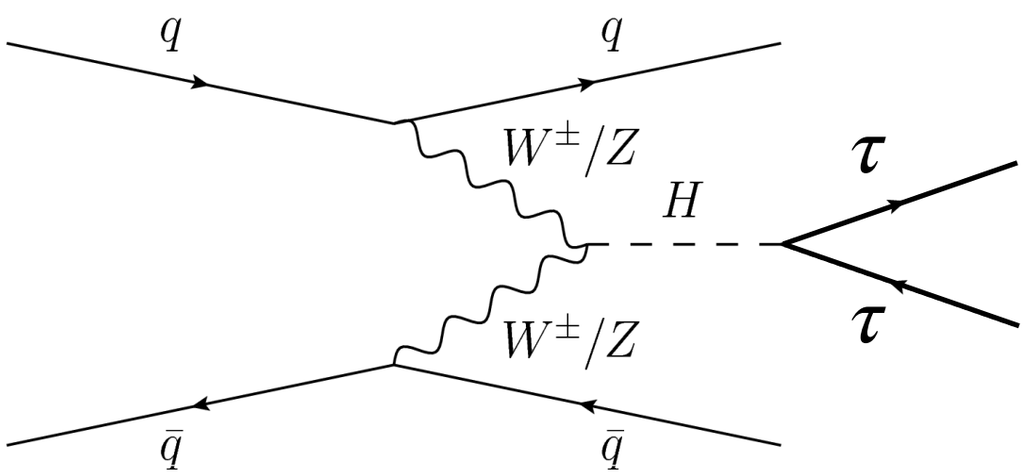


Stephanie Majewski
University of Oregon,
on behalf of the ATLAS Collaboration

ICHEP 2018
Seoul, South Korea
July 4-11, 2018

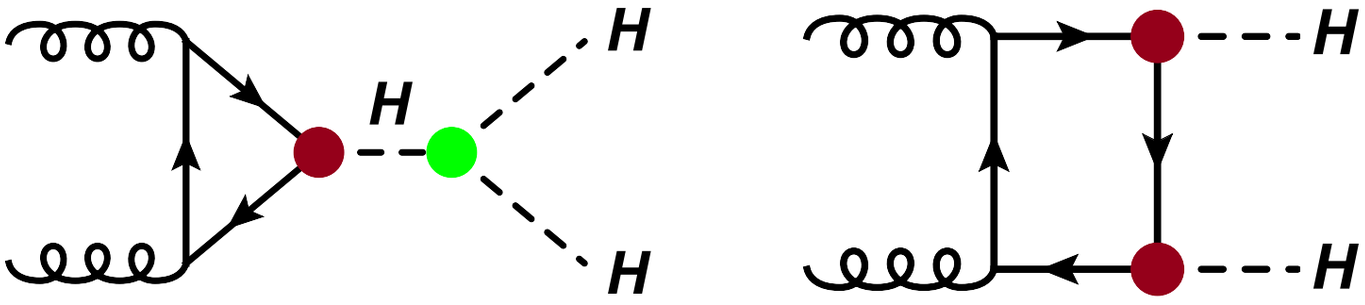
PHYSICS MOTIVATION: HIGGS AND DI-HIGGS AT THE HL-LHC

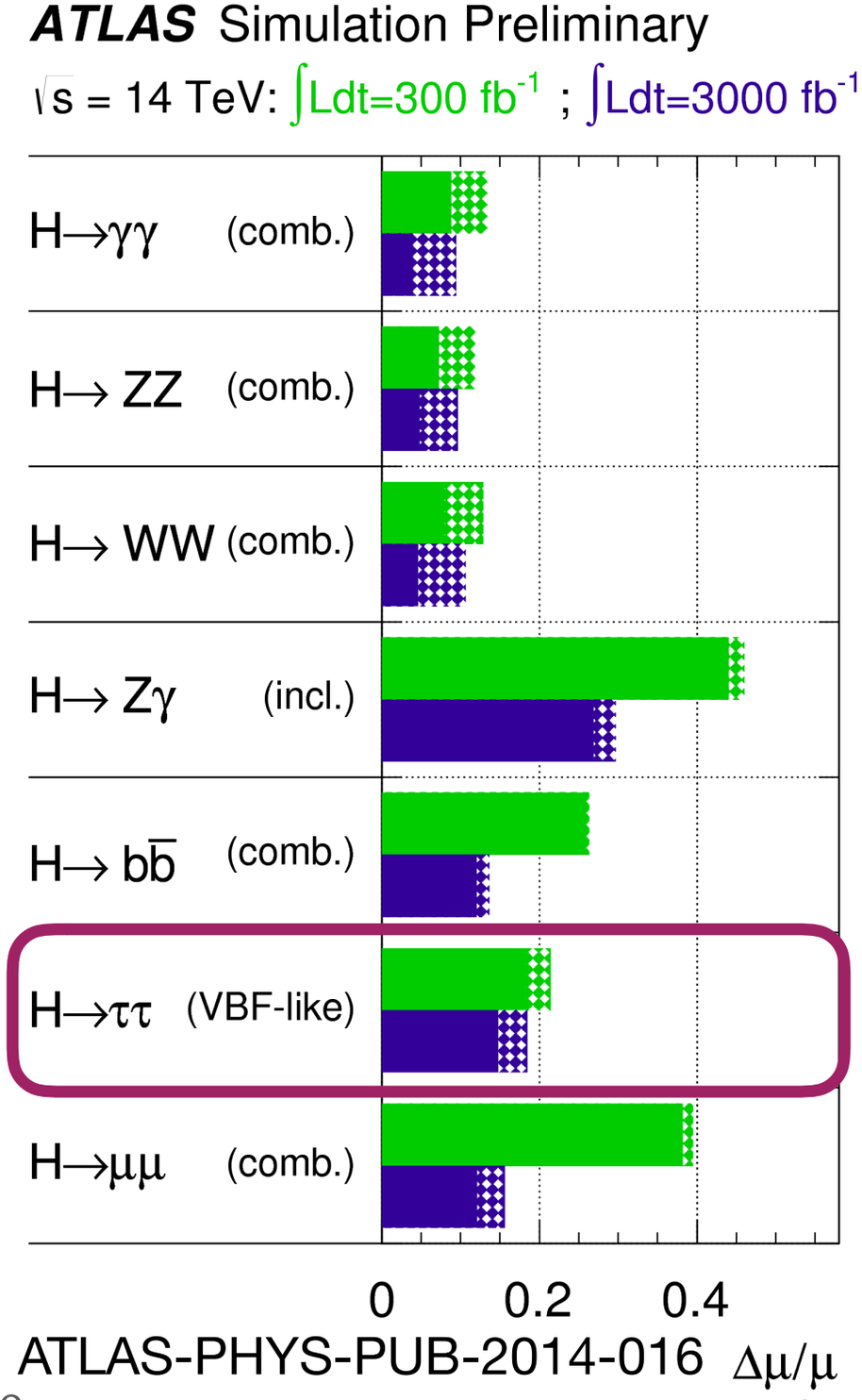
- Higgs production through Vector Boson Fusion



- Di-Higgs production

$$\sigma(pp \to HH) = 39.5^{+2.9}_{-3.2}\,\text{fb at}\,\sqrt{s} = 14\,\text{TeV}$$





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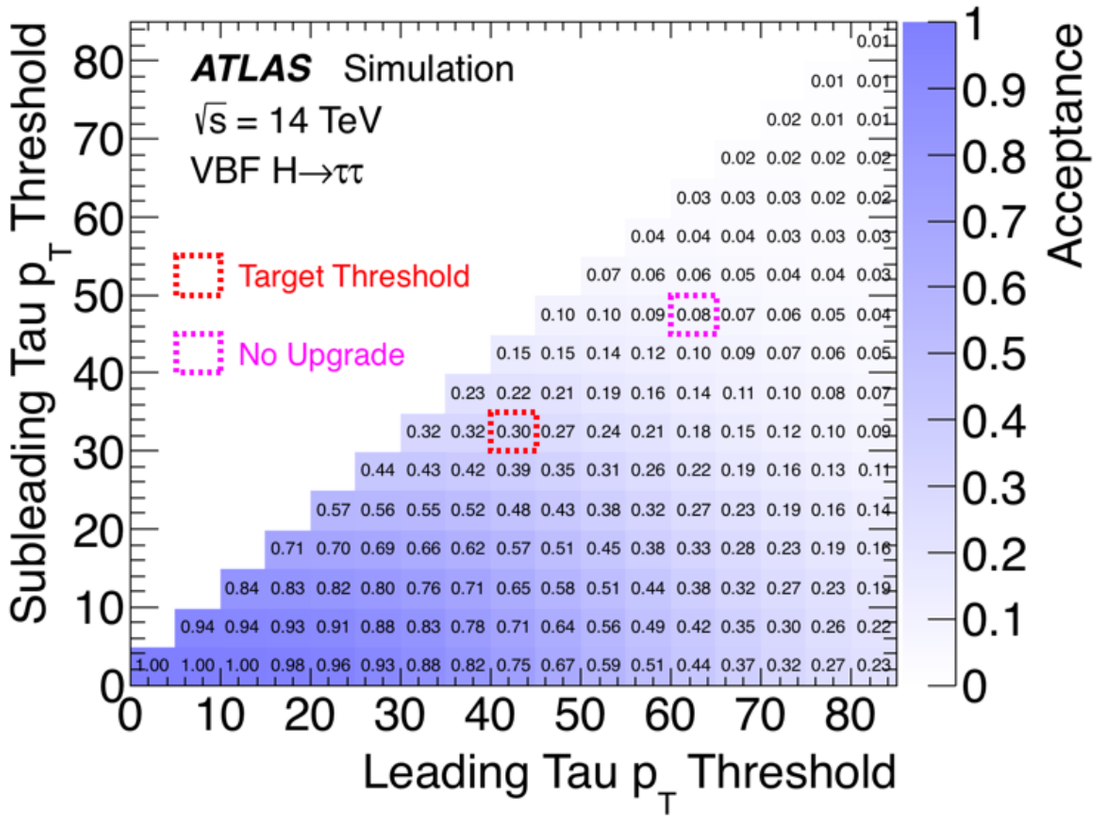
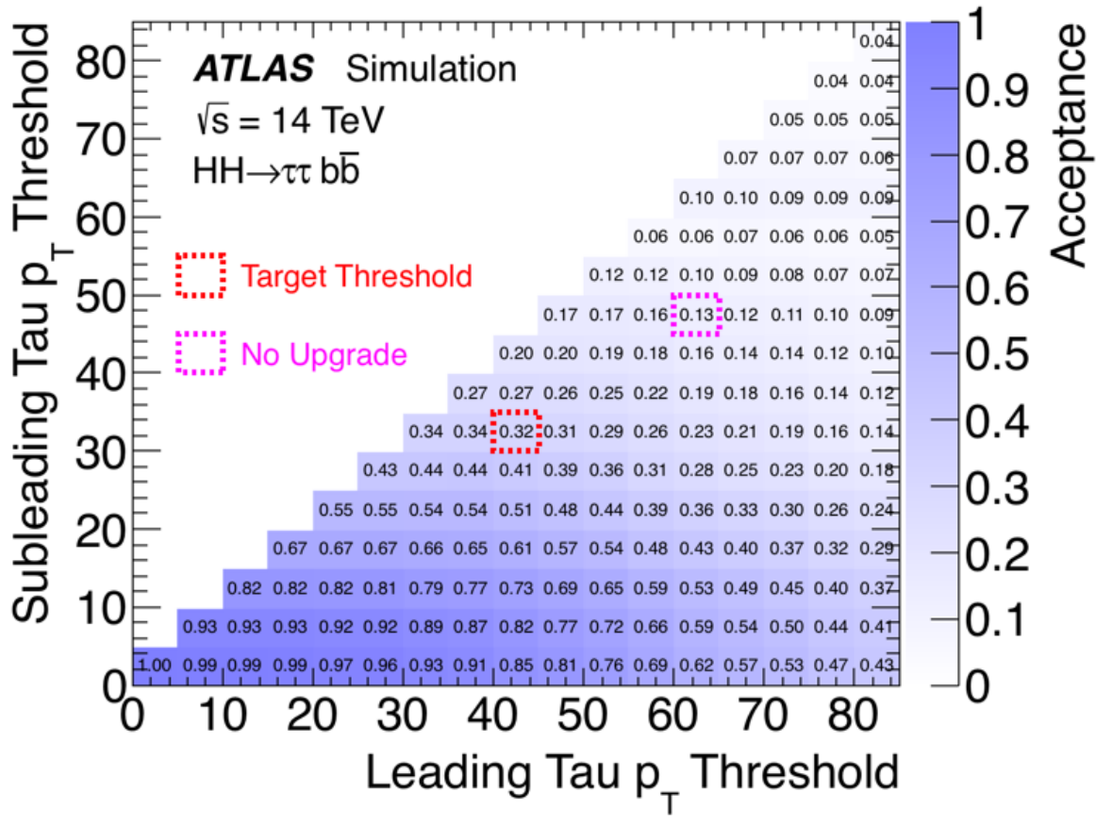


- Di-Higgs production

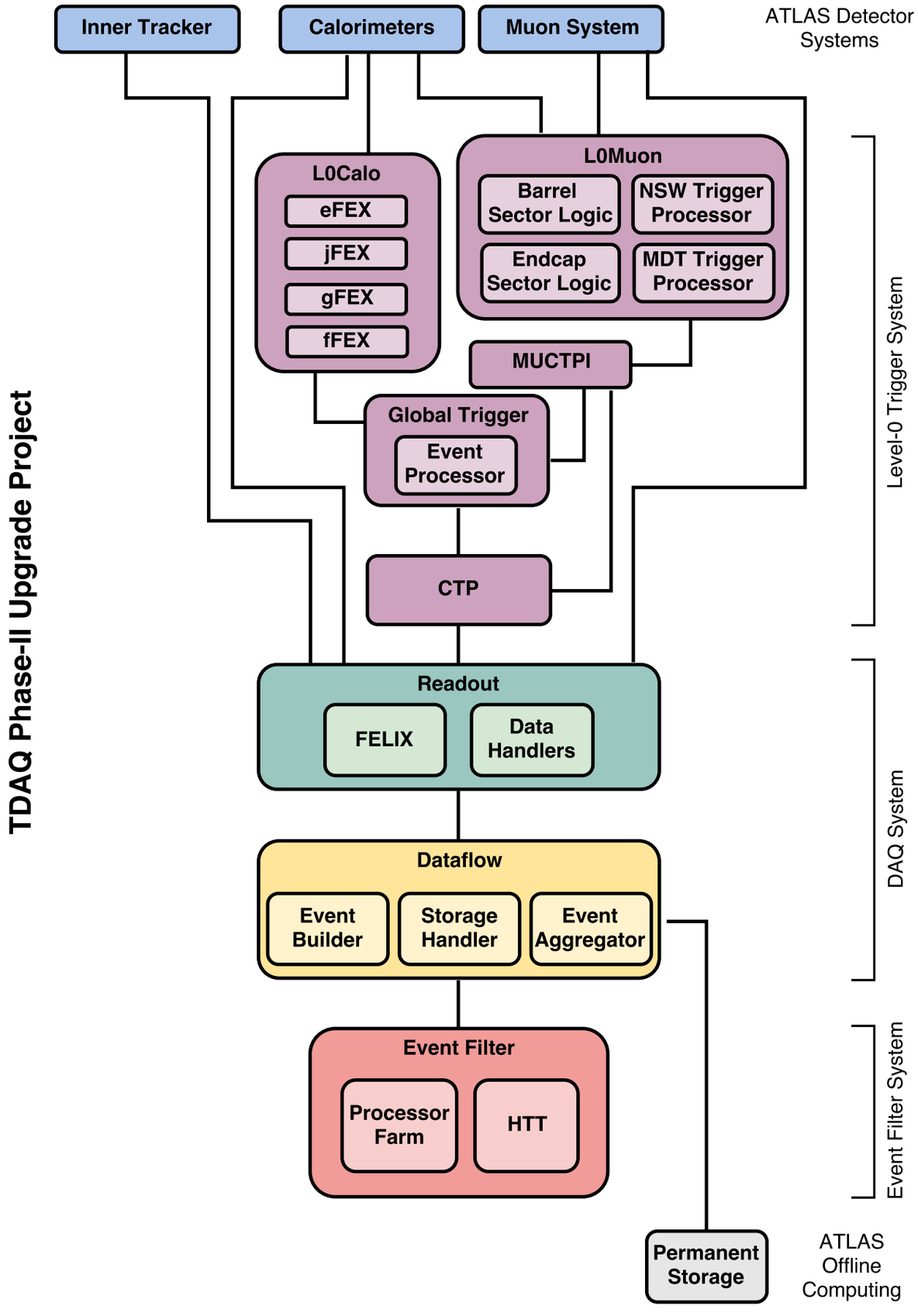


hadronically decaying taus

PHASE-II TDAQ ARCHITECTURE

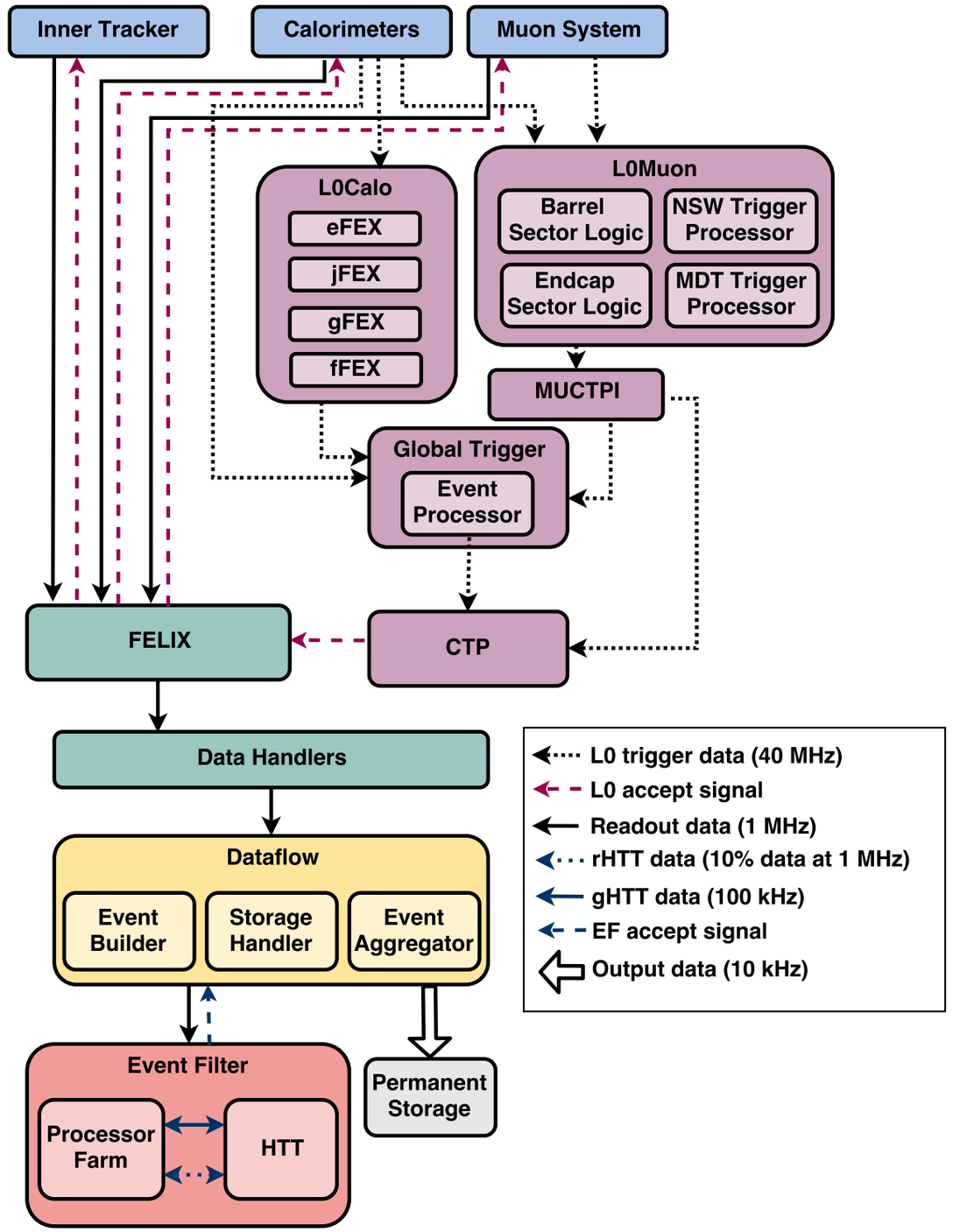
Three TDAQ Systems:

- Level-0 Trigger
- Data Acquisition
- Event Filter

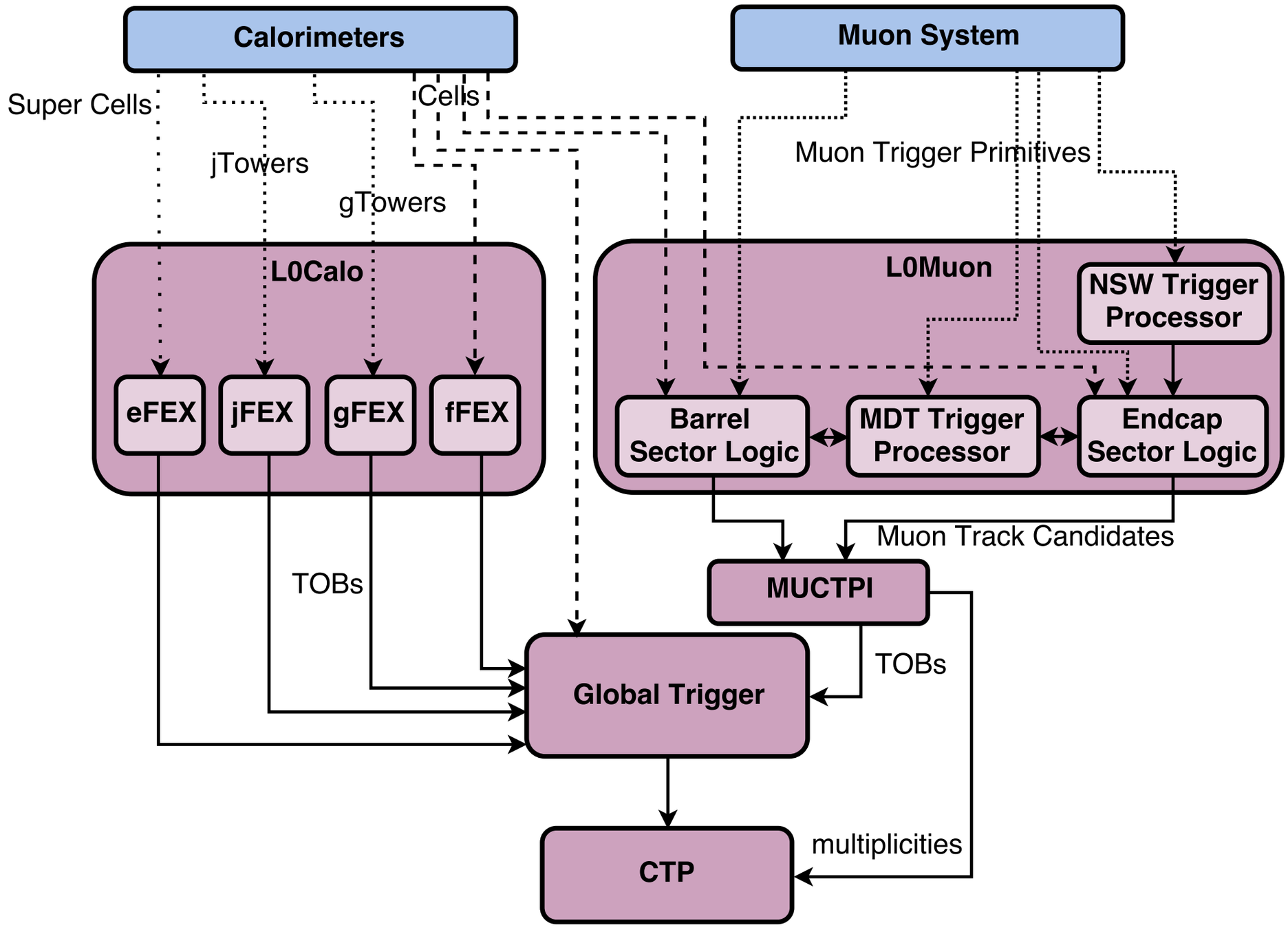


PHASE-II TDAQ DESIGN CONSIDERATIONS

- Increased Level-0 trigger rate from 100 kHz to 1 MHz; hardware-based Level-0 trigger system designed for a maximum latency of 10μs (2.5μs in Run 3)
- Data acquisition system provides common readout interface and can handle input readout bandwidth of 5.2 TB/s
- Event filter includes commodity processing farm plus regional & full-scan hardware-based tracking; max output event rate: 10 kHz



LEVEL-0 TRIGGER ARCHITECTURE



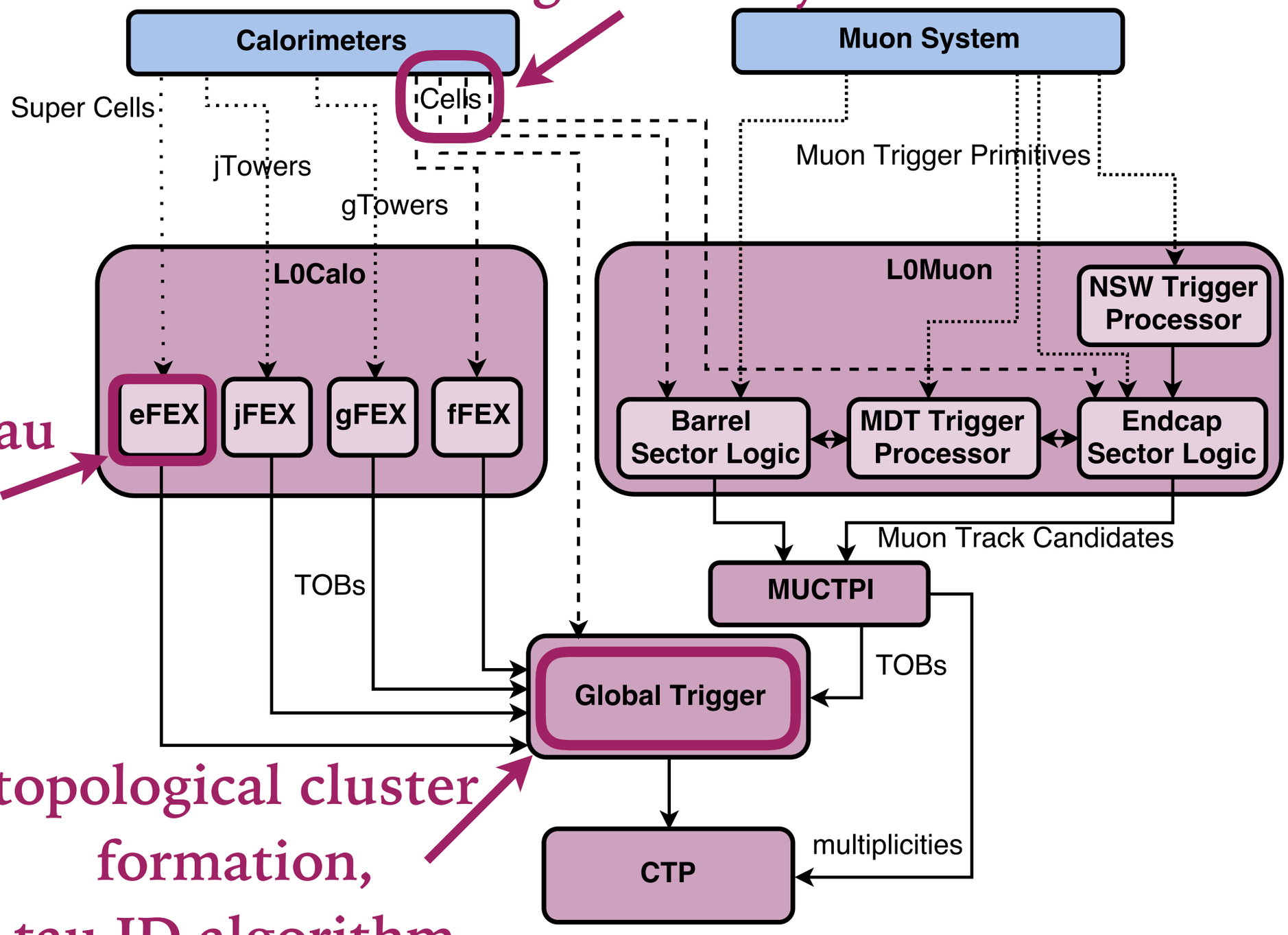
LEVEL-0 TRIGGER ARCHITECTURE

Target Level-0 di-τ rate: 200 kHz

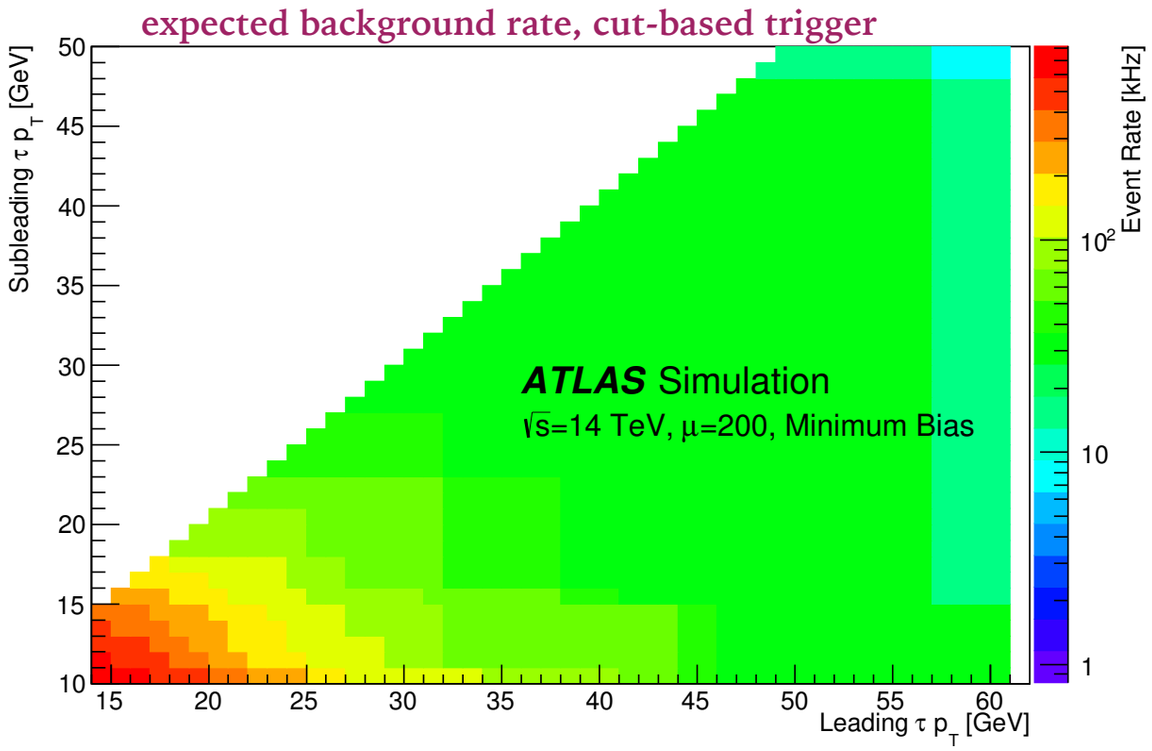
full granularity

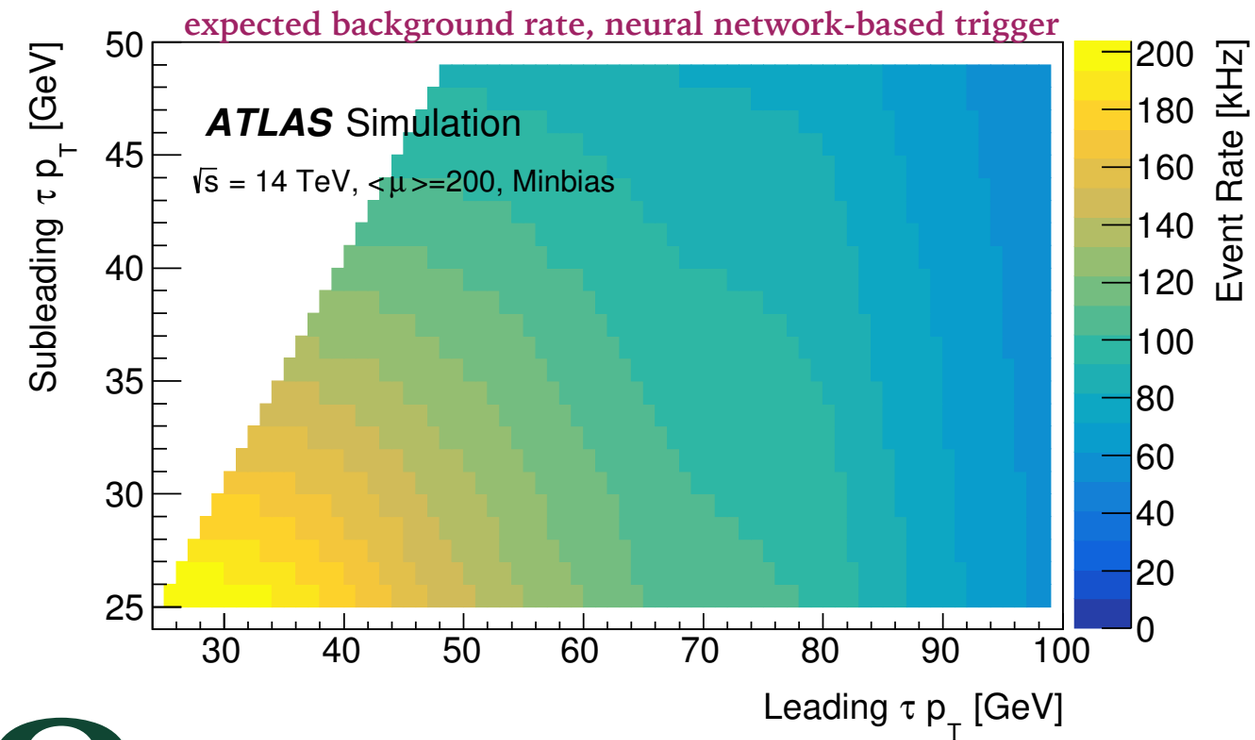
legacy hardware; electron feature extractor seeds tau candidates

topological cluster formation, tau ID algorithm



EXPECTED LEVEL-0 DI-TAU TRIGGER PERFORMANCE (1)



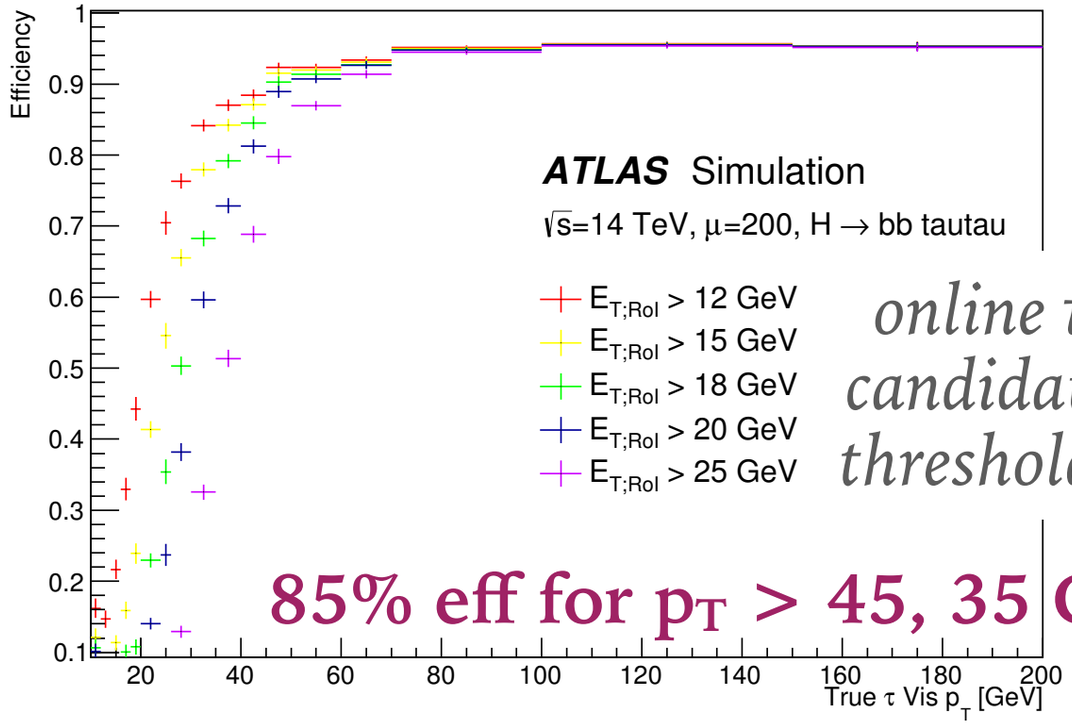


- Cut-based trigger exploiting:
  - energy in a narrow core,
  - depth profile of the energy deposition,
  - isolation requirements

- Recurrent neural network:
  - energy, depth moments of up to 6 topoclusters around seed axis
  - probability that each cluster is an EM shower

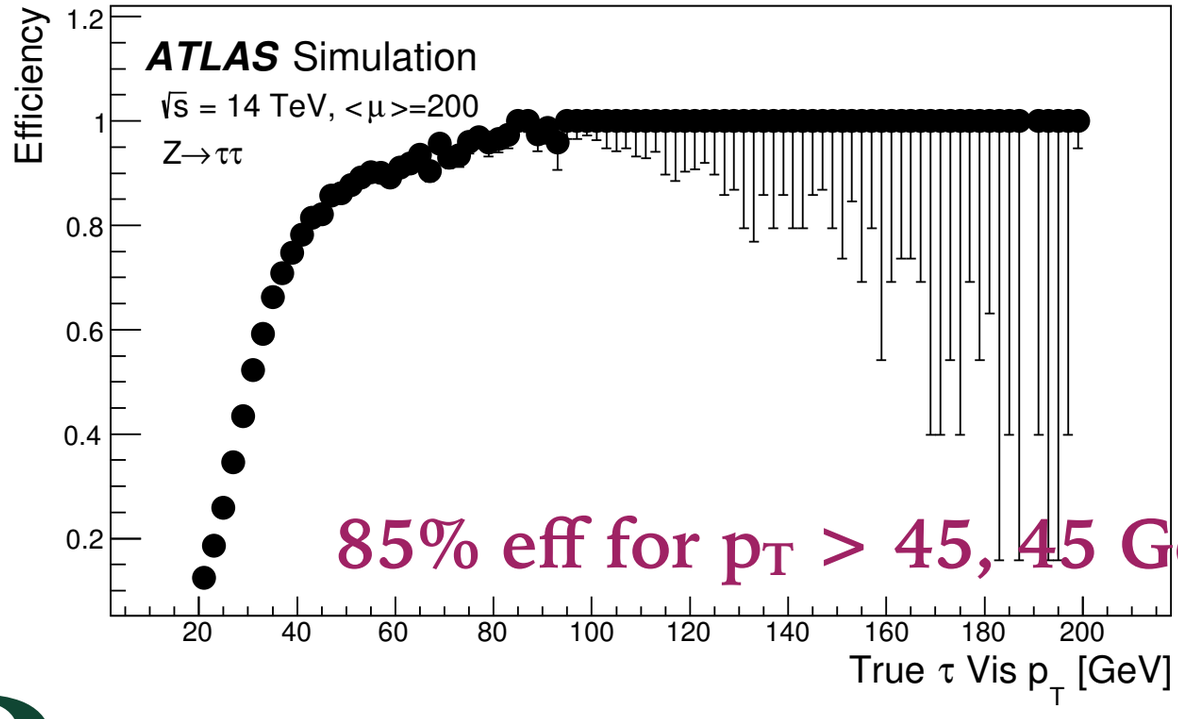
EXPECTED LEVEL-0 DI-TAU TRIGGER PERFORMANCE (2)

200 kHz di-τ trigger rate



online τ candidate thresholds

85% eff for p_T > 45, 35 GeV



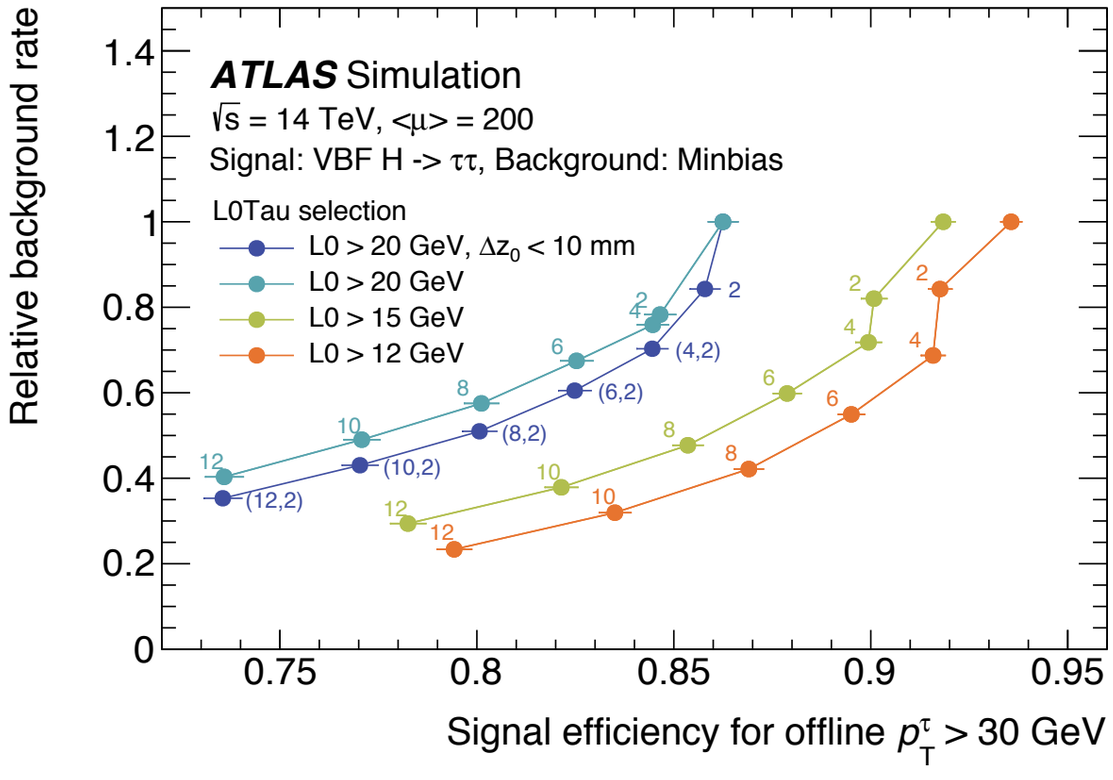
85% eff for p_T > 45, 45 GeV

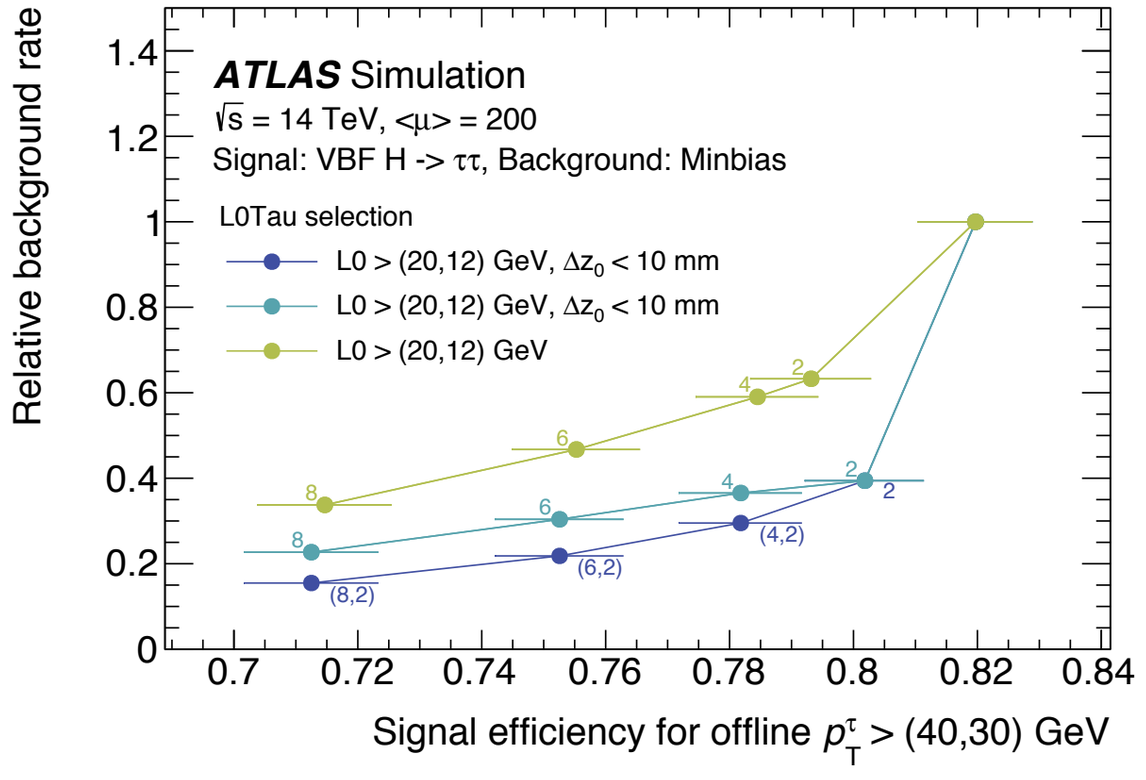
- Cut-based trigger exploiting:
  - energy in a narrow core,
  - depth profile of the energy deposition,
  - isolation requirements

- Recurrent neural network:
  - energy, depth moments of up to 6 topoclusters around seed axis
  - probability that each cluster is an EM shower

EVENT FILTER REJECTION

Regional tracking: 1-5 tracks with p_T > 2 GeV within ΔR < 0.2



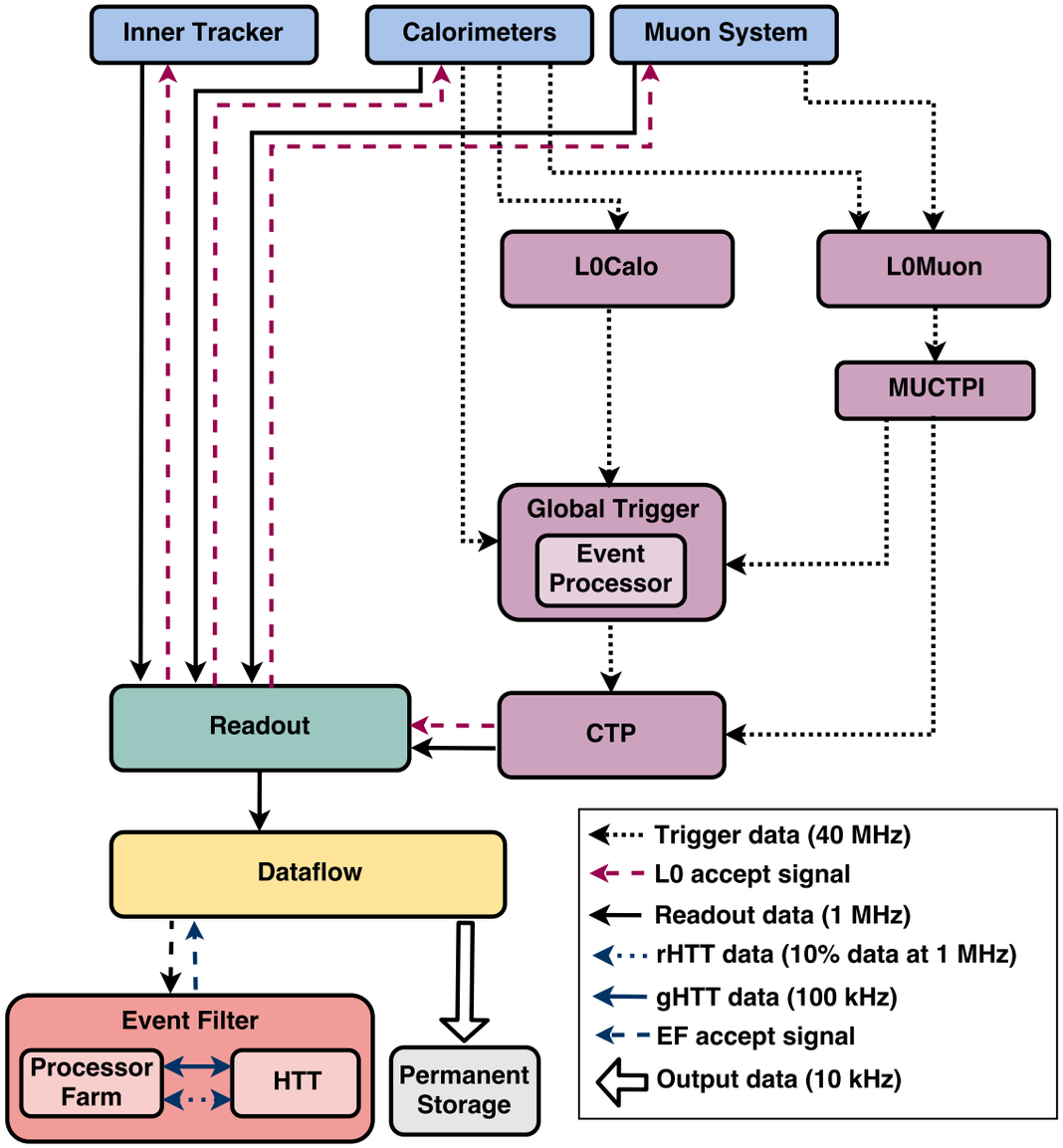


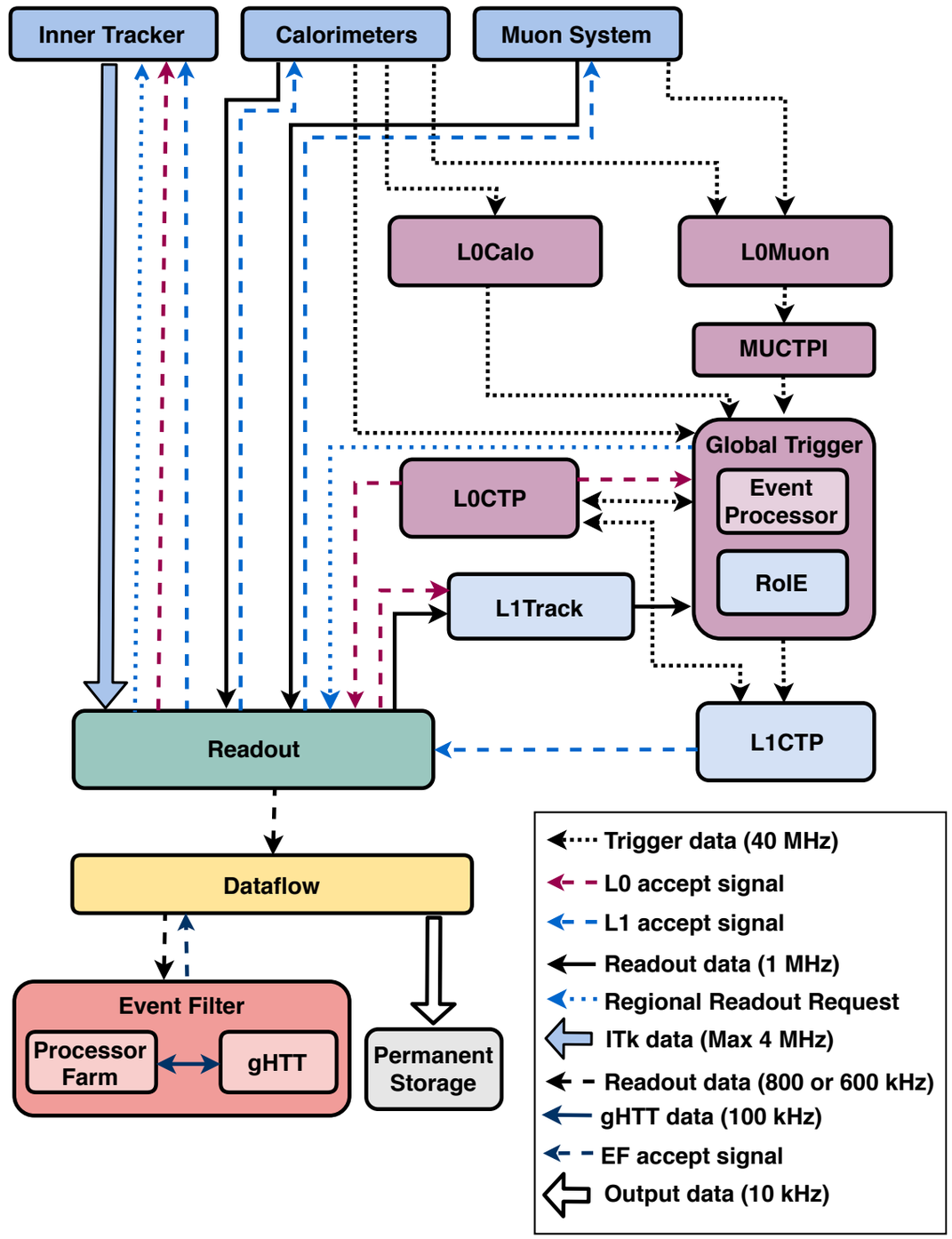
Full-scan tracking: tracks down to 1 GeV used for identification and isolation

Additional requirements needed:
e.g., ΔR(τ,τ) < 3 vetoes back-to-back dijet events

DI-TAU OPPORTUNITIES WITH SPLIT-LEVEL ARCHITECTURE

potential architecture evolution





DI-TAU OPPORTUNITIES WITH SPLIT-LEVEL ARCHITECTURE

Signature	Single-Level Scheme Threshold	Dual-Level Scheme Threshold	Level-0 (kHz)	Level-1 (kHz)	EF before analysis specific cuts (kHz)	Gain
di-τ	40, 30 GeV	30, 20 GeV	800	80	2.2	increased acceptance from 30% to 55% for VBF $H \rightarrow \tau\tau$ and 32% to 54% for $HH \rightarrow bb\tau\tau$

SUMMARY

- The ATLAS Phase-II TDAQ Architecture enables **triggering on hadronic taus** to support the physics program at the HL-LHC

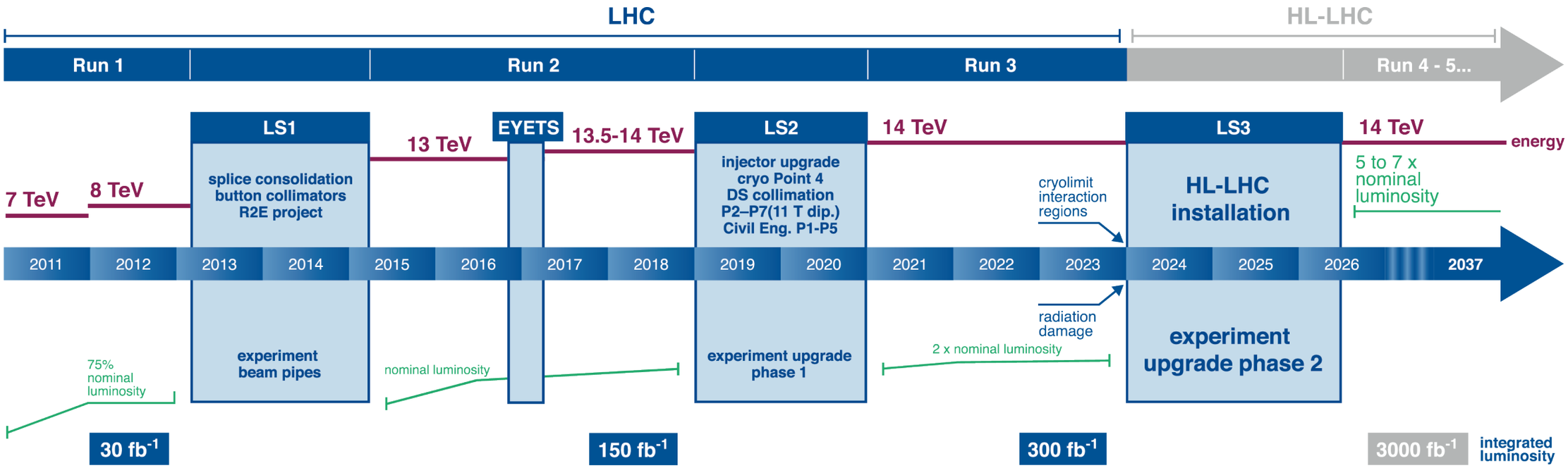
Trigger	Offline Threshold [GeV]	Rate
Level-0 Single Tau	150	3 kHz
No regional tracking cuts	-	-
Event Filter Isolated Single Tau	150	0.35 kHz
Level-0 Di-τ	40,30	200 kHz
After regional tracking cuts	40,30	40 kHz
Event Filter Isolated Di-τ	40,30	1.6 kHz
Event Filter Isolated Di-τ with $0.3 < \Delta R < 3$	40,30	0.5 kHz

- Additional $H \rightarrow \tau\tau$ and $HH \rightarrow bb\,\tau\tau$ signal acceptance can be achieved with the potential evolution to a split-level architecture
- Details available in the TDAQ Phase-II Technical Design Report: CERN-LHCC-2017-020; ATLAS-TDR-029

ADDITIONAL MATERIAL

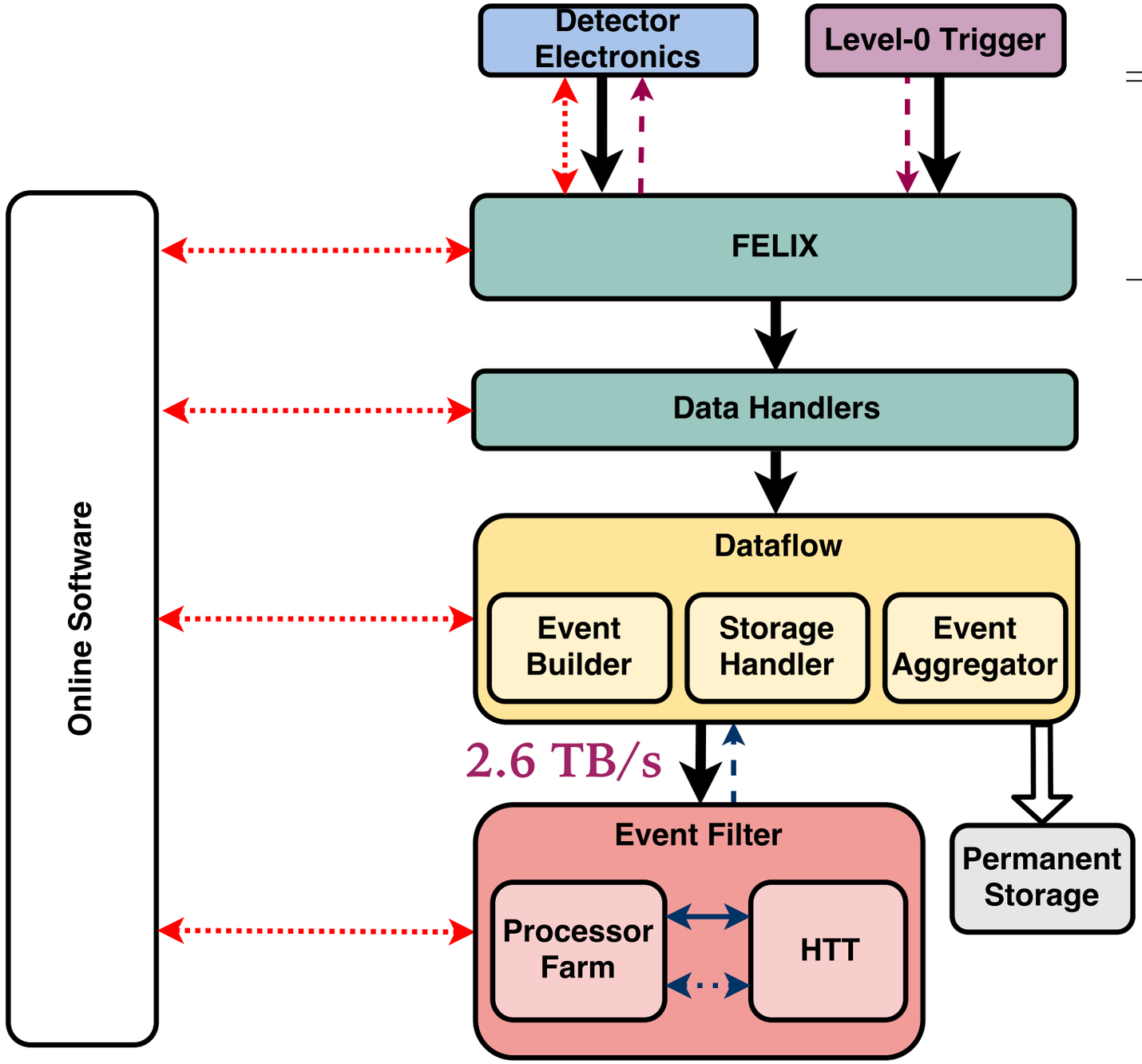
HL-LHC: SCHEDULE

LHC / HL-LHC Plan



- LHC reached its design luminosity in 2016: 1 x 10^{34} cm^{-2} s^{-1}
  Run 2 peak luminosity: >2 x 10^{34} cm^{-2} s^{-1}, **over 60 interactions/crossing**
- Goals for HL-LHC: $\sqrt{s}$ = 14 TeV,
  ultimate luminosity: 7.5 x 10^{34} cm^{-2} s^{-1}, **200 interactions/crossing**,

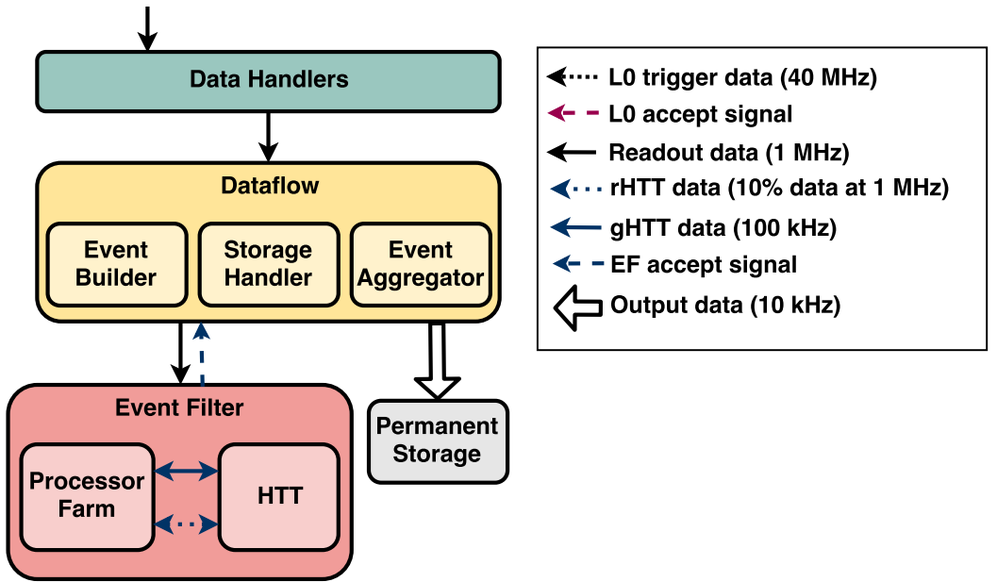
DATA ACQUISITION SYSTEM



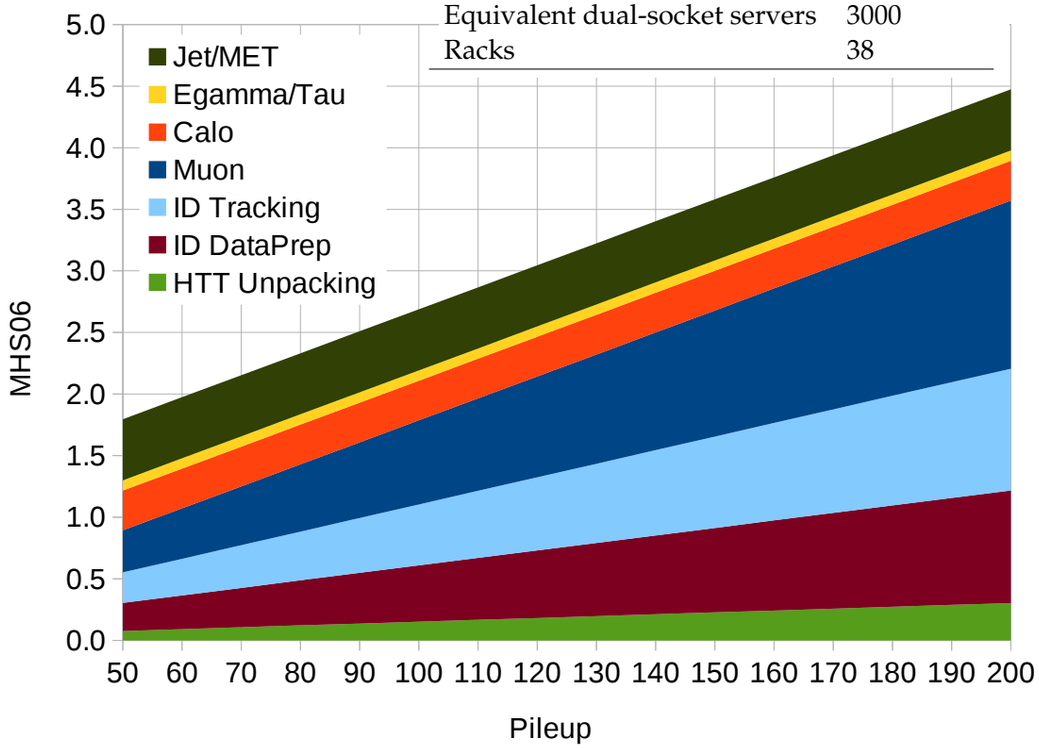
Component	Total Number
Total links from detectors	17093
FELIX I/O card	545
FELIX servers	279
Data Handler PCs	545

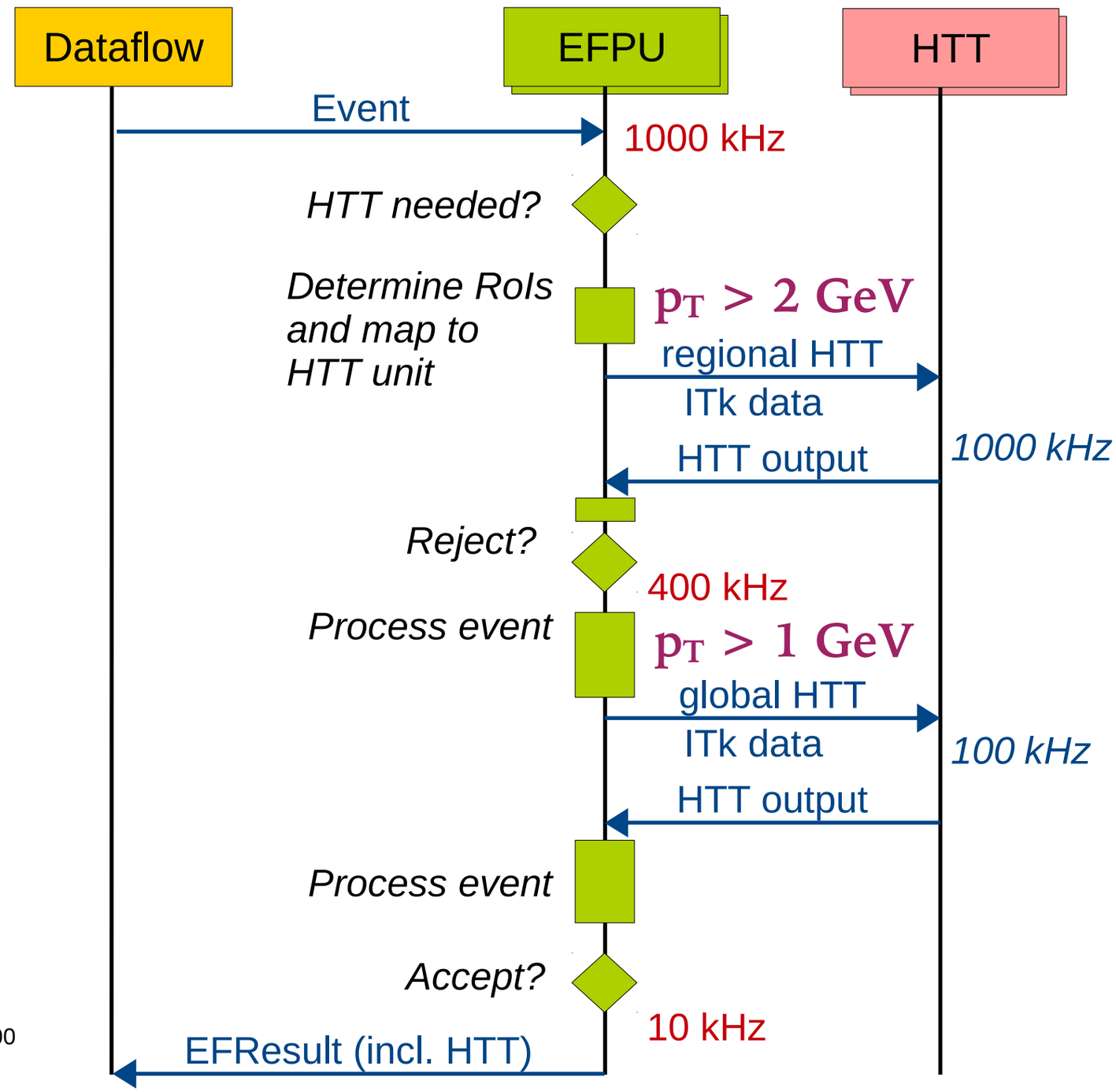
- Storage capacity: 36 PB

EVENT FILTER



Compute capacity required	4.5 MHS06
Equivalent dual-socket servers	3000
Racks	38





TRACKING ARCHITECTURE CONSIDERATIONS

- Several technologies considered for tracking

  i. hardware-based tracking (HTT) based on FPGAs and custom-designed Associative Memory ASICs **[baseline]**

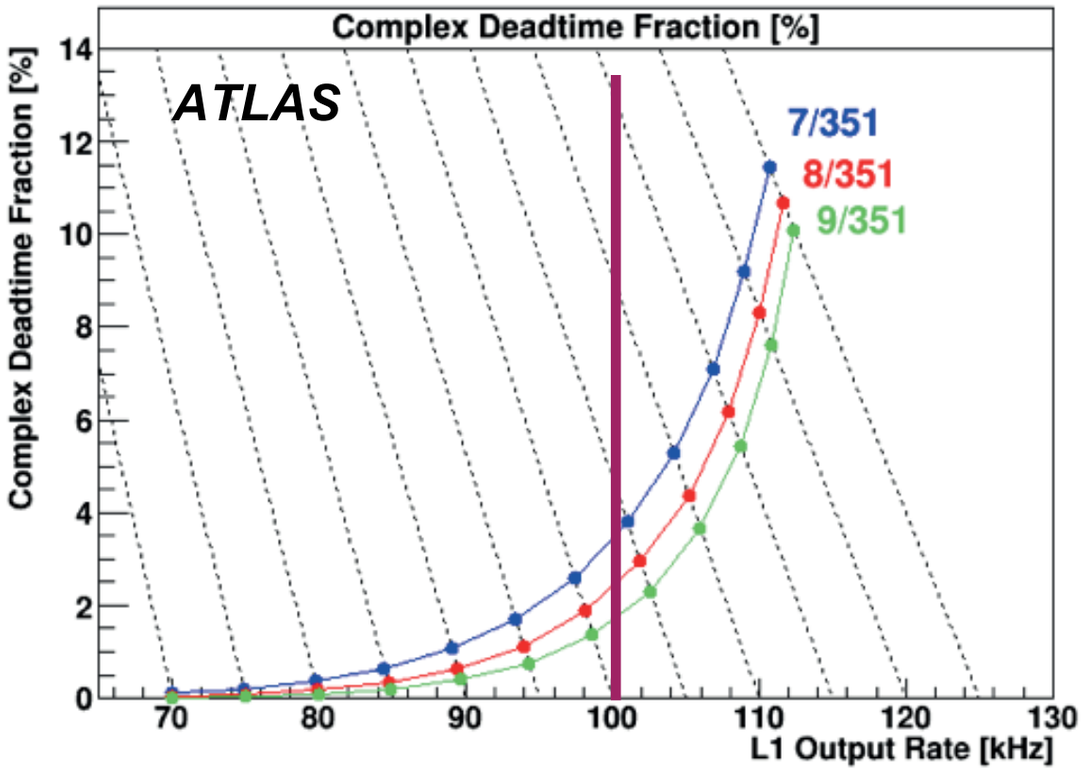
  ii. commodity CPU-based servers
  [13.4 MHS06 (regional) + 27 MHS06 (full-scan) computing power would be needed]

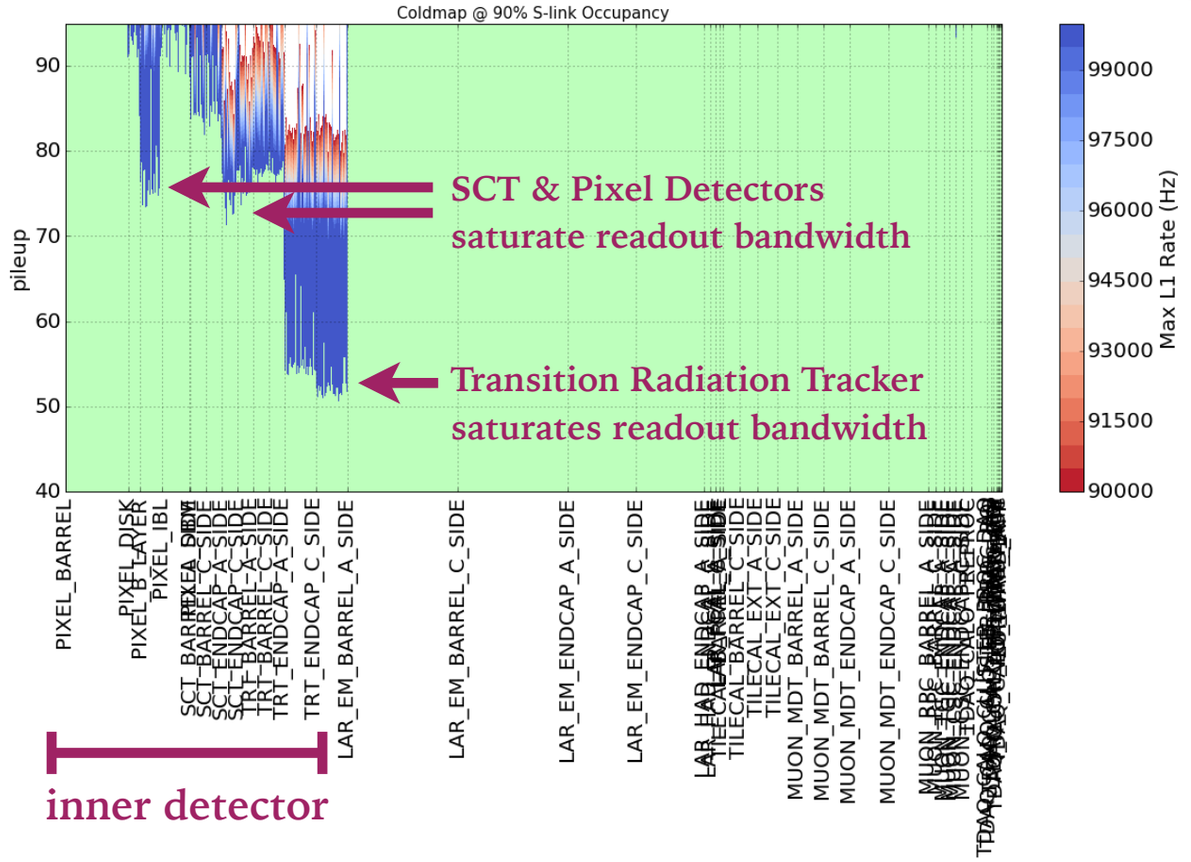
  iii. systems based on accelerators (e.g., general purpose GPUs)
  [currently under study]

  iv. future architectures based on devices integrating machine learning capabilities

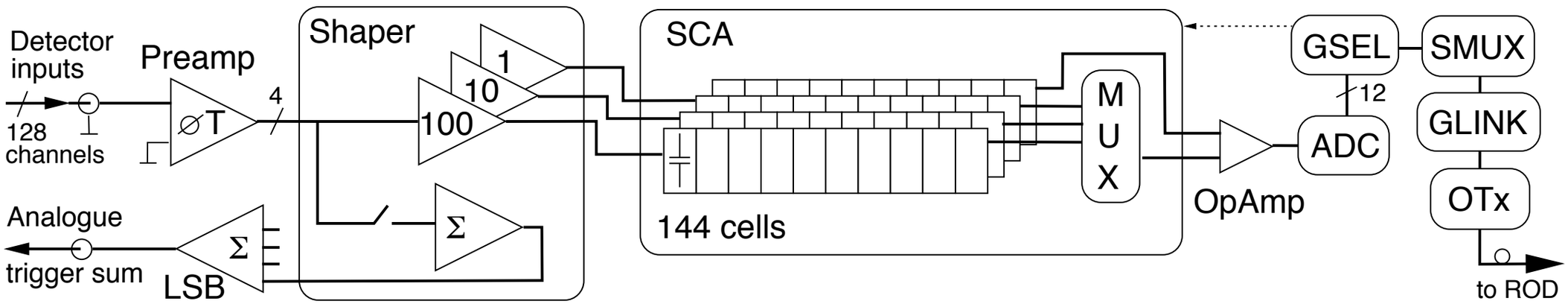
- Decision point to confirm or change baseline:
system-wide Preliminary Design Review (April 2019)

CHALLENGES & LIMITATIONS OF THE RUN 3 TDAQ SYSTEM





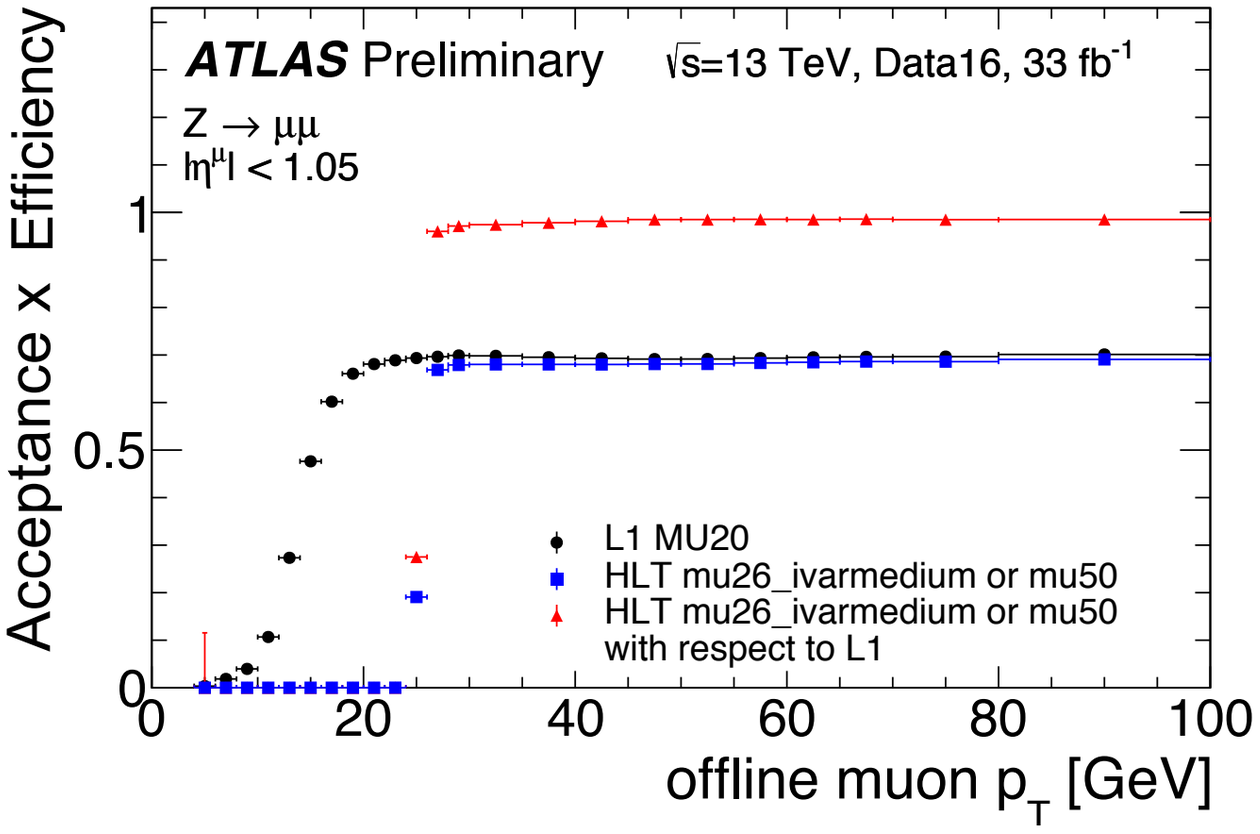
Example: LAr Calorimeter front-end electronics



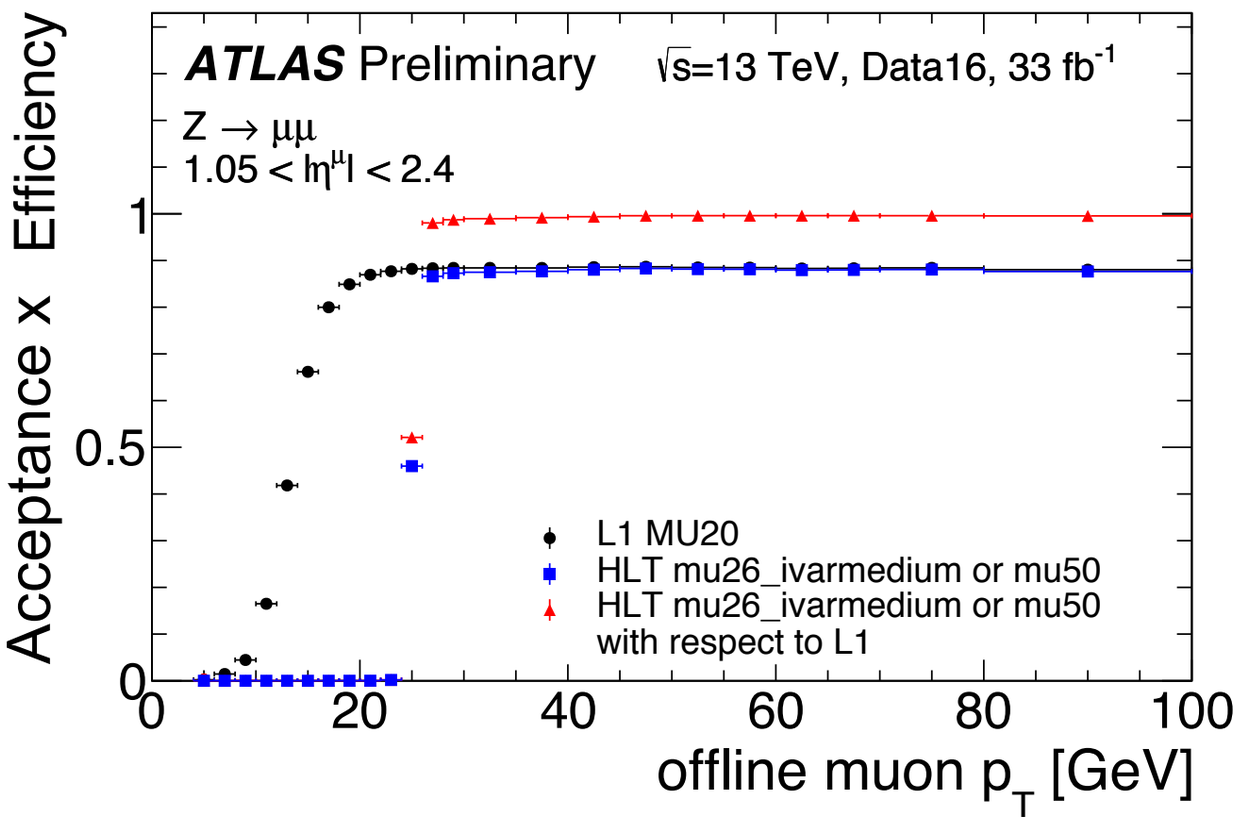
Switched Capacitor Array limit: 144/40MHz = 3.6μs

CHALLENGES & LIMITATIONS OF THE RUN 3 TDAQ SYSTEM

muon barrel, Run 2



muon endcap, Run 2



- Original Resistive Plate Chamber and Thin Gap Chamber electronics cannot cope with latencies & rates
- Latency prevents inclusion of precision p_T from Monitored Drift Tubes
- Muon trigger logic requires coincidence in all three chambers

CHALLENGES & LIMITATIONS OF THE RUN 3 TDAQ SYSTEM

- HL-LHC pileup conditions (<μ>=200) indicate **x10 increase in trigger rate** compared to Run 3
- **Maximum Level-1 trigger rate: 100 kHz, Maximum latency: 2.5 μs**

Expected Fast TracKer (FTK) performance

Parameter	$\mu = 80$	$\mu = 200$	
Max. Processing Rate [kHz]	100	5	100
Efficiency (for tracks with $p_{\mathrm{T}} > 1\,\mathrm{GeV}$)	∼90%	∼90%	∼60%

- Hardware-based **tracking cannot maintain high efficiency**

LEVEL-0 TRIGGER ARCHITECTURE: SYSTEM SIZE

Subsystem	Component	Module	Phase-I deliverable	Number of Boards	Input links per board	Output links per board
L0Calo	eFEX	-	Yes	24	144	48
	jFEX	-	Yes	6	240	48
	gFEX	-	Yes	1	312	108
	fFEX	-	-	2	240	48
L0Muon	NSW	-	-	16	148	28
	Endcap SL	SL	-	48	96	60
	Barrel SL	SL	-	32	60	60
	MDT	-	-	64	72	72
Global Trigger	MUX	GCM	-	23	156	108
	GEP	GCM	-	24	108	36
	CTP Interface	GCM	-	1	60	24
MUCTPI	-	-	Yes	2	208	65
CTP	CTPMI	-	-	1	-	-
	CTPIN	-	-	1-2	24	12
	CTPCORE	-	-	1	24	60
	LTI	-	-	36	1	8

HARDWARE-BASED TRACKING FOR THE TRIGGER (HTT)

- 24 HTTIFs, 96 HTT units
- 6 AMTP + 1 SSTP / unit
- 300 W estimated / Trigger Processor

AMTP: Associative Memory Tracking Processor

SSTP: Second-Stage Tracking Processor