Upgrade of the ATLAS Muon System for High-Luminosity LHC

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on behalf of the ATLAS Muon Collaboration

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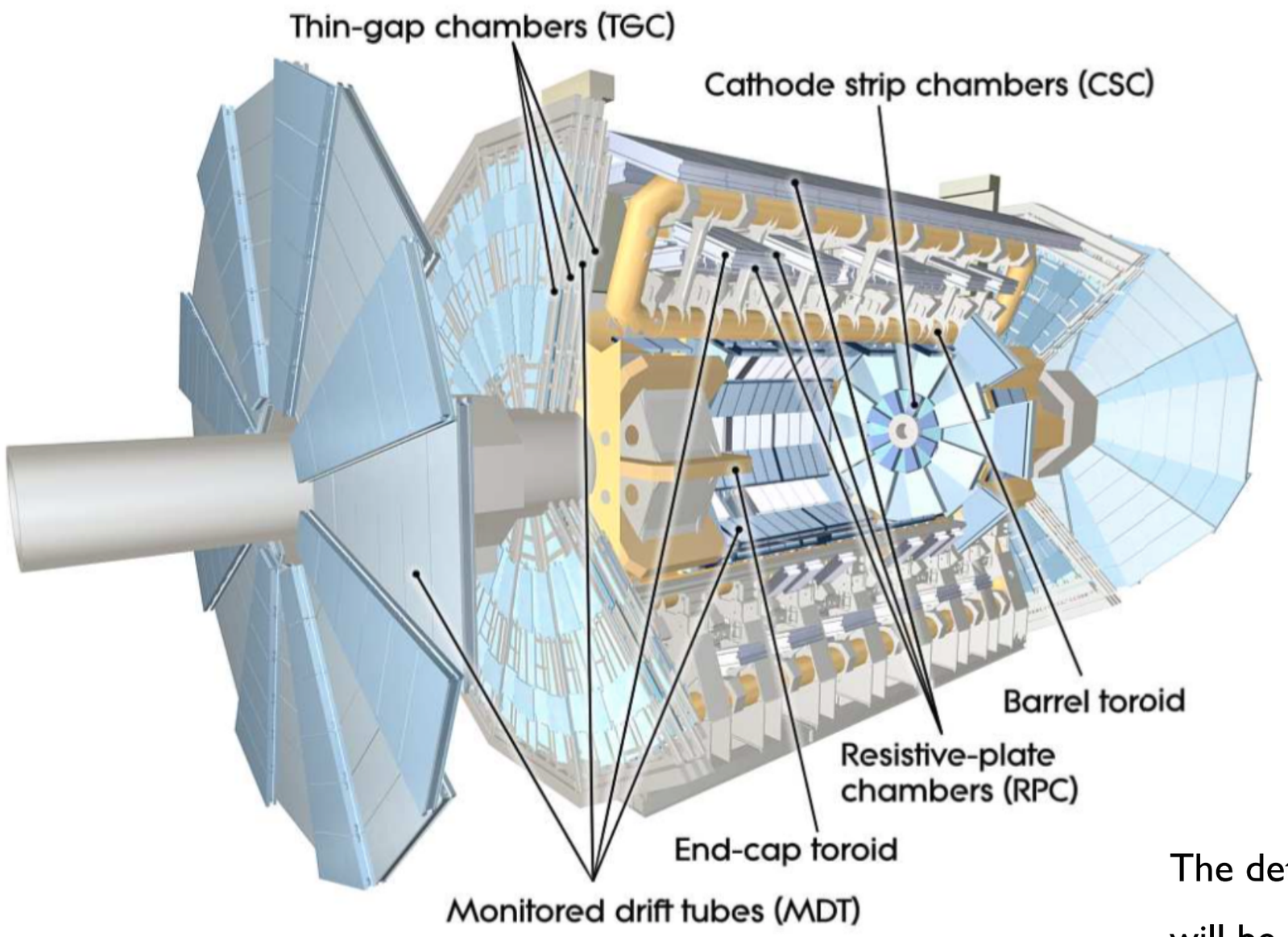
ATLAS Muon System Overview



MDT

- Precision tracking
- $|\eta| < 2.7$ (inner layer: $|\eta| < 2.0$)

CSC

- Precision tracking
- $2.0 < |\eta| < 2.7$ (only inner layer)

RPC

- Triggering, second coordinate
- $|\eta| < 1.05$

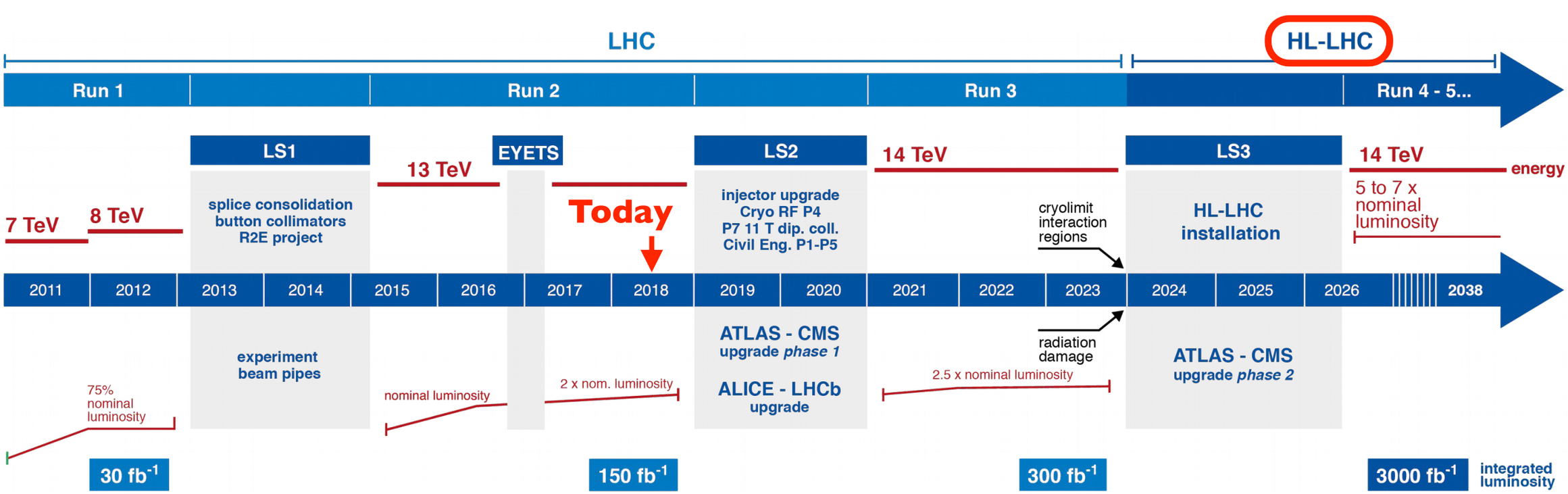
TGC

- Triggering, second coordinate
- $1.05 < |\eta| < 2.7$ (2.4 for triggering)

The detectors of the inner layer in $1.3 < |\eta| < 2.7$ will be replaced by **New Small Wheel (NSW)**, which consists of micro-mesh gaseous detectors and small-strip TGCs, in 2019-2020.

High-Luminosity LHC (HL-LHC)

- Aim for **SM precision studies** and **BSM searches** at $\sqrt{s}$ **= 13-14 TeV** with
  - peak instantaneous luminosity of **5 x 10^{34} $cm^{-2}s^{-1}$** (ultimate: **7.5 x 10^{34} $cm^{-2}s^{-1}$**),
  - total integrated luminosity of **3000 fb^{-1}** (ultimate: **4000 fb^{-1}**).
- **ATLAS Phase II upgrade** in 2024-2026, followed by HL-LHC Runs 4, 5, …



TDR for Muon System Phase II Upgrade

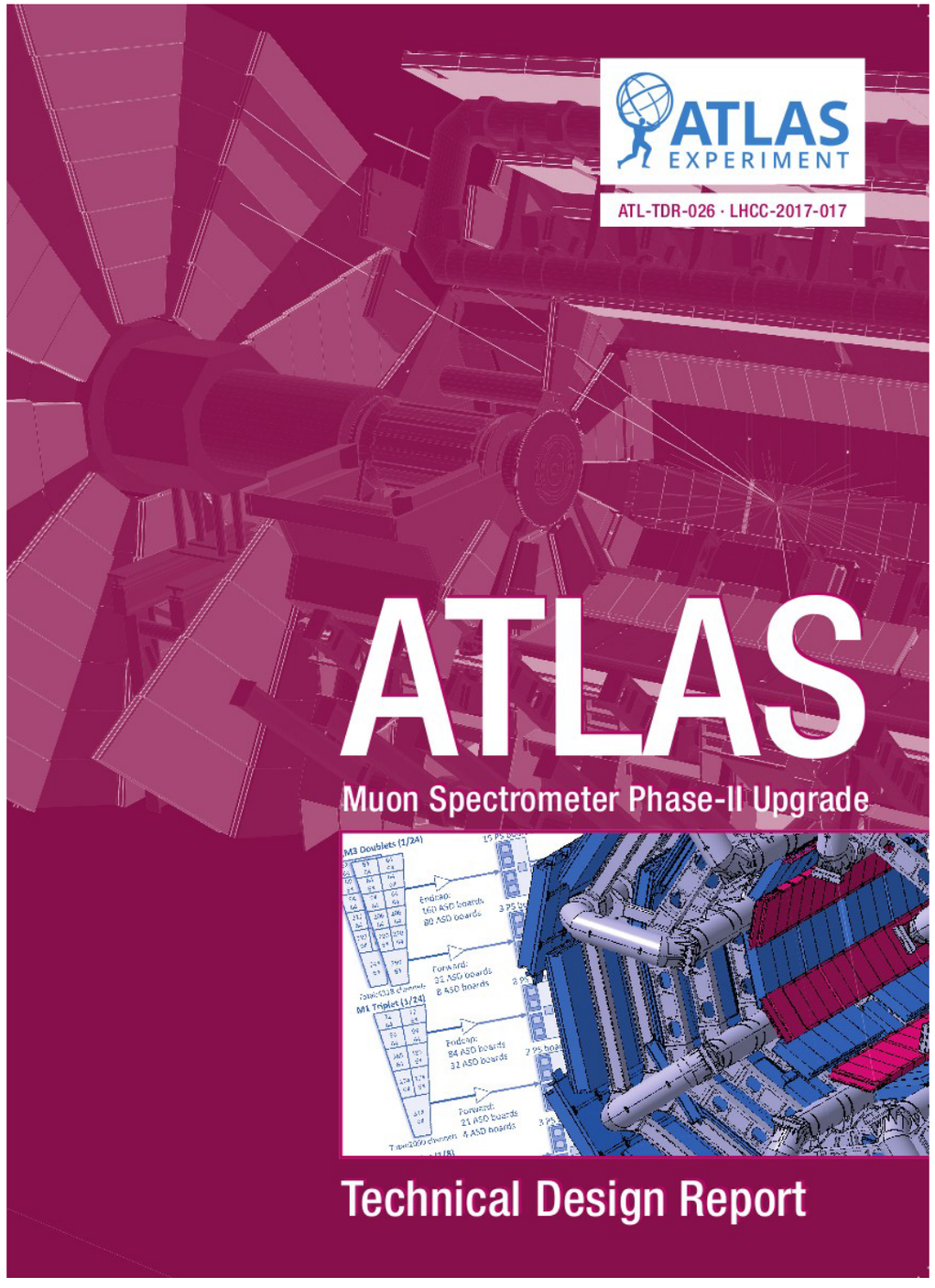
Technical Design Report (TDR)

for the Phase II upgrade of the muon system

has been published in Dec. 2017.

Currently we are at a **'post-TDR' phase**

of **designing and prototyping**.

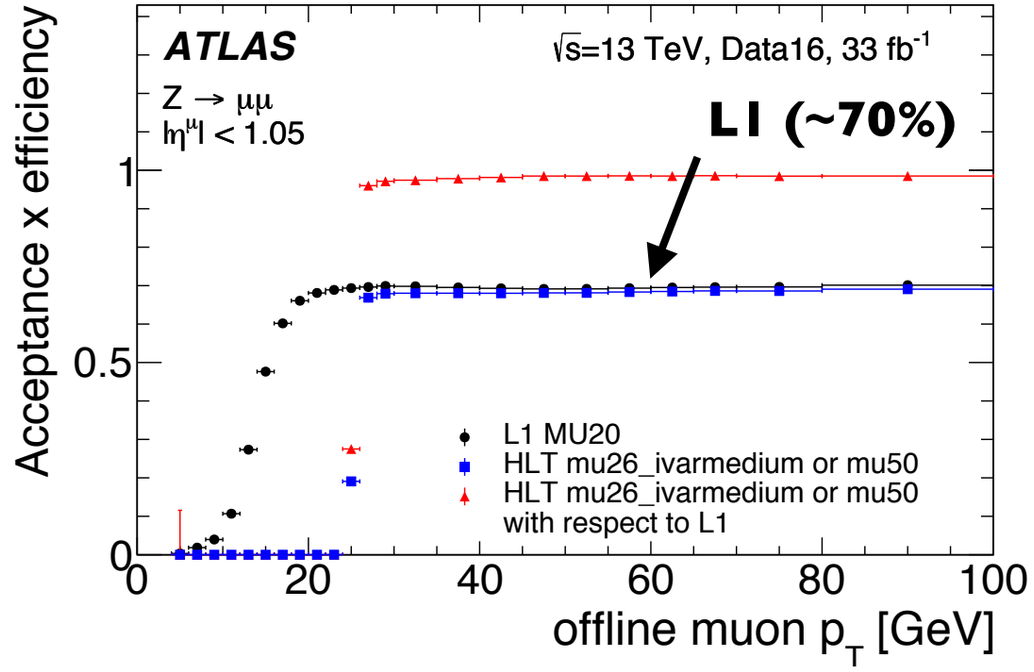


http://cds.cern.ch/record/2285580

Requirements for the Muon System at HL-LHC

Trigger Chamber

To improve the product of the trigger acceptance and the efficiency in the barrel, the coverage of trigger chambers (RPCs) should be extended.

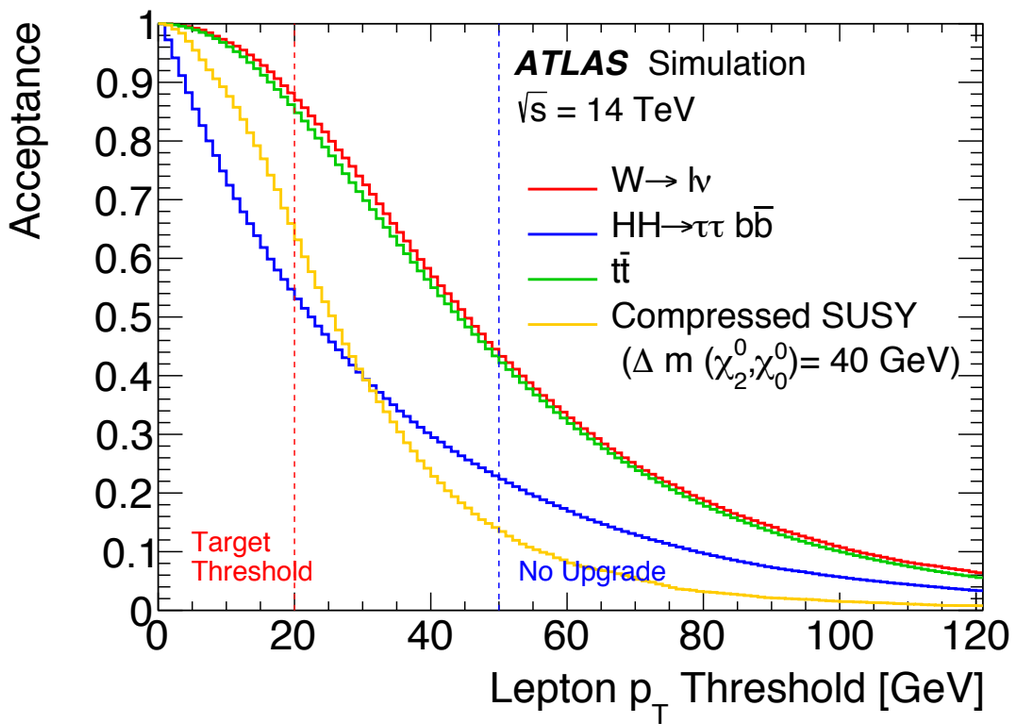


Trigger and Readout Electronics

To keep the trigger p_T thresholds, the electronics should be upgraded for extended L0 trigger latency (10 μs) and rate (1 MHz).

First trigger level: renamed L1 → L0

Option to evolve to L0/L1 scheme, max 4 MHz/800 kHz and 10/35 μs



Overview of the Muon System Phase II Upgrade

Chambers

- Add new RPC in the inner barrel layer to extend the coverage of the trigger.

  Replace MDT chambers with small-diameter MDT (sMDT) chambers to provide space.

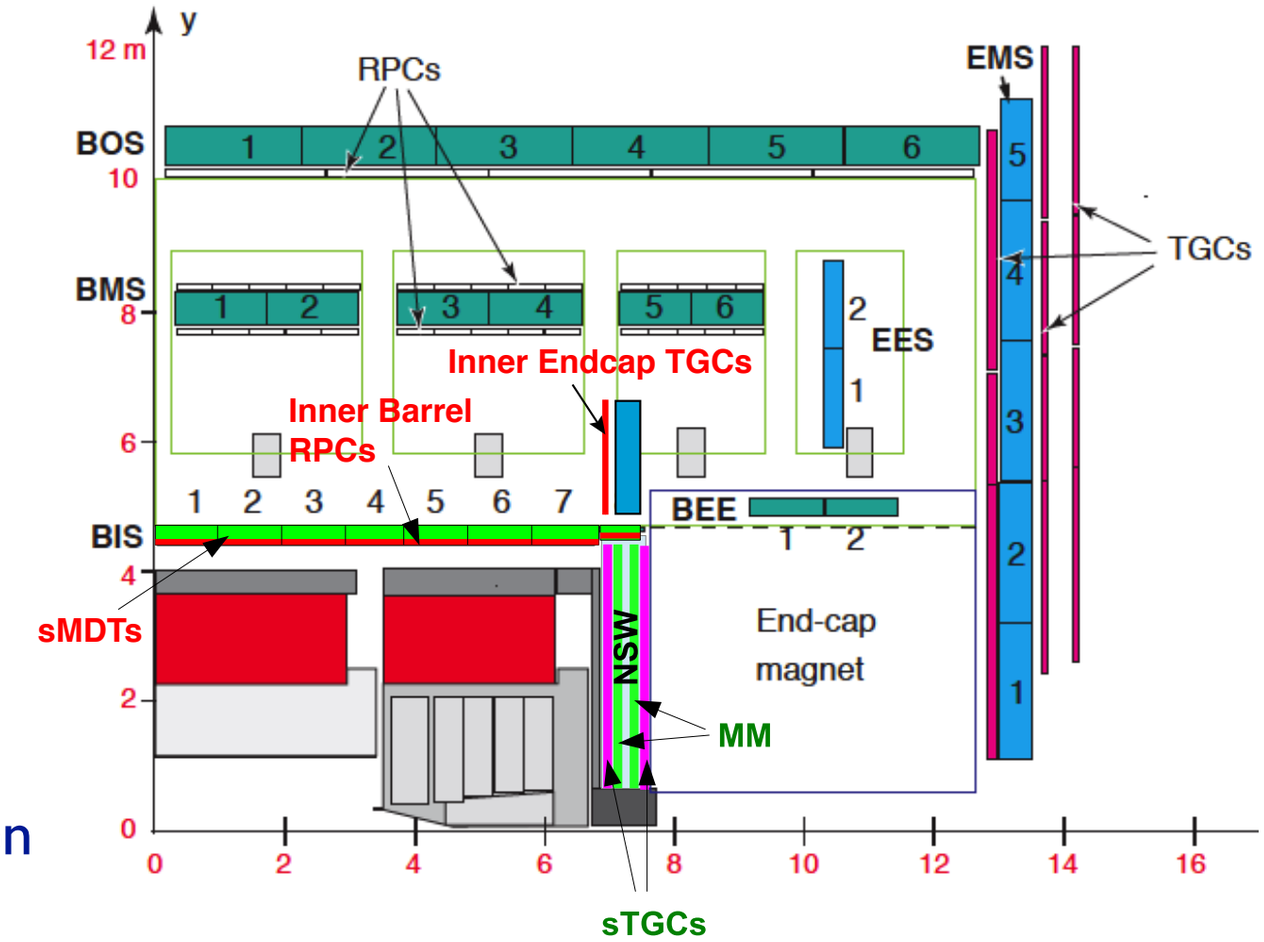
- Replace TGC in the inner endcap layer (1.05<|η|<1.3) to improve the trigger redundancy.

Electronics

- Replace trigger and readout electronics (RPC, TGC, and MDT) to extend the first-level trigger latency and rate.
- Include MDT in the first-level trigger for an improved selectivity.

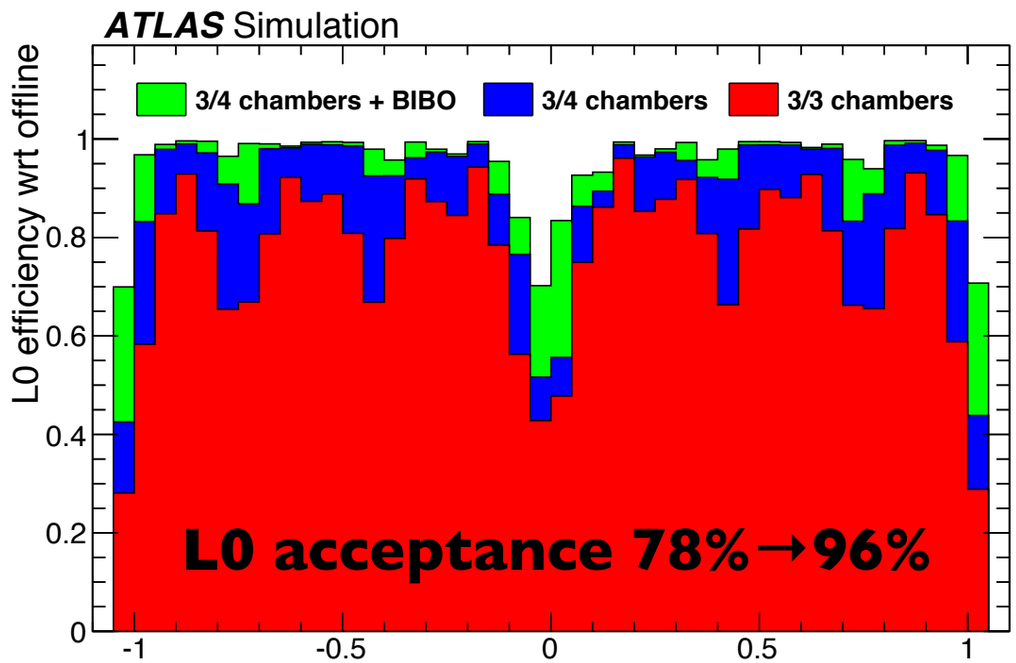
Power System

- Replace the power system due to radiation limitation and general obsolescence.



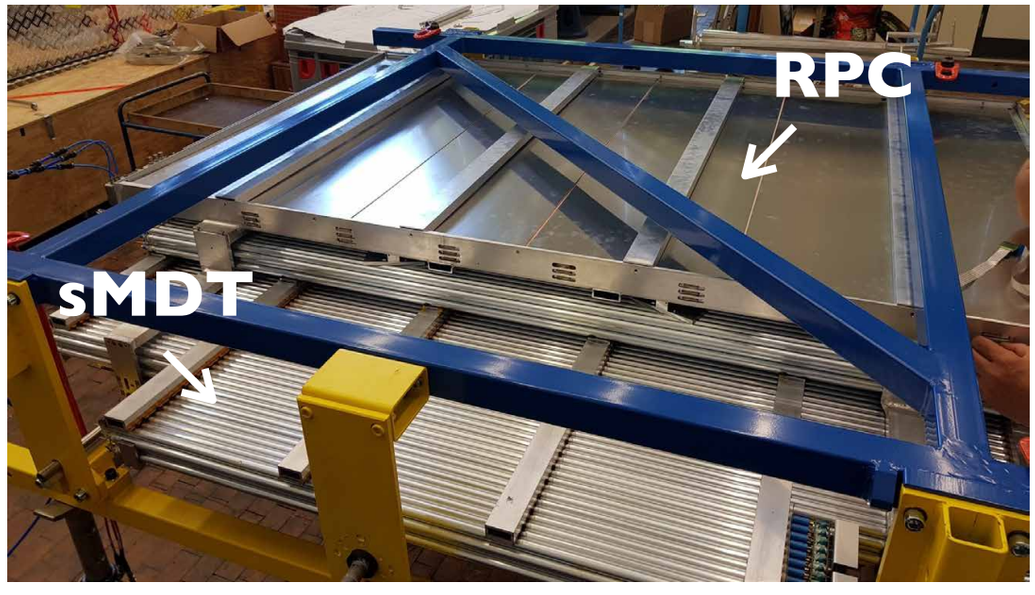
MDT/RPC Upgrade in the Inner Barrel

To extend the coverage and the redundancy of L0 trigger, **new RPC triplet chambers** (1 mm gas gap instead of 2 mm, high-sensitivity electronics, rate capability of order 10 kHz/cm^2) will be installed in the inner barrel layer.



The available space in the inner barrel is limited and about half of the MDT chambers (⌀=30 mm) will be replaced by **sMDT chambers** (⌀=15 mm).

The replacement of outermost (the highest |η|) chambers ('BIS78') is foreseen already for 2019-2020. **The chamber production** has been started.



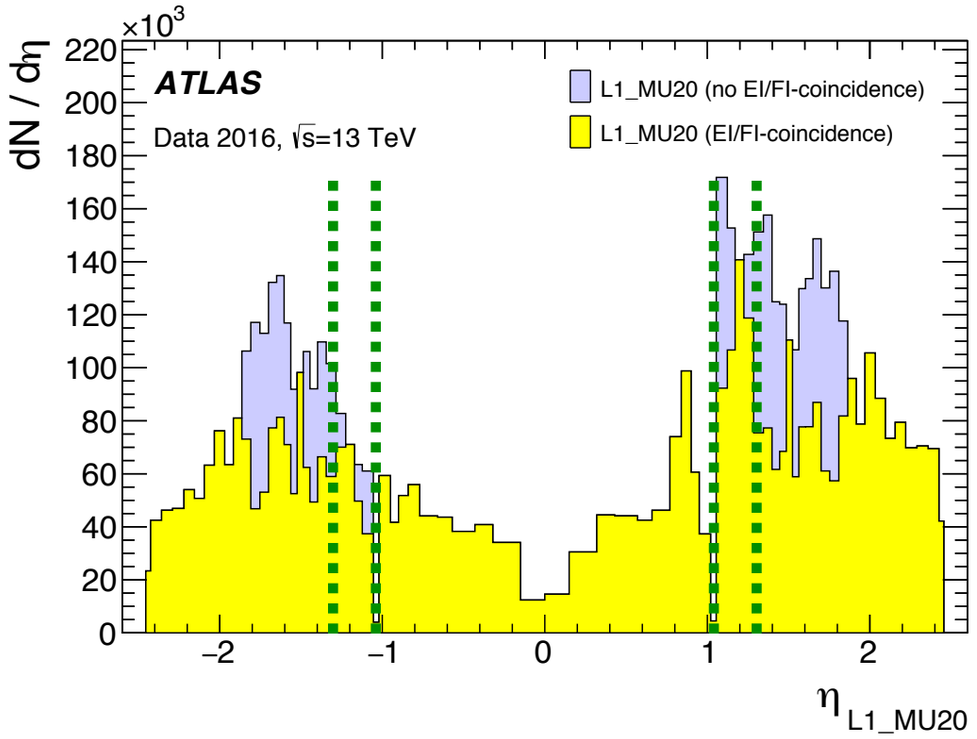
TGC Upgrade in the Inner Endcap

TGCs in the inner endcap (1.05 < |η| < 1.3): doublet chambers originally not foreseen to be used in trigger, but included to reduce the rate of triggers due to charged particles not from IP.

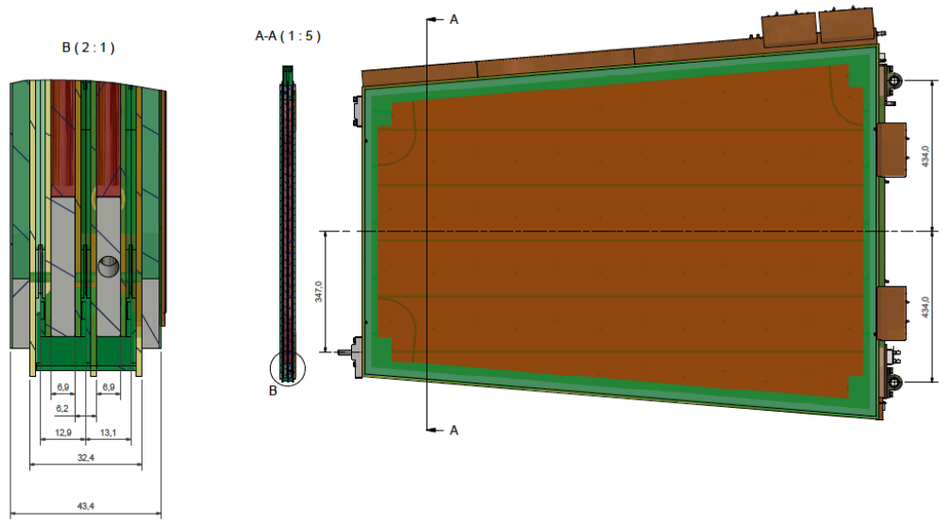
To maintain higher efficiency, **doublet chambers** can only be used in a **1/2 coincidence**.

To enable a more robust **2/3 coincidence**, doublet chambers will be replaced by **triplet chambers** with **finer readout granularity**.

The chamber designing is ongoing.

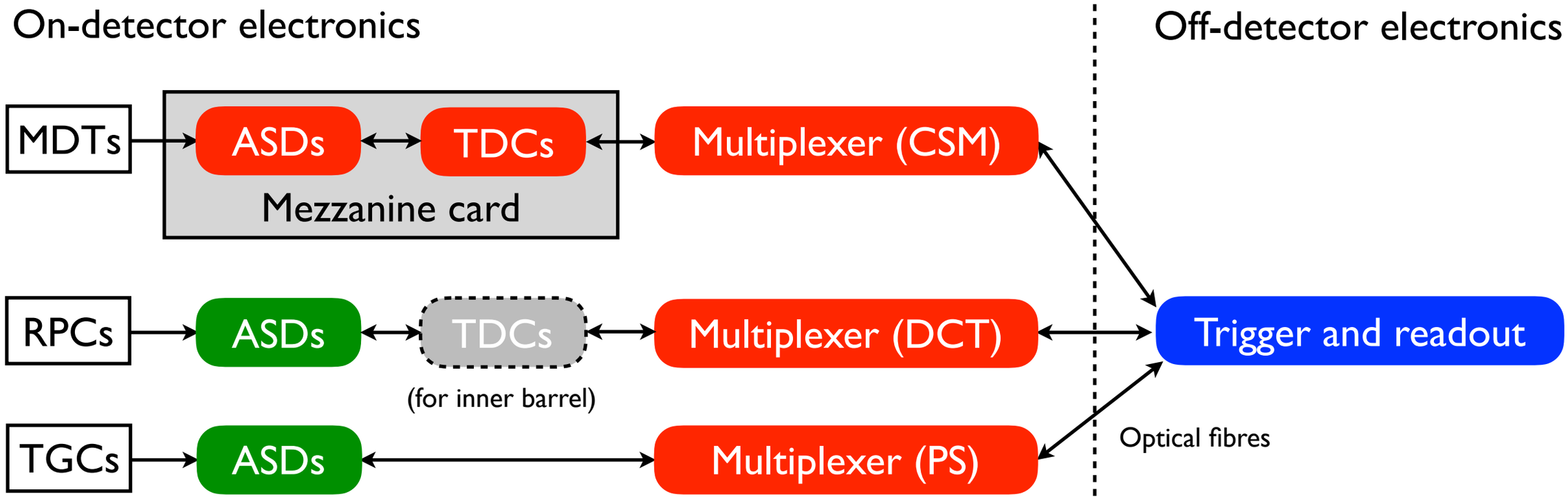


Trigger rate reduction with the current inner endcap TGC, will be improved by new TGC (1.05<|η|<1.3) and NSW (|η|>1.3)



Electronics Upgrade Overview

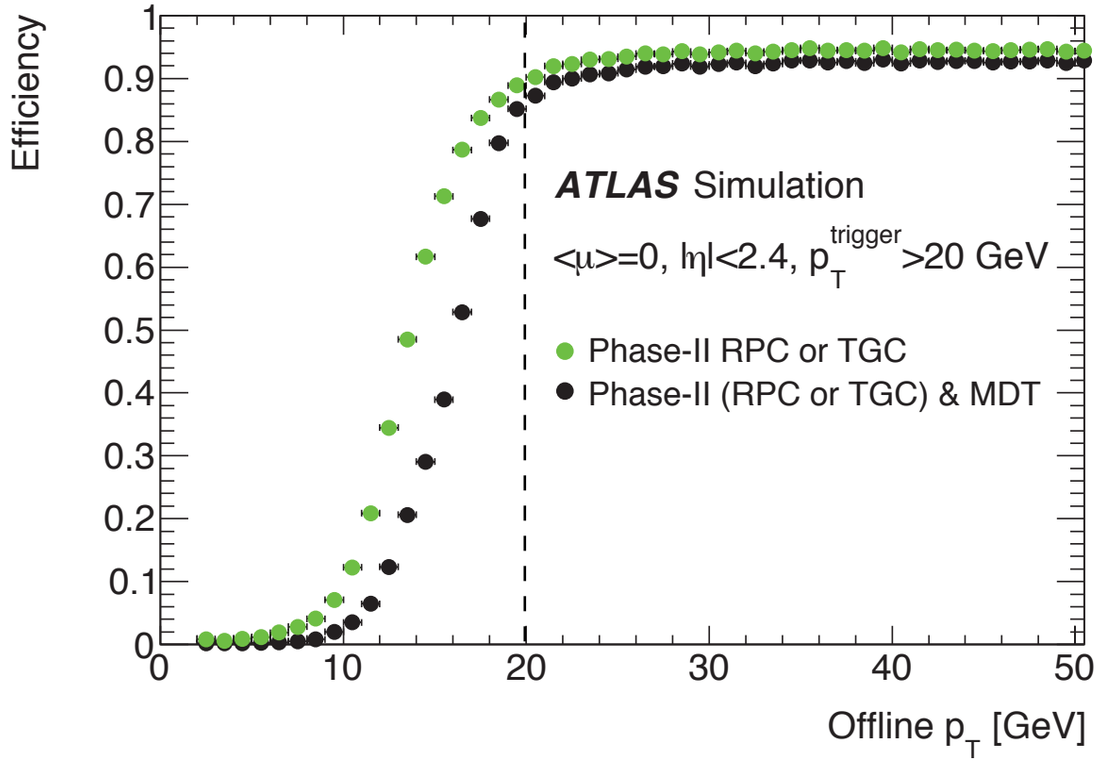
- The full electronics chain of **MDT** will be replaced, including frontend boards.
- For "old" **RPC** and **TGC**, the on-detector trigger and readout boxes will be replaced.
- **All data** will be sent to the off-detector electronics in **triggerless mode**,
  and all the trigger logic will be in the off-detector electronics.
- ASICs are already in prototyping phase, while the other parts are generally in designing phase.



MDT Trigger

Presently, MDT information is used only in high-level trigger and offline analysis. Resolution of p_T in the first-level trigger is limited by position resolution of RPC/TGC.

MDT will be included in L0 trigger at Phase II. MDT will **sharpen the p_T threshold** thanks to higher spacial resolution and **reject low-quality candidates**.



p_T resolution at p_T = 20 GeV: ~6%

Challenges in the latency. MDT hits are sent out every hit immediately, and only hits in regions of interest from RPC/TGC are processed. Fast tracking algorithm is used.

An estimate on the latency of MDT trigger: 3.8 μs, fitted to total L0 latency of 10 μs.

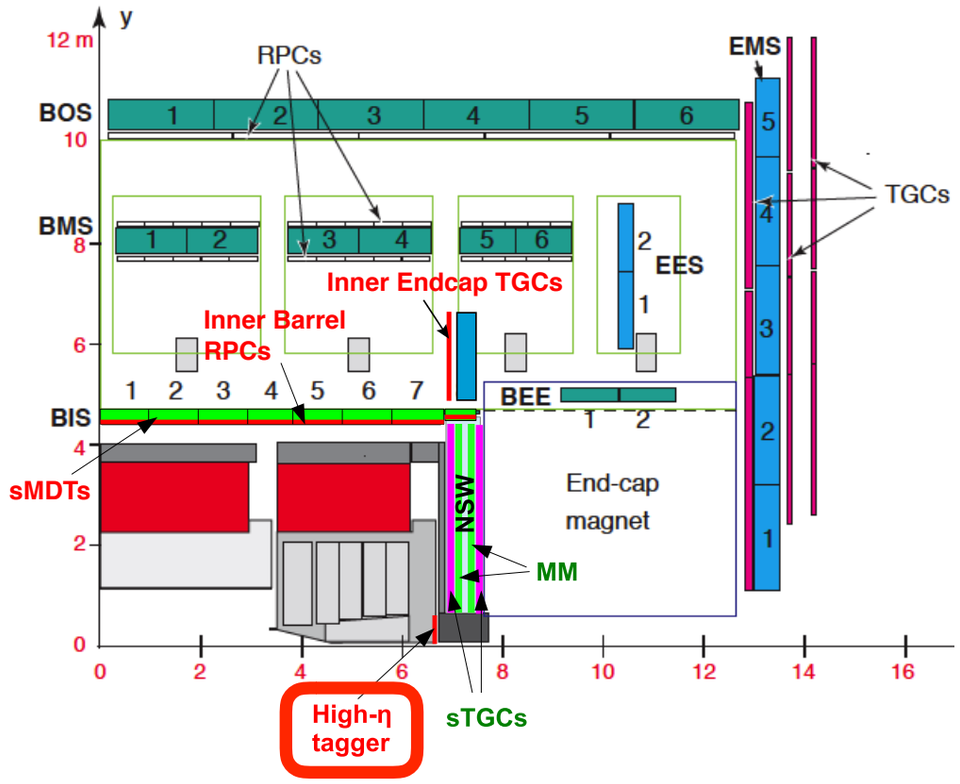
High-η Tagger (Option)

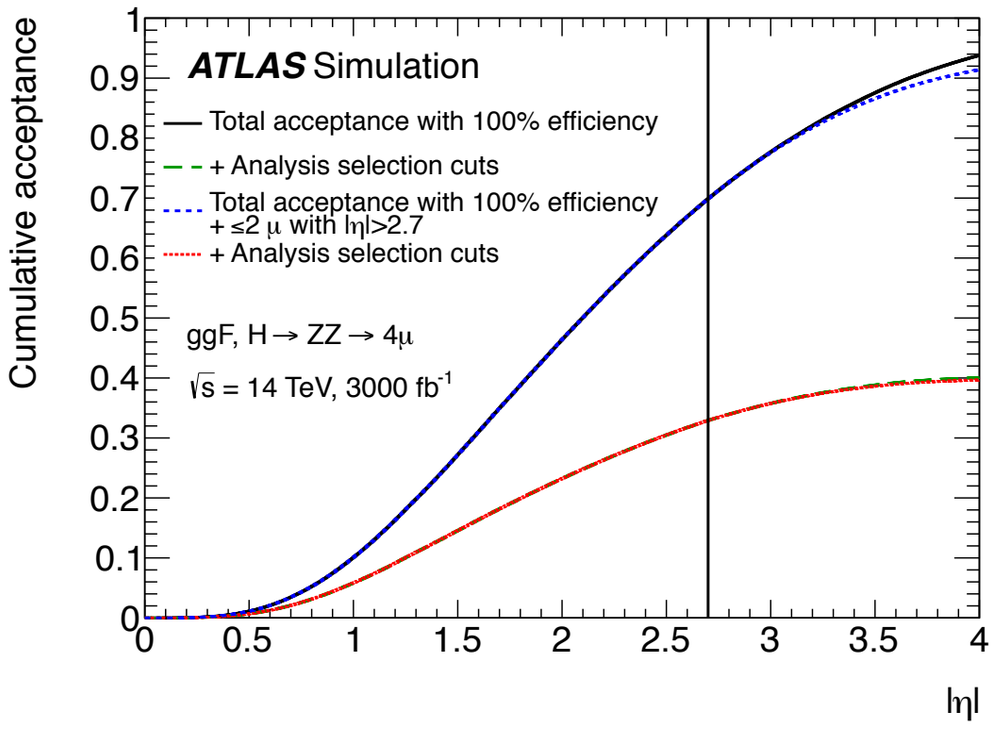
The replacement of the Inner Detector extends the coverage of tracking up to $|\eta| < 4.0$.

As a consequence, it becomes interesting to identify muons at such large $|\eta|$ values.

Installation of **micro-pattern gaseous or silicon pixel detectors in $2.7 < |\eta| < 4.0$** was proposed.

Physics potential and technical feasibility are under evaluation. For **ggF, $H \rightarrow ZZ^* \rightarrow 4\mu$**, **an acceptance gain of 22%** is expected.





Summary

The ATLAS Muon System will be upgraded to fully exploit the potential of precision SM studies and BSM searches at HL-LHC.

RPC and small-diameter MDT will be installed in the inner barrel layer to improve the acceptance of the muon trigger. TGC will be replaced in the inner endcap layer to suppress the trigger due to non-IP tracks.

The electronics for MDT, RPC, and TGC will be upgraded to retain trigger p_T thresholds. MDT will be included in L0 for an improved selectivity.

TDR was published in Dec. 2017. Designing and prototyping are ongoing.

Backup Slides

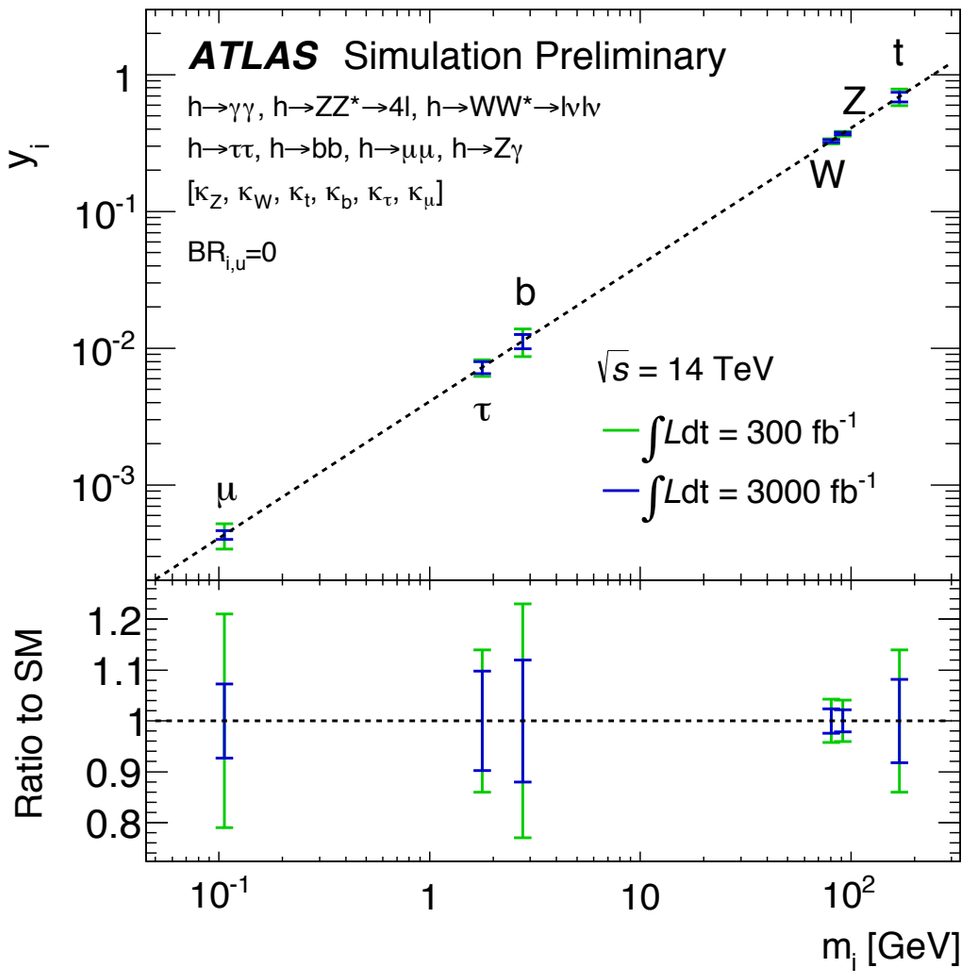
Role of the Muon System

The muon system is crucial for **full physics programs** of ATLAS.

Example: **Higgs physics**

- Contributed to Higgs boson observation.
- Important for precision Higgs boson coupling measurements.

ATL-PHYS-PUB-2014-016



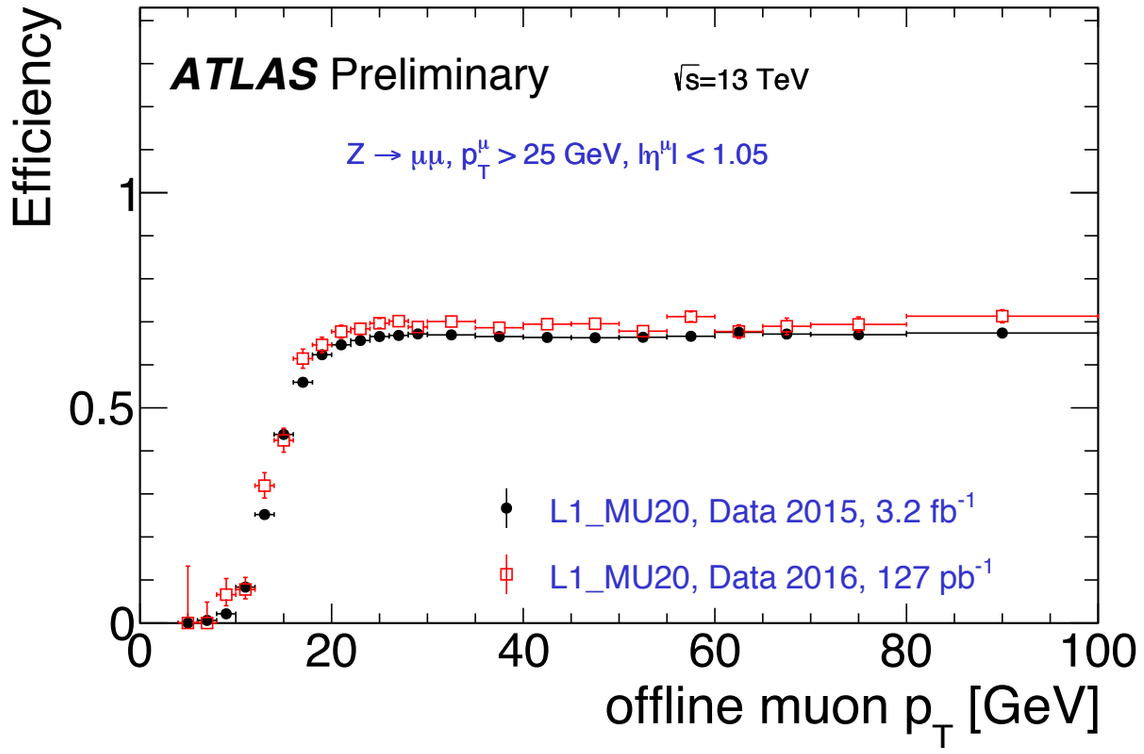
h→γγ, h→ZZ*→4l, h→WW*→lνlν

h→ττ, h→bb, h→μμ, h→Zγ

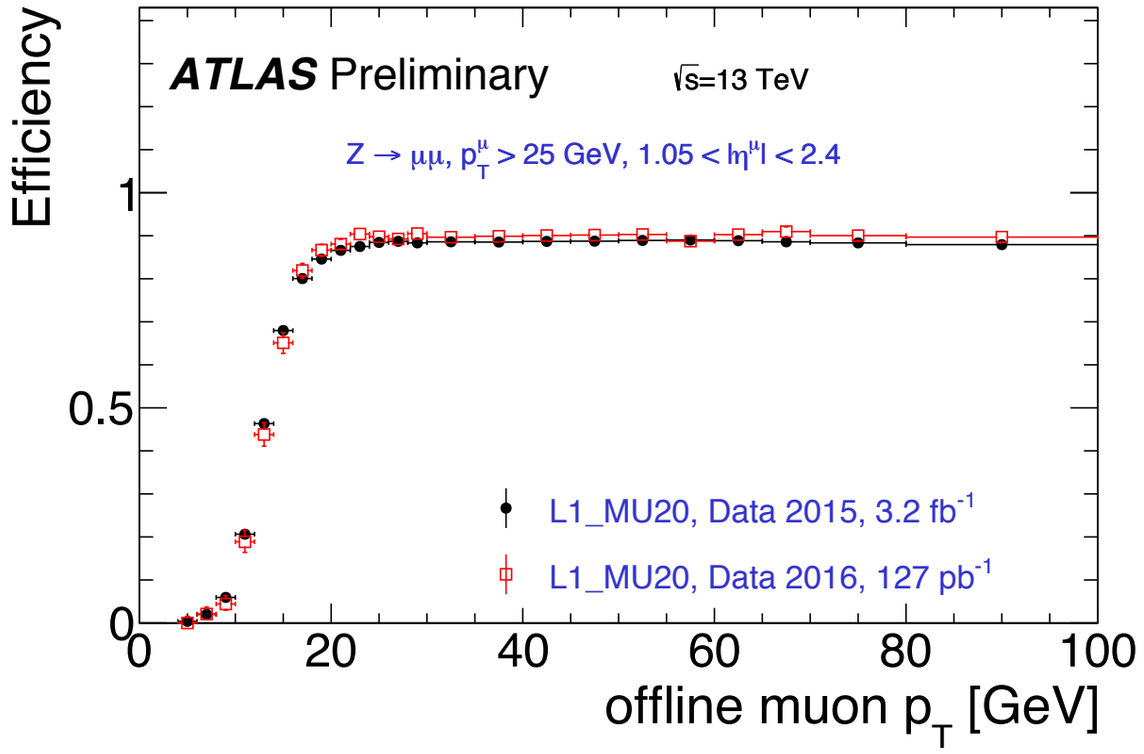
Zh, Wh, tth

Trigger Efficiency for Run 2

Barrel



Endcap

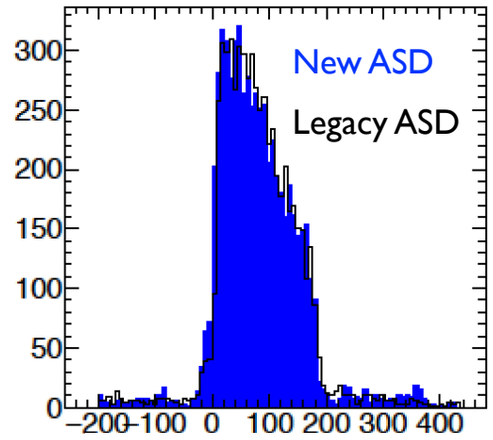


https://twiki.cern.ch/twiki/bin/view/AtlasPublic/MuonTriggerPublicResults

MDT Electronics Upgrade

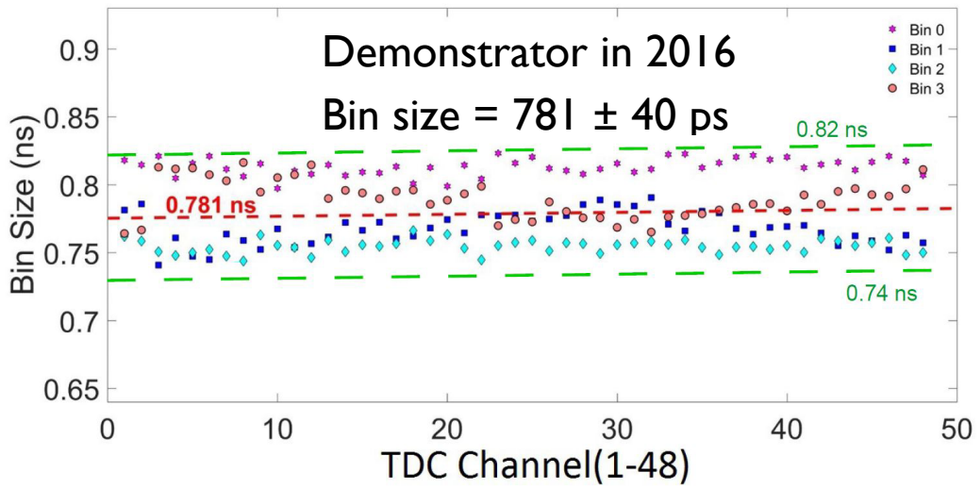
ASD (Amplifier-Shaper-Discriminator) ASIC

- Prototype chip has been developed in 2017 and all functions have been confirmed.
- Design of final prototype is ready.



TDC (Time-to-Digital Converter) ASIC

- Demonstrator chip has been developed in 2016 and the timing resolution has been verified.
- Submission of full-chip prototype in Aug. 2018.



Mezzanine Card

- Preliminary design exists, which will be updated after the packaging of ASICs is defined.

Multiplexer (CSM)

- Demonstration is ongoing for two options: FPGA-based and ASIC-based design.

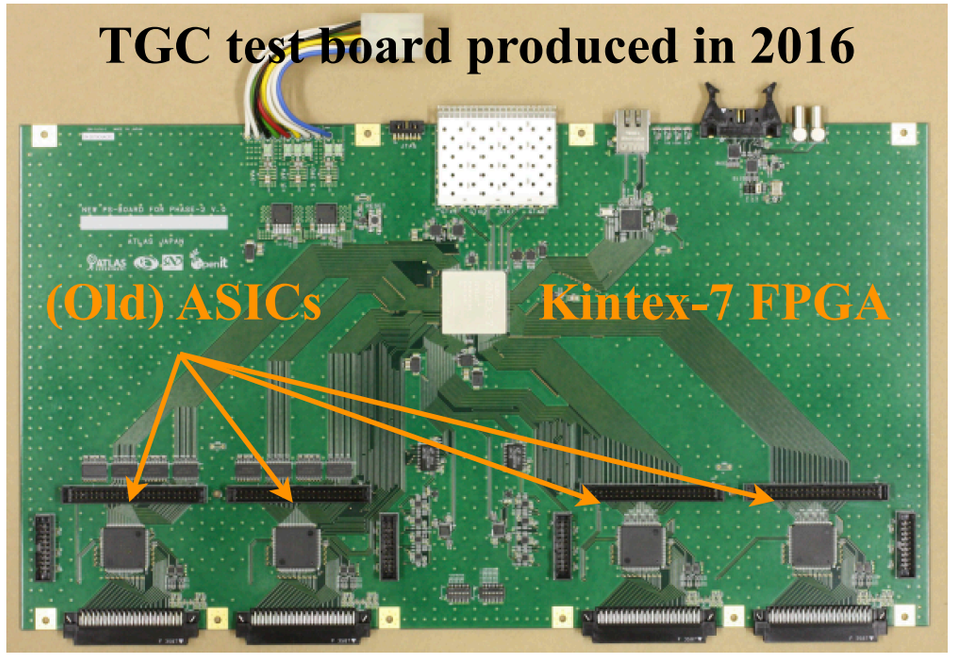
RPC and TGC Electronics Upgrade

RPC Electronics

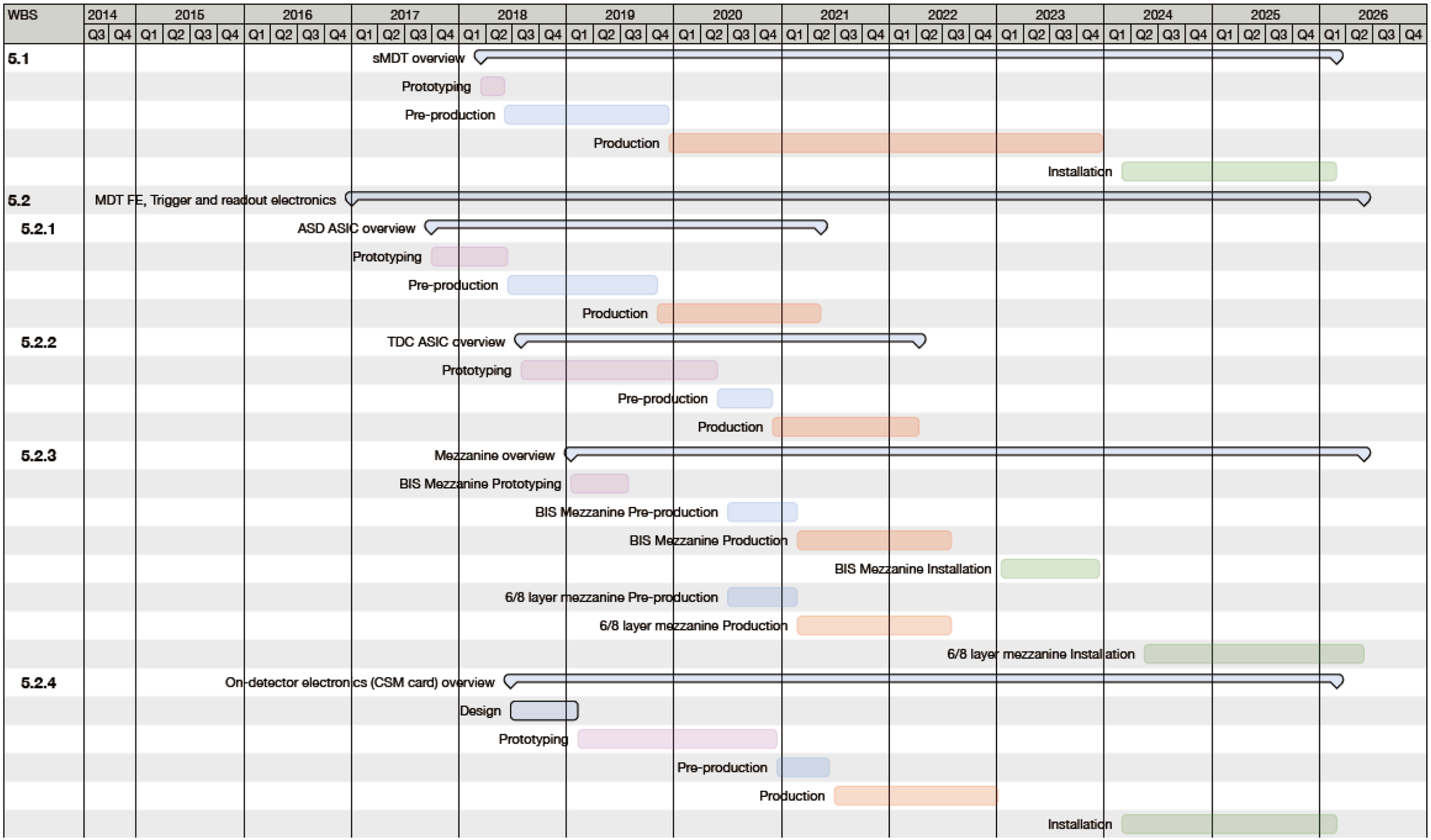
- Samples the RPC hit time with 1 ns resolution (3.125 ns in the current system) to improve time-of-flight measurements for rejecting background particles.
- For the inner barrel RPC, 100 ps TDC embedded in the frontend ASIC is foreseen.
- The designing is ongoing. The prototyping will start in 2019.

TGC Electronics

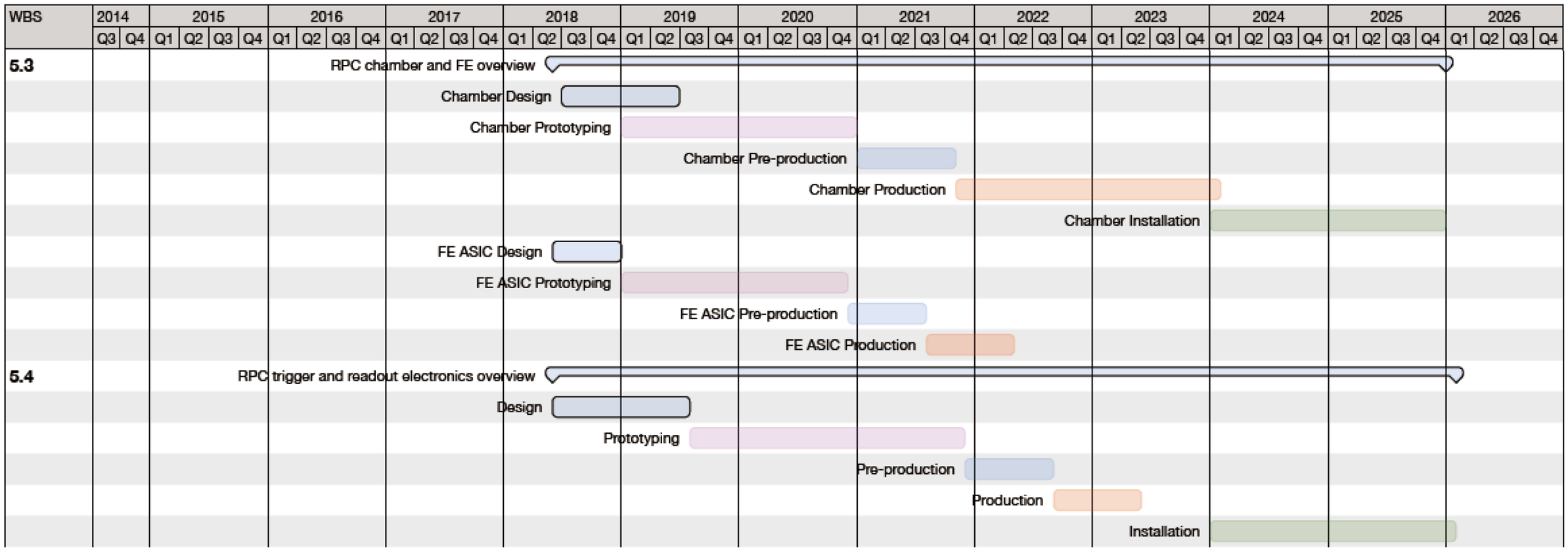
- A bunch crossing is assigned to each hit in ASIC, and data are transmitted from FPGA (8x2 Gbps).
- ASIC prototype chip was submitted in Jun. 2018.
- Data transmission was verified with a test board.



Schedule for MDT



Schedule for RPC



Schedule for TGC and Power System