Upgrade of the ATLAS Monitored Drift Tube Front-end Electronics for the HL-LHC

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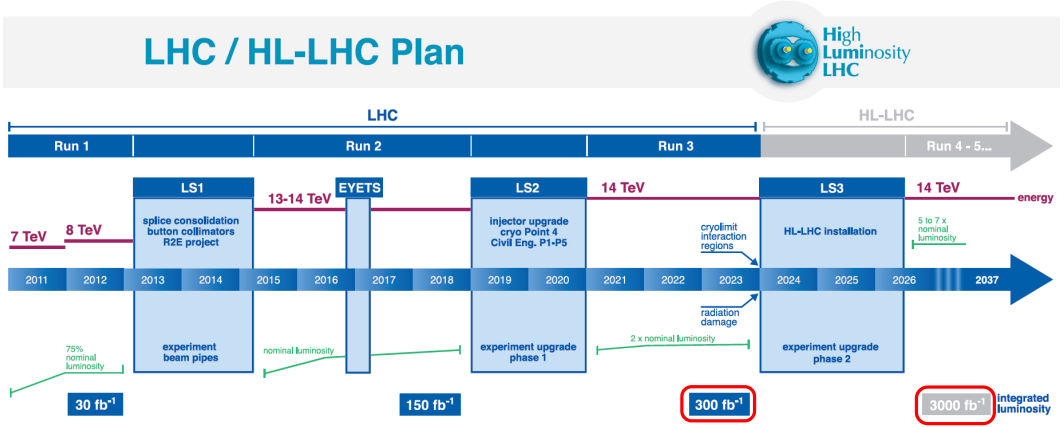
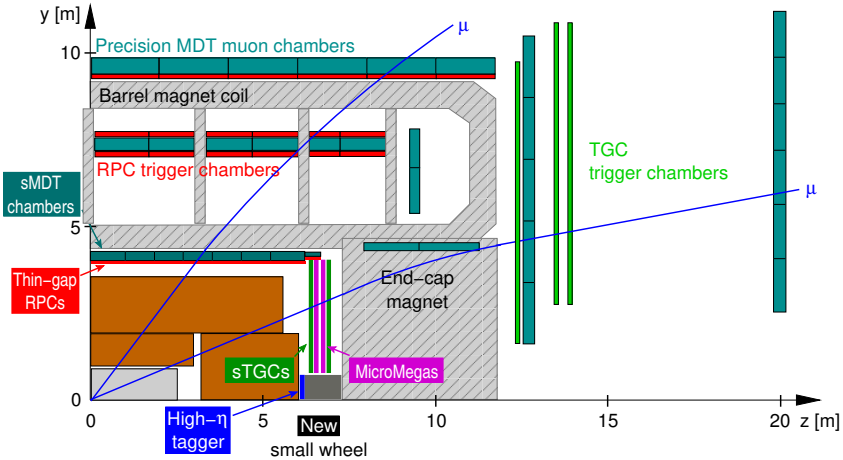
The roadmap to High-Luminosity LHC



- Plan to increase the LHC luminosity by an order of magnitude.
- Increase of the particle fluxes/rates by an order of magnitude from the LHC to the HL-LHC requires a major detector upgrade.
- Muon spectrometer upgrade in two steps during long shutdowns 2 and 3.

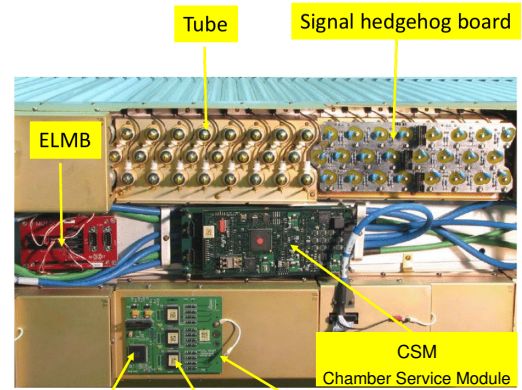
The ATLAS muon spectrometer at the HL-LHC



- New small wheel with high-resolution trigger chambers to reject fake muon triggers and improve momentum resolution at trigger level.
- New thin-gap RPCs to close acceptance gaps of the barrel muon trigger.
- New sMDT chambers to free space for new RPCs.
- New 1^{st} level muon trigger using MDT chamber information.

\+ New on- and off-chamber electronics for new trigger architecture.

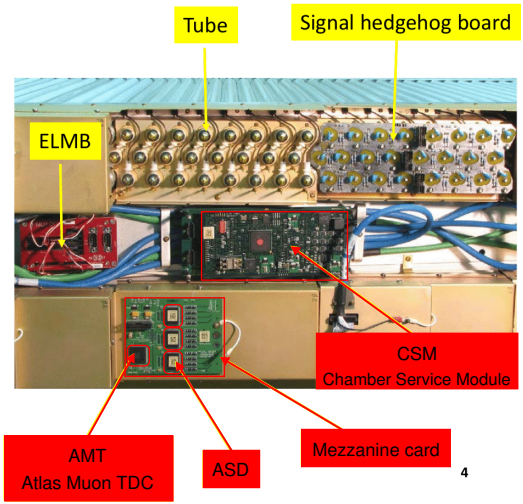
On-chamber MDT read-out electronics



Present read-out electronics

- Read-out in groups of 24 tubes (3×8 or 4×6).
- Passive part: Heghog cards with coupling capacitors.
- Active part:
  3 ASDs$\rightarrow$TDC
  18 TDCs$\rightarrow$CSM$\rightarrow$off-detector elx

On-chamber MDT read-out electronics



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Trigger requirements at the HL-LHC

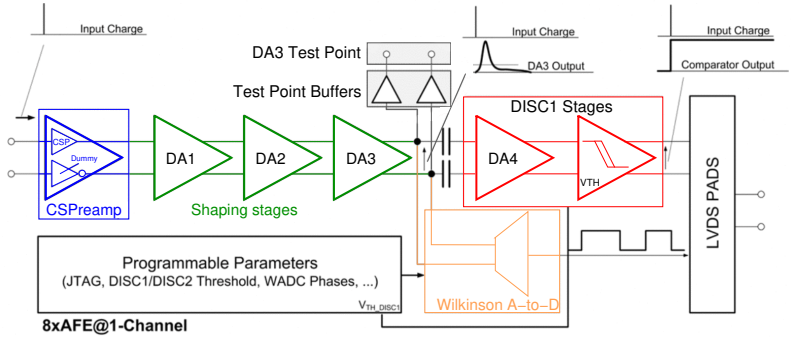
- 1^{st} level trigger rate will be increased from the present 100 kHz to 1-4 MHz.

⇒ Present TDCs and CSMs incompatible with trigger rates >200 kHz.

⇒ New on-chamber electronics needed for operation at the HL-LHC!

New Amplifier Shaper Discriminator (ASD) chip

- Present "legacy" ASD chip in 500 nm Agilent technology (obsolete).
- New ASD chip:
  - In 130 nm Global Foundries CMOS technology.
  - Design follows legacy chip with a fix of a specific design error of the legacy chip in the output logic.
- Block diagram of the new ASD chip

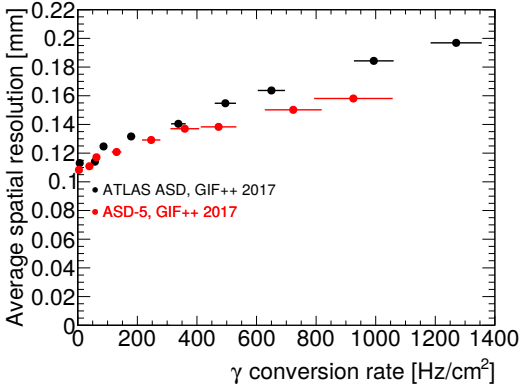


- Differential charge sensitive preamplifier.
- Bipolar shaping with ion tail cancellation.
- Wilkinson ADC for time-walk corrections to discriminated signals.

Test of the new ASD chip

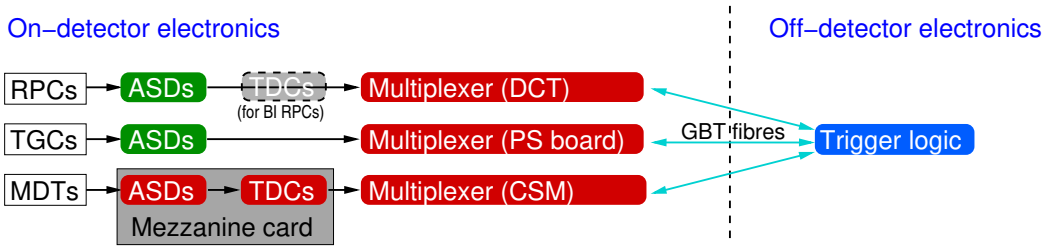
- The final version of the new ASD has been tested with test pulses and on an MDT chamber in the GIF++ at CERN.

Parameter	Unit	Specs	Legacy ASD	New ASD
Signal peaking time	ns	15	14.4	12
Amplification	mV/fC	8.9	10	21
Noise r.m.s	mV	8.5	8	4
Threshold spread	mV		12-16	4
Power consumption	mW		300	360



Performance of the new chip better than the legacy chip in terms of noise, threshold spread, and amplification leading to a better achievable spatial resolution!

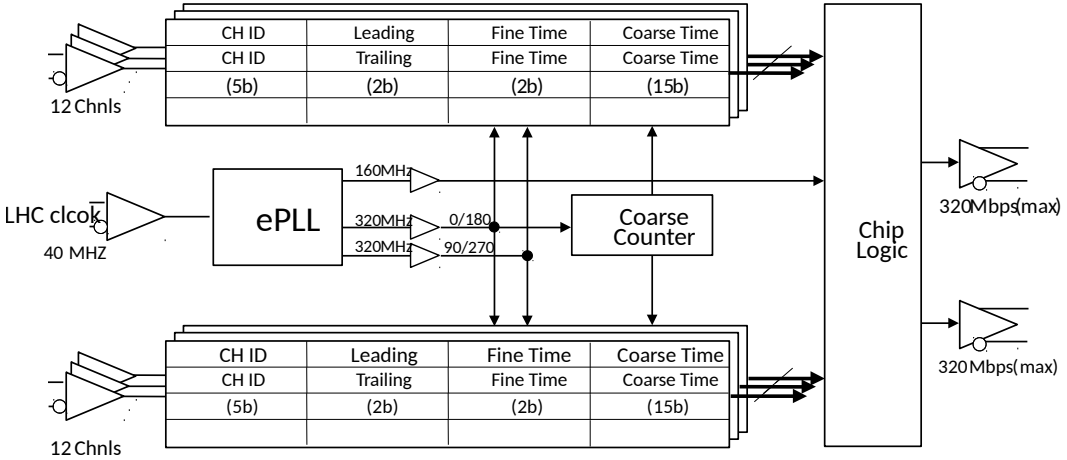
Read-out scheme and data rates at the HL-LHC



- Streamed read-out of all muon chambers at the HL-LHC to minimize trigger latency.
Max. rate [kHz/tube]	Mode	TDC output rate	CSM output rate
400	Edge mode	2×288 Mbps	2×5.2 Gbps
400	Pair mode	1×384 Mbps	1×6.9 Gbps

Edge mode: 24 bits for leading edge + 24 bits for trailing edge.
Pair mode: 32 bits for leading+trailing edge.
Data transfer after with 8b/10b encoding.

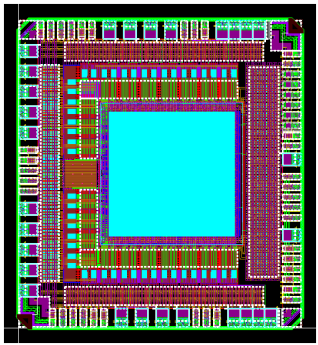
New Time-to-Digital Converter (TDC) chip



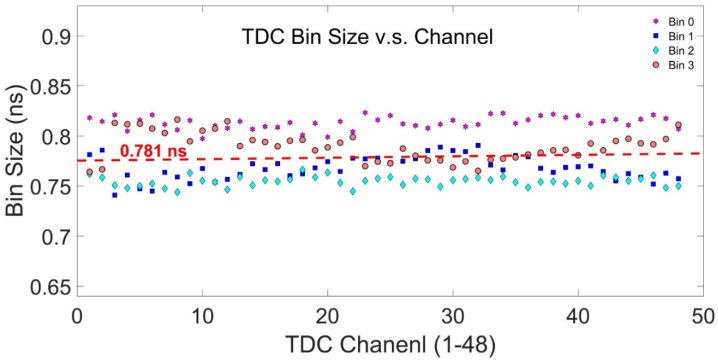
- Time measurement:
  - Coarse time in steps of 3.125 ns (15 bits).
  - Fine time in step of 3.125 ns/4=0.7815 ns (2 bits).
- Technology:
  - TDC demonstrator in 130 nm Global Foundries CMOS technology.
  - Prototypes and final chip in 130 nm TSMC CMOS technology.

Results from the TDC demonstrator

Floor plan



Time resolution



Excellent uniformity. Diffential and integral non-linearity: $\pm$40 ps!

New Chamber Service Module (CSM)

CSM tasks

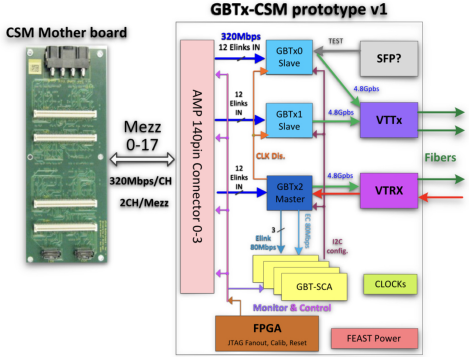
- Multiplexer collecting the data from up to 18 mezzanine cards and sending them downstream via high-speed optical links.
- Distribution of configuration information to the mezzanine cards via down-link.
- Passing of monitoring information from mezzanine cards and CSM via up-link.

Boundary conditions

- Design must be allow for the reuse of the existing cables from the mezzanine cards.
- Backward compatibility with legacy mezzanine cards for chambers where these cards are inaccessible for exchange with new cards.

Design options for the new CSM

Baseline: GBTx based



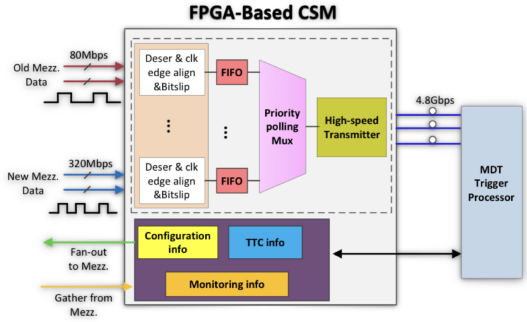
Advantages

- Support of low-power GBT.
- Radiation hard.

Disadvantage

- Difficult to achieve backward compatibility with legacy electronics.

Alternative: FPGA based



Advantages

- Reprogrammable.
- Backward compatibility with legacy electronics.

Disadvantages

- Limited radiation hardness.
- No support of low-power GBT so far.

Summary

- New ATLAS trigger scheme (1-4 MHz 1^{st} level trigger rate) requires new MDT chamber front-end electronics:
  - New on-chamber mezzanine cards with new ASD and TDC ASICs.
  - New on-chamber multiplexer, so-called "CSM".
- New ASD design completed in 130 nm Global Foundries CMOS technology, chip production in 2018/2019.
- TDC demonstrator in 130 nm Global Foundries CMOS technology completed and successfully tested in 2017.
  First prototype in 130 nm TSMC CMOS technology in preparation.
- Two options for CSM prototypes:
  - Baseline: GBTx based CSM.
  - Alternative for read-out of chambers with legacy electronics: FPGA based CSM.