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Frontend and backend electronics for the ATLAS New Small Wheel Upgrade

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The Phase-I and Phase-II upgrades of the LHC accelerator will increase the LHC instantaneous luminosity to 2×1034 cm−2s−1 and 7.5×1034 cm−2s−1, respectively. The luminosity increase drastically impacts the ATLAS trigger and readout data rates. The present ATLAS small wheel muon detector will be replaced with a New Small Wheel (NSW) detector in 2019. The NSW will feature two new detector technologies, Resistive Micromegas (MM) and small strip Thin Gap Chambers (sTGC) conforming a system of ~2.4 million readout channels. Both detectors will be used for muon triggering and precision tracking. A common readout path and two separate trigger paths are developed for these two detector technologies. The frontend electronics will be implemented in about 8000 boards including the design of 4 custom ASICs capable of driving trigger and tracking primitives to the backend trigger processor and readout system. The readout data flow is designed through a high-throughput network approach. The large number of readout channels, short time available to prepare and transmit trigger data, large volume of output data, harsh radiation environment, and the need of low power consumption all impose great challenges on the system design. We will present the overall design along with the status of all ASIC and board prototypes.

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